AUTOMOTIVE PRODUCTS

DATABOOK

1st EDITION

OCTOBER 1989

USE IN LIFE SUPPORT MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPOF DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS-THOMSC Microelectronics. As used herein:

1. Life support devices to systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life su port device or system whose failure to perform can t reasonably expected to cause the failure of the life su port device or system, or to affect its safety or effec veness.

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INTRODUCTION

The development of monolithic and discrete devices dedicated to the automotive sector has been the natural consequence of SGS-THOMSON's technological knowhow, especially in power IC technology , power packages and innovative solutions.

Thanks to this remarkable background, new technologies and circuits allow our devices to withstand the extremely hostile automotive environment: a very wide temperature and supply voltage range, accidental battery reversal, load dump transients, over and undervoltage spikes.

High side, low side, single and multi output drivers realized with these mixed technologies guarantee high current and high voltage performance together with diagnostic functions for external microcontrollers, enriching enormously the automotive product portfolio.

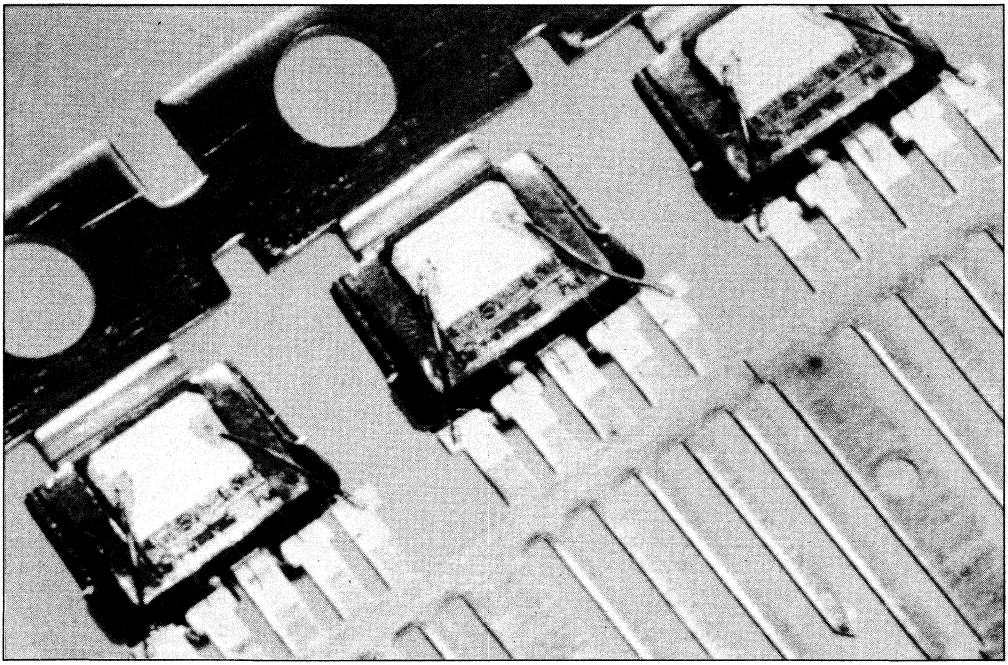
Intelligent power actuators like the L9821 and VM200 high side drivers, intelligent ignition circuits like the VB020 offer a completely new approach to power system design.

Many different memories and automotive dedicated microcontrollers like ST6 and ST9 make possible software and hardware integration in new advanced applications.

The company has been active in the automotive field for more than 15 years and today has design, marketing and engineering departments dedicated to this market.

Thanks to twenty years of uninterrupted leadership in audio amplifier technology SGS-THOMSON also offers a wide choice of rugged and cost-effective solutions for car entertainment.

SGS-THOMSON's automotive product portfolio covers a very broad range of powertrain, body electronics, instrumentation and vehicle control applications. For most of your design needs you will find the solution in this book.



Designed to drive lamps, relays and DC motors, the L9821 smart power driver car replace for the first time the relay used in car blinker circuits.

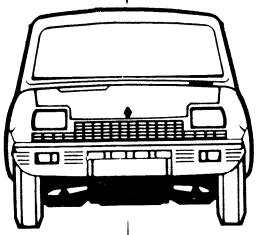
DEDICATED AUTOMOTIVE PRODUCTS

POWER TRAIN

- ☐ IGNITION CONTROL
- ☐ INJECTION SOLENOID DRIVERS/CONTROLLERS
- ☐ MICROCONTROLLERS WITH INTEGRATED DEDICATED PERIPHERALS
- ☐ EPROMS

BODY ELECTRONICS

- ☐ MONOLITHIC VOLTAGE REGULATORS FOR CHARGING SYSTEMS
- ☐ ACTUATORS FOR LIGHTING CONTROL
- ☐ MOTOR DRIVERS FOR MIRRORS, DOOR LOCKS AND SEATS
- ☐ MULTIPLEXING: BUS INTERFACE ICs
- ☐ CENTRALIZED AND DECENTRALIZED PROTECTION



INSTRUMENTATION

- ☐ LAMP CHECK ICs
- ☐ LIQUID LEVEL DETECTORS
- ☐ AUDIBLE ALARM ICs
- ☐ MULTIFUNCTION VOLTAGE REGULATORS
- ☐ MICROCONTROLLER WITH LCD DRIVE
- ☐ EEPROMS FOR DIAGNOSIS

VEHICLE CONTROL

- ☐ DEDICATED ICs FOR ABS SYSTEM
- ☐ POWER ACTUATORS FOR SUSPENSION AND STEERING
- ☐ TRANSMISSION VALVE SOLENOD DRIVERS

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MONOLITHIC POWER ACTUATORS

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ST18940/41	Digital Signal Processor	829

PROTECTION DEVICES

TRANSIL

P_P (W)	W_{RM} (V)	Type		Case	Page
		Unidirectional	Bidirectional		
400/1 ms	5.8 to 376	BZW04../BZW04P..	BZW04..B/BZW04P..B	F126	833
600/1 ms	5.8 to 376	P6KE.. P,A	P6KE..CP, CA	CB-417	839
300/1 ms	270	PL360D	—	F126	845
1500/1 ms	5.8 to 376	1.5KE...P,A	1.5KE...CP, CA	CB-429	851
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P_P (W)	W_{RM} (V)	Type		Case	Page
		Unidirectional	Bidirectional		
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	5.5 to 171	—	SM6T...C,A	CB-472	
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	5.5 to 171	—	SM15T...C,A	CB-473	

** NMOS UV EPROM

Part Number	Org.	Access Time	I_{CC} Max		V_{CC}	Temperature Range	Pin Count
			Act	St.by			
M2764AF6	8K x 8	250ns	75mA	35mA	5V ± 5%	−40 to +85°C	28
M2764A-4F6	8K x 8	450ns	75mA	35mA	5V ± 5%	−40 to +85°C	28
M27128AF6	16K x 8	250ns	85mA	40mA	5V ± 5%	−40 to +85°C	28
M27128A-4F6	16K x 8	450ns	85mA	40mA	5V ± 5%	−40 to +85°C	28
M27256F1	32K x 8	250ns	100mA	40mA	5V ± 5%	0 to +70°C	28
M27256-1F1	32K x 8	170ns	100mA	40mA	5V ± 5%	0 to +70°C	28
M27256-2F1	32K x 8	200ns	100mA	40mA	5V ± 5%	0 to +70°C	28
M27256-3F1	32K x 8	300ns	100mA	40mA	5V ± 5%	0 to +70°C	28
M27256-4F1	32K x 8	450ns	100mA	40mA	5V ± 5%	0 to +70°C	28
M27256-20F1	32K x 8	200ns	100mA	40mA	5V ± 10%	0 to +70°C	28
M27256-25F1	32K x 8	250ns	100mA	40mA	5V ± 10%	0 to +70°C	28
M27256-30F1	32K x 8	300ns	100mA	40mA	5V ± 10%	0 to +70°C	28
M27256-45F1	32K x 8	450ns	100mA	40mA	5V ± 10%	0 to +70°C	28
M27256F6	32K x 8	250ns	100mA	40mA	5V ± 5%	−40 to +85°C	28
M27256-4F6	32K x 8	450ns	100mA	40mA	5V ± 5%	−40 to +85°C	28
M27512F1	64K x 8	250ns	125mA	40mA	5V ± 5%	0 to +70°C	28
M27512-2F1	64K x 8	200ns	125mA	40mA	5V ± 5%	0 to +70°C	28
M27512-3F1	64K x 8	300ns	125mA	40mA	5V ± 5%	0 to +70°C	28
M27512-25F1	64K x 8	250ns	125mA	40mA	5V ± 10%	0 to +70°C	28
M27512-30F1	64K x 8	300ns	125mA	40mA	5V ± 10%	0 to +70°C	28
M27512F6	64K x 8	250ns	125mA	40mA	5V ± 5%	−40 to +85°C	28

** For Memory Datasheets consult our Memory Databook

** CMOS UV EPROM

Part Number	Org.	Access Time	I_{CC} Max		V_{CC}	Temperature Range	Pin Count
			Act	St.by			
TS27C64A-20VQ	8K x 8	200ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
TS27C64A-25VQ	8K x 8	250ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
TS27C64A-30VQ	8K x 8	300ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
TS27C256-20VQ	32K x 8	200ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
TS27C256-25VQ	32K x 8	250ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
TS27C256-30VQ	32K x 8	300ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
M27C1024-12XF1	64K x 16	120ns	50mA	1mA	5V ± 5%	0 to +70°C	40
M27C1024-15XF1	64K x 16	150ns	50mA	1mA	5V ± 5%	0 to +70°C	40
M27C1024-20XF1	64K x 16	200ns	50mA	1mA	5V ± 5%	0 to +70°C	40
M27C1024-25XF1	64K x 16	250ns	50mA	1mA	5V ± 5%	0 to +70°C	40
M27C1024-12F1	64K x 16	120ns	50mA	1mA	5V ± 5%	0 to +70°C	40
M27C1024-15F1	64K x 16	150ns	50mA	1mA	5V ± 10%	0 to +70°C	40
M27C1024-20F1	64K x 16	200ns	50mA	1mA	5V ± 10%	0 to +70°C	40
M27C1024-25F1	64K x 16	250ns	50mA	1mA	5V ± 10%	0 to +70°C	40
M27C1024-15XF6	64K x 16	150ns	50mA	1mA	5V ± 5%	−40 to +85°C	40
M27C1024-20XF6	64K x 16	200ns	50mA	1mA	5V ± 5%	−40 to +85°C	40
M27C1024-25XF6	64K x 16	250ns	50mA	1mA	5V ± 5%	−40 to +85°C	40
M27C256B-80XF1	32K x 8	80ns	50mA	1mA	5V ± 5%	0 to +70°C	28
M27C256B-12XF1	32K x 8	120ns	50mA	1mA	5V ± 5%	0 to +70°C	28
M27C256B-15XF1	32K x 8	150ns	50mA	1mA	5V ± 5%	0 to +70°C	28
M27C256B-80F1	32K x 8	80ns	50mA	1mA	5V ± 10%	0 to +70°C	28
M27C256B-12F1	32K x 8	120ns	50mA	1mA	5V ± 10%	0 to +70°C	28
M27C256B-15F1	32K x 8	150ns	50mA	1mA	5V ± 10%	0 to +70°C	28
M27C256B-12XF6	32K x 8	120ns	50mA	1mA	5V ± 5%	−40 to +85°C	28
M27C256B-15XF6	32K x 8	150ns	50mA	1mA	5V ± 5%	−40 to +85°C	28

** For Memory Datasheets consult our Memory Databook

**** CMOS UV EPROM** (Continued)

Part Number	Org.	Access Time	I_{CC} Max		V_{CC}	Temperature Range	Pin Count
			Act	St.by			
M87C257B-80XF1	32K x 8*	80ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M87C257B-12XF1	32K x 8*	120ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M87C257B-15XF1	32K x 8*	150ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M87C257B-80F1	32K x 8*	80ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M87C257B-12F1	32K x 8*	120ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M87C257B-15F1	32K x 8*	150ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M87C257B-12XF6	32K x 8*	120ns	50mA	1mA	5V ± 5%	−40 to + 85°C	28
M87C257B-15XF6	32K x 8*	150ns	50mA	1mA	5V ± 5%	−40 to + 85°C	28
M87C257B-12XF7	32K x 8*	120ns	50mA	1mA	5V ± 5%	−40 to + 105°C	28
M87C257B-15XF7	32K x 8*	150ns	50mA	1mA	5V ± 5%	−40 to + 105°C	28
M27C512-10XF1	64K x 8	100ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M27C512-12XF1	64K x 8	120ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M27C512-15XF1	64K x 8	150ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M27C512-20XF1	64K x 8	200ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M27C512-10F1	64K x 8	100ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M27C512-12F1	64K x 8	120ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M27C512-15F1	64K x 8	150ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M27C512-20F1	64K x 8	200ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M27C512-15XF6	64K x 8	150ns	50mA	1mA	5V ± 5%	−40 to + 85°C	28
M27C512-20XF6	64K x 8	200ns	50mA	1mA	5V ± 5%	−40 to + 85°C	28
M27C512-15XF7	64K x 8	150ns	50mA	1mA	5V ± 5%	−40 to + 105°C	28
M27C512-20XF7	64K x 8	200ns	50mA	1mA	5V ± 5%	−40 to + 105°C	28
M87C512-10XF1	64K x 8*	100ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M87C512-12XF1	64K x 8*	120ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M87C512-15XF1	64K x 8*	150ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M87C512-20XF1	64K x 8*	200ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M87C512-10F1	64K x 8*	100ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M87C512-12F1	64K x 8*	120ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M87C512-15F1	64K x 8*	100ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M87C512-20F1	64K x 8*	200ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M87C512-15XF6	64K x 8*	150ns	50mA	1mA	5V ± 5%	−40 to + 85°C	28
M87C512-20XF6	64K x 8*	200ns	50mA	1mA	5V ± 5%	−40 to + 85°C	28
M87C512-15XF7	64K x 8*	150ns	50mA	1mA	5V ± 5%	−40 to + 105°C	28
M87C512-20XF7	64K x 8*	200ns	50mA	1mA	5V ± 5%	−40 to + 105°C	28
M27C1001-12XF1	128K x 8	120ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M27C1001-15XF1	128K x 8	150ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M27C1001-20XF1	128K x 8	200ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M27C1001-25XF1	128K x 8	250ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M27C1001-12F1	128K x 8	120ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M27C1001-15F1	128K x 8	150ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M27C1001-20F1	128K x 8	200ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M27C1001-25F1	128K x 8	250ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M27C1001-15XF6	128K x 8	150ns	50mA	1mA	5V ± 5%	−40 to + 85°C	28
M27C1001-20XF6	128K x 8	200ns	50mA	1mA	5V ± 5%	−40 to + 85°C	28
M27C1001-25XF6	128K x 8	250ns	50mA	1mA	5V ± 5%	−40 to + 85°C	28
M87C1001-12XF1	128K x 8*	120ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M87C1001-15XF1	128K x 8*	150ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M87C1001-20XF1	128K x 8*	200ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M87C1001-25XF1	128K x 8*	250ns	50mA	1mA	5V ± 5%	0 to + 70°C	28
M87C1001-12F1	128K x 8*	120ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M87C1001-15F1	128K x 8*	150ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M87C1001-20F1	128K x 8*	200ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M87C1001-25F1	128K x 8*	250ns	50mA	1mA	5V ± 10%	0 to + 70°C	28
M87C1001-15XF6	128K x 8*	150ns	50mA	1mA	5V ± 5%	−40 to + 85°C	28
M87C1001-20XF6	128K x 8*	200ns	50mA	1mA	5V ± 5%	−40 to + 85°C	28
M87C1001-25XF6	128K x 8*	250ns	50mA	1mA	5V ± 5%	−40 to + 85°C	28

* Feature Address Latch

** For Memory Datasheets consult our Memory Databook

** NMOS OTP ROM

Part Number	Org.	Access Time	I_{CC} Max		V_{CC}	Temperature Range	Pin Count
			Act	St.by			
ST2764A-18CP	8K x 8	180ns	75mA	35mA	5V ± 10%	0 to +70°C	28
ST2764A-20CP	8K x 8	200ns	75mA	35mA	5V ± 10%	0 to +70°C	28
ST2764A-25CP	8K x 8	250ns	75mA	35mA	5V ± 10%	0 to +70°C	28
ST2764A-30CP	8K x 8	300ns	75mA	35mA	5V ± 10%	0 to +70°C	28
ST27128A-20CP	16K x 8	200ns	85mA	40mA	5V ± 10%	0 to +70°C	28
ST27128A-25CP	16K x 8	250ns	85mA	40mA	5V ± 10%	0 to +70°C	28
ST27128A-30CP	16K x 8	300ns	85mA	40mA	5V ± 10%	0 to +70°C	28
ST27256-20CP	32K x 8	200ns	100mA	40mA	5V ± 10%	0 to +70°C	28
ST27256-25CP	32K x 8	250ns	100mA	40mA	5V ± 10%	0 to +70°C	28
ST27256-30CP	32K x 8	300ns	100mA	40mA	5V ± 10%	0 to +70°C	28

** For Memory Datasheets consult our Memory Databook

** CMOS OTP ROM

Part Number	Org.	Access Time	I_{CC} Max		V_{CC}	Temperature Range	Pin Count
			Act	St.by			
TS27C64A-15CFN	8K x 8	150ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
TS27C64A-20CFN	8K x 8	200ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
TS27C64A-25CFN	8K x 8	250ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
TS27C64A-15VFN	8K x 8	150ns	30mA	1mA	5V ± 10%	−40 to + 85°C	32
TS27C64A-20VFN	8K x 8	200ns	30mA	1mA	5V ± 10%	−40 to + 85°C	32
TS27C64A-25VFN	8K x 8	250ns	30mA	1mA	5V ± 10%	−40 to + 85°C	32
TS27C64A-15TFN	8K x 8	150ns	30mA	1mA	5V ± 10%	−40 to +105°C	32
TS27C64A-20TFN	8K x 8	200ns	30mA	1mA	5V ± 10%	−40 to +105°C	32
TS27C64A-25TFN	8K x 8	250ns	30mA	1mA	5V ± 10%	−40 to +105°C	32
TS27C64A-15CP	8K x 8	150ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
TS27C64A-20CP	8K x 8	200ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
TS27C64A-25CP	8K x 8	250ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
TS27C64A-15VP	8K x 8	150ns	30mA	1mA	5V ± 10%	−40 to + 85°C	28
TS27C64A-20VP	8K x 8	200ns	30mA	1mA	5V ± 10%	−40 to + 85°C	28
TS27C64A-25VP	8K x 8	250ns	30mA	1mA	5V ± 10%	−40 to + 85°C	28
TS27C64A-15TP	8K x 8	150ns	30mA	1mA	5V ± 10%	−40 to +105°C	28
TS27C64A-20TP	8K x 8	200ns	30mA	1mA	5V ± 10%	−40 to +105°C	28
TS27C64A-25TP	8K x 8	250ns	30mA	1mA	5V ± 10%	−40 to +105°C	28
ST27C256-17CFN	32K x 8	170ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
ST27C256-20CFN	32K x 8	200ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
ST27C256-25CFN	32K x 8	250ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
ST27C256-17VFN	32K x 8	170ns	30mA	1mA	5V ± 10%	−40 to + 85°C	32
ST27C256-20VFN	32K x 8	200ns	30mA	1mA	5V ± 10%	−40 to + 85°C	32
ST27C256-25VFN	32K x 8	250ns	30mA	1mA	5V ± 10%	−40 to + 85°C	32
ST27C256-17TFN	32K x 8	170ns	30mA	1mA	5V ± 10%	−40 to +105°C	32
ST27C256-20TFN	32K x 8	200ns	30mA	1mA	5V ± 10%	−40 to +105°C	32
ST27C256-25TFN	32K x 8	250ns	30mA	1mA	5V ± 10%	−40 to +105°C	32
ST27C256-17CP	32K x 8	170ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
ST27C256-20CP	32K x 8	200ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
ST27C256-25CP	32K x 8	250ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
ST27C256-17VP	32K x 8	170ns	30mA	1mA	5V ± 10%	−40 to + 85°C	28
ST27C256-20VP	32K x 8	200ns	30mA	1mA	5V ± 10%	−40 to + 85°C	28
ST27C256-25VP	32K x 8	250ns	30mA	1mA	5V ± 10%	−40 to + 85°C	28
ST27C256-17TP	32K x 8	170ns	30mA	1mA	5V ± 10%	−40 to +105°C	28
ST27C256-20TP	32K x 8	200ns	30mA	1mA	5V ± 10%	−40 to +105°C	28
ST27C256-25TP	32K x 8	250ns	30mA	1mA	5V ± 10%	−40 to +105°C	28

** For Memory Datasheets consult our Memory Databook

** NMOS EEPROM

Part Number	Org.	Frequency	I_{CC} Max		V_{CC}	Temperature Range	Pin Count
			Act	St.by			
M9306B1	256 Bits	500KHz	5mA	3.5mA	5V ± 10%	0 to + 70°C	8
M9306B6	256 Bits	500KHz	5mA	4.0mA	5V ± 10%	−40 to + 85°C	8
M9306M1	256 Bits	500KHz	5mA	3.5mA	5V ± 10%	0 to + 70°C	8
M9306M6	256 Bits	500KHz	5mA	4.0mA	5V ± 10%	−40 to + 85°C	8
M9306M3	256 Bits	500KHz	5mA	4.5mA	5V ± 10%	−40 to + 125°C	8

** For Memory Datasheets consult our Memory Databook

** CMOS EEPROM

Part Number	Org.	Frequency	I_{CC} Max		V_{CC}	Temperature Range	Pin Count
			Act	St.by			
ST93C06AB1	256 Bits	1MHz	3mA	50µA	5V ± 10%	0 to + 70°C	8
ST93C06AB3	256 Bits	1MHz	5mA	100µA	5V ± 10%	−40 to + 125°C	8
ST93C06AM1	256 Bits	1MHz	3mA	50µA	5V ± 10%	0 to + 70°C	8
ST93C06AM6	256 Bits	1MHz	5mA	100µA	5V ± 10%	−40 to + 85°C	8
ST93C06AM3	256 Bits	1MHz	5mA	100µA	5V ± 10%	−40 to + 125°C	8
ST93C46AB1	1K Bits	1MHz	3mA	50µA	5V ± 10%	0 to + 70°C	8
ST93C46AB3	1K Bits	1MHz	5mA	100µA	5V ± 10%	−40 to + 125°C	8
ST93C46AM1	1K Bits	1MHz	3mA	50µA	5V ± 10%	0 to + 70°C	8
ST93C46AM6	1K Bits	1MHz	5mA	100µA	5V ± 10%	−40 to + 85°C	8
ST93C46AM3	1K Bits	1MHz	5mA	100µA	5V ± 10%	−40 to + 125°C	8
ST93CS56B1	2K Bits	1MHz	3mA	50µA	5V ± 10%	0 to + 70°C	8
ST93CS56B3	2K Bits	1MHz	5mA	100µA	5V ± 10%	−40 to + 125°C	8
ST93CS56M1	2K Bits	1MHz	3mA	50µA	5V ± 10%	0 to + 70°C	8
ST93CS56M6	2K Bits	1MHz	5mA	100µA	5V ± 10%	−40 to + 85°C	8
ST93CS56M3	2K Bits	1MHz	5mA	100µA	5V ± 10%	−40 to + 125°C	8
ST93CS57B1	2K Bits	500KHz	3mA	50µA	2.5 to 5.5V	0 to + 70°C	8
ST93CS57B3	2K Bits	500KHz	5mA	100µA	2.5 to 5.5V	−40 to + 125°C	8
ST93CS57M1	2K Bits	500KHz	3mA	50µA	2.5 to 5.5V	0 to + 70°C	8
ST93CS57M6	2K Bits	500KHz	5mA	100µA	2.5 to 5.5V	−40 to + 85°C	8
ST93CS57M3	2K Bits	500KHz	5mA	100µA	2.5 to 5.5V	−40 to + 125°C	8
ST24C02CP	2K Bits	100KHz	3mA	100µA	5V ± 10%	0 to + 70°C	8
ST24C02YVP	2K Bits	100KHz	5mA	100µA	5V ± 10%	−40 to + 85°C	8
ST24C04B1	4K Bits	100KHz	3mA	50µA	5V ± 10%	0 to + 70°C	8
ST24C04B3	4K Bits	100KHz	5mA	100µA	5V ± 10%	−40 to + 125°C	8
ST24C04M1	4K Bits	100KHz	3mA	50µA	5V ± 10%	0 to + 70°C	8
ST24C04M6	4K Bits	100KHz	5mA	100µA	5V ± 10%	−40 to + 85°C	8
ST24C04M3	4K Bits	100KHz	5mA	100µA	5V ± 10%	−40 to + 125°C	8
ST24C16B1	16K Bits	100KHz	4mA	50µA	5V ± 10%	0 to + 70°C	8
ST24C16B3	16K Bits	100KHz	6mA	100µA	5V ± 10%	−40 to + 125°C	8

** For Memory Datasheets consult our Memory Databook

** SRAM

Part Number	Org.	Access Time	Cycle Time	I_{CC} Max		Temperature Range	Pin Count
				Act	St.by		
MK6116N-15	2K x 8	150ns	150mA	70mA	3mA	0°C to 70°C	24
MK6116N-20	2K x 8	200ns	200ns	70mA	3mA	0°C to 70°C	24
MK6116N-25	2K x 8	250ns	250ns	70mA	3mA	0°C to 70°C	24

** For Memory Datasheets consult our Memory Databook

** ZEROPOWER

Part Number	Org.	Access Time	I_{CC} Max		V_{CC}	Temperature Range	Pin Count
			Act	St.by			
MKI48Z12B12	2K x 8	120ns	80mA	3mA	5V ± 10%	−40 to +85°C	24
MKI48Z12B15	2K x 8	150ns	80mA	3mA	5V ± 10%	−40 to +85°C	24
MKI48Z12B20	2K x 8	200ns	80mA	3mA	5V ± 10%	−40 to +85°C	24
MKI48Z12B25	2K x 8	250ns	80mA	3mA	5V ± 10%	−40 to +85°C	24
MKI48Z12BU12	2K x 8	120ns	80mA	3mA	5V ± 10%	−40 to +85°C	24
MKI48Z12BU15	2K x 8	150ns	80mA	3mA	5V ± 10%	−40 to +85°C	24
MKI48Z12BU20	2K x 8	200ns	80mA	3mA	5V ± 10%	−40 to +85°C	24
MKI48Z12BU25	2K x 8	250ns	80mA	3mA	5V ± 10%	−40 to +85°C	24

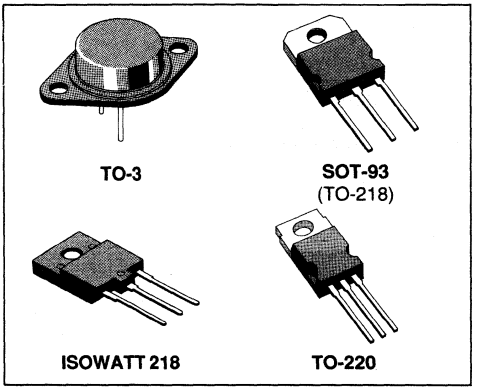
** For Memory Datasheets consult our Memory Databook

DATASHEETS

BU920/P/PFI/T
BU921/P/PFI/T
BU922/P/PFI/T

HIGH VOLTAGE POWER DISSIPATION

- HIGH VOLTAGE POWER DARLINGTON
- AUTOMOTIVE IGNITION APPLICATIONS
- HIGH CURRENT

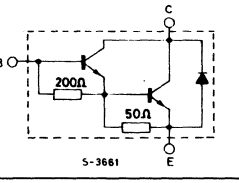


DESCRIPTION

The BU920/921/922, BU920P/921P/922P, BU920-PFI/BU921PFI/BU922PFI and BU920T/921T/922T are silicon multiepitaxial planar NPN transistors in monolithic darlington configuration mounted respectively in Jedec TO-3 metal case, SOT-93 plastic package, ISOWATT218 fully isolated package and TO-220 plastic package.

They are particularly intended for automative ignition applications and inverter circuits for motor control.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value				Unit
	TO-3 SOT-93 ISOWATT218 TO-220	BU920 BU920P BU920PFI BU920T		BU921 BU921P BU921PFI BU921T	BU922 BU922P BU922PFI BU922T	
V_{CES}	Collector-emitter Voltage (V_{BE} = 0)	400		450	500	V
V_{CEO}	Collector-emitter Voltage (I_B = 0)	350		400	450	V
V_{EBO}	Emitter-base Voltage (I_C = 0)	5				V
I_C	Collector Current	10				A
I_{CM}	Collector Peak Current	15				A
I_B	Base Current	5				A
		TO-3	SOT-93	ISOWATT218	TO-220	
P_{tot}	Total Dissipation at $T_c \leq 25$ °C	120	105	55	105	W
T_{stg}	Storage Temperature – 65 to	175	150	150	150	°C
T_j	Max. Operating Junction Temperature	175	150	150	150	°C

THERMAL DATA

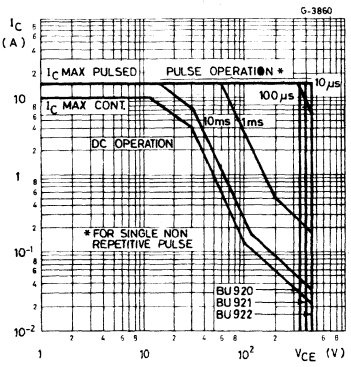
			TO-3	SOT-93	ISOWATT218	TO-220	
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.25	1.2	2.27•	1.2	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

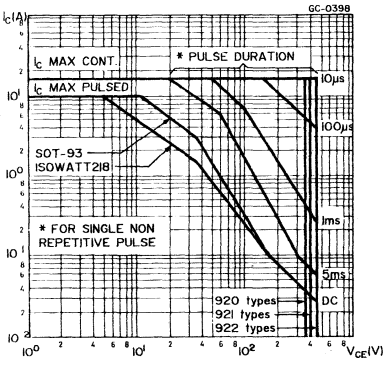
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cutoff Current (V_{BE} = 0)	V_{CE} = 400 V for **920 Types** V_{CE} = 450 V for **921 Types** V_{CE} = 500 V for **922 Types** V_{CE} = 400 V for **920 Types** V_{CE} = 450 V for **921 Types** V_{CE} = 500 V for **922 Types** T_c = 150 °C			250 250 250 0.5 0.5 0.5	µA µA µA mA mA mA
I_{CEO}	Collector Cutoff Current (I_B = 0)	V_{CE} = 350 V for **920 Types** V_{CE} = 400 V for **921 Types** V_{CE} = 450 V for **922 Types**			250 250 250	µA µA µA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{EB} = 5 V			50	mA
$V_{CEO(sus)}$*	Collector-emitter Sustaining Voltage	I_C = 100 mA for **920 Types** for **921 Types** for **922 Types**	350 400 450			V V V
$V_{CE(sat)}$*	Collector-emitter Saturation Voltage	I_C = 5 A I_B = 50 mA I_C = 7 A I_B = 140 mA			1.8 1.8	V V
$V_{BE(sat)}$*	Base-emitter Saturation Voltage	I_C = 5 A I_B = 50 mA I_C = 7 A I_B = 140 mA			2.2 2.5	V V
V_F	Diode Forward Voltage	I_F = 7 A			2.5	V
	Functional Test (see test circuit Fig.2 and 3)	for **920 Types** V_{CE} = 350 V L = 7 mH for **921 and 922 Types** V_{CE} = 400 V L = 7 mH	7 7			A A

* Pulsed : pulse duration = 300 µs, duty cycle = 1.5 %.

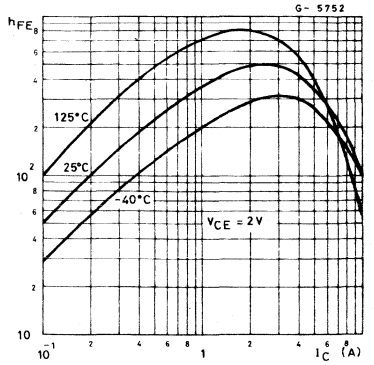
Safe Operating Areas.



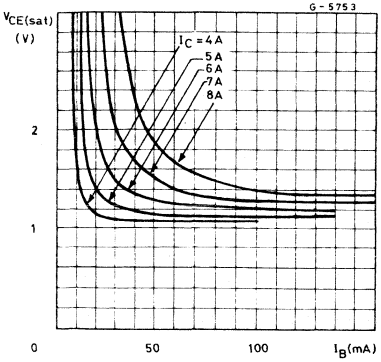
Safe Operating Areas.



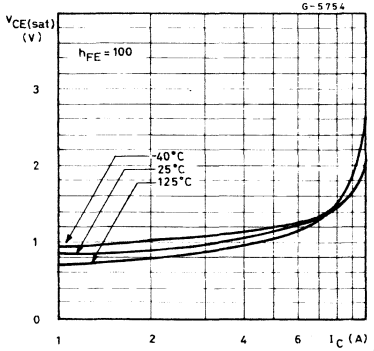
DC Current Gain.



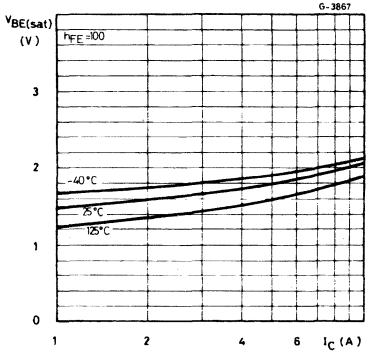
Colltector-emitter Saturation Voltage.



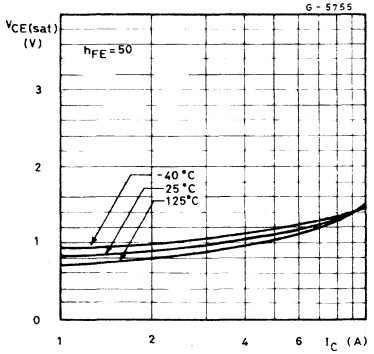
Collector-emitter Saturation Voltage.



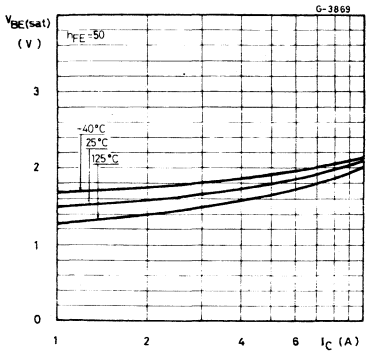
Base-emitter Saturation Voltage.



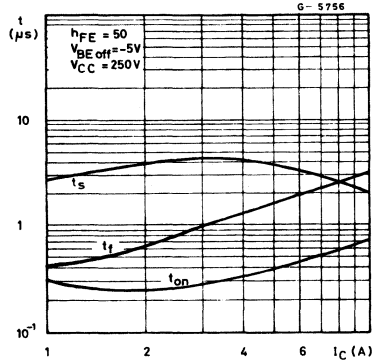
Collector-emitter Saturation Voltage.



Base-emitter Saturation Voltage.



Saturated Switching Characteristics.



Clamped Reverse Bias Safe Operating Areas.

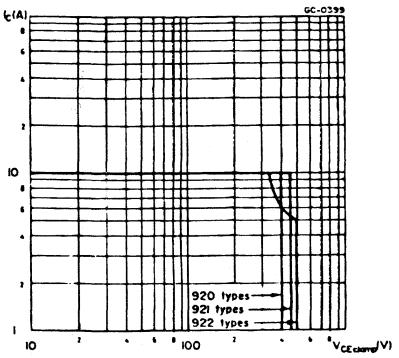
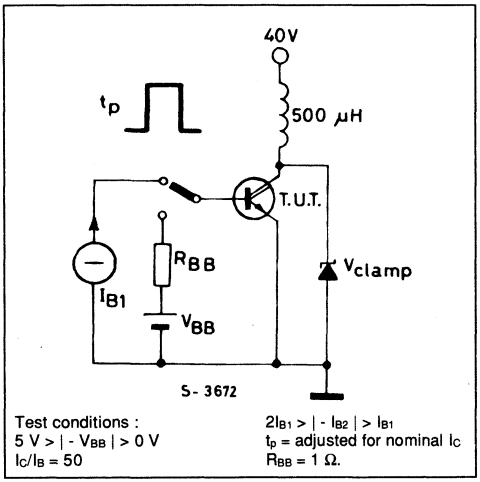
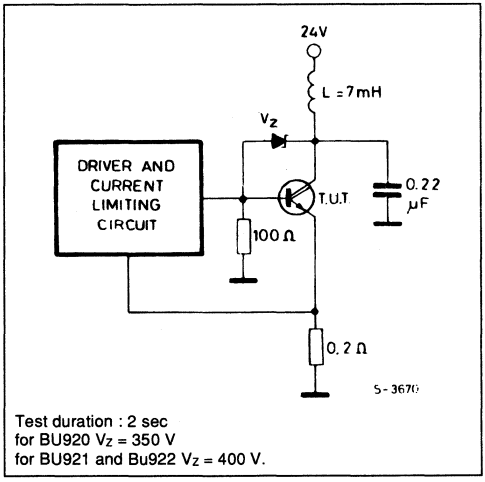


Figure 1 : Clamped $E_{S/O}$ Test Circuit.



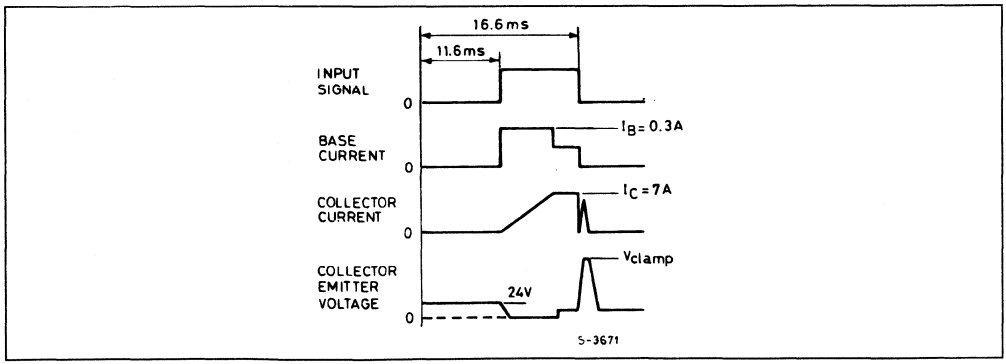
Test conditions :
5 V > | - V_{BB} | > 0 V
I_C/I_B = 50
$2I_{B1}$ > | - I_{B2} | > I_{B1}
t_p = adjusted for nominal I_C
R_{BB} = 1 Ω.

Figure 2 : Functional Test Circuit.



Test duration : 2 sec
for BU920 V_Z = 350 V
for BU921 and Bu922 V_Z = 400 V.

Figure 3 : Functional Test Waveforms.



ISOWATT 218 PACKAGE CHARACTERISTICS AND APPLICATION

ISOWATT218 is fully isolated to 4000 V dc. Its thermal impedance, given in the data sheet, is optimized to give efficient thermal conduction together with excellent electrical isolation.

The structure of the case ensures optimum distances between the pins and heatsink. These distances are in agreement with VDE and UL creepage and clearance standards. The ISOWATT218 package eliminates the need for external isolation so reducing fixing hardware.

The package is supplied with leads longer than the standard TO-218 to allow easy mounting on pcbs. Accurate moulding techniques used in manufacture assures consistent heat spreader-to-heatsink capacitance.

ISOWATT218 thermal performance is better than that of the standard part, mounted with a 0.1 mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT218 packages is determined by :

$$P_D = \frac{T_j - T_c}{R_{th}}$$

THERMAL IMPEDANCE OF ISOWATT 218 PACKAGE

Fig. 4 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT218 package.

The total thermal resistance $R_{th(tot)}$ is the sum of each of these elements.

The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows :

1 - for a short duration power pulse less than 1 ms ;

$$Z_{th}\ R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5 ms to 50 ms :

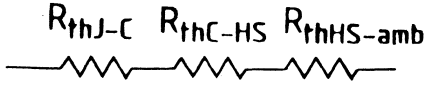
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500 ms or greater :

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

It is often possible to discern these areas on transient thermal impedance curves.

Figure 4.



SGS-THOMSON MICROELECTRONICS

BU921ZP/ZPFI
BU921ZT/ZTFI

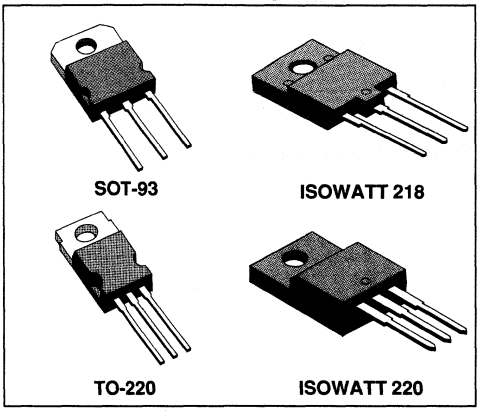
NPN POWER DARLINGTON

ADVANCE DATA

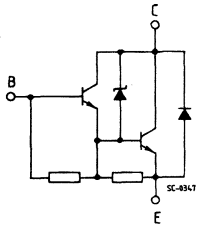
- HIGH RUGGEDNESS
- INTEGRATED HIGH VOLTAGE ZENER

AUTOMOTIVE MARKET

- APPLICATION IN HIGH PERFORMANCE ELECTRONIC CAR IGNITION



INTERNAL SCHEMATIC DIAGRAM



DESCRIPTION

The BU921ZP, BU921ZT, BU921ZPFI and BU921ZTFI are silicon multiepitaxial biplanar NPN transistors in monolithic darlington configuration mounted respectively in SOT-93, TO-220 plastic packages and ISOWATT218, ISOWATT220 fully isolated packages.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value				Unit
V_{CBO}	Collector-base Voltage (I_E = 0)	350				V
V_{CER}	Collector-emitter Voltage (R_{BE} = 100 Ω)	350				V
V_{CES}	Collector-emitter Voltage (V_{BE} = 0)	350				V
V_{CEO}	Collector-emitter Voltage (I_B = 0)	350				V
V_{EBO}	Emitter-base Voltage (I_C = 0)	5				V
I_C	Collector Current	16				A
I_B	Base Current	5				A
		SOT-93	**ISOWATT218**	**TO-220**	**ISOWATT220**	
P_{tot}	Total Dissipation at T_c < 25 °C	125	60	100	40	W
T_{stg}	Storage Temperature	– 40 to 150				°C
T_j	Max. Operating Junction Temperature	150				°C

THERMAL DATA

			SOT-93	ISOWATT218	TO-220	ISOWATT220	
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1	2.08	1.25	3.12	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CEO}	Collector Cut-off Current (I_B = 0)	V_{CE} = 350 V			250	μA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{BE} = − 5 V			50	mA
V_{CL}	Clamping Voltage	either I_B = 0 or V_{BE} = 0 and I_C = 100 mA same T_j = 125 °C	 350 350		 500 500	 V V
$V_{CE(sat)}$*	Collector-emitter Saturation Voltage	I_C = 5 A I_B = 50 mA I_C = 6 A I_B = 75 mA I_C = 8 A I_B = 120 mA T_j = 125 °C I_C = 5 A I_B = 50 mA I_C = 6 A I_B = 75 mA I_C = 8 A I_B = 120 mA		1.03 1.08 1.17 0.98 1.04 1.17	1.4 1.5 1.6	V V V V V V
$V_{BE(sat)}$*	Base-emitter Saturation Voltage	I_C = 6 A I_B = 75 mA I_C = 8 A I_B = 120 mA			2.2 2.3	V V
h_{FE}	DC Current Gain	I_C = 5 A V_{CE} = 10 V	300			
V_F*	Diode Forward Voltage	I_F = 10 A			2.5	V
	USE TEST	V_{CC} = 24 V L = 8 mH	8			A

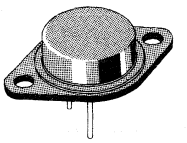
* Pulsed : pulsed duration = 300 μs, duty cycle = 1.5 %.

SGS-THOMSON MICROELECTRONICS

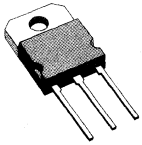
BU931R/RP/RPFI
BU932R/RP/RPFI

NPN POWER DARLINGTON

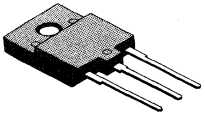
- AUTOMOTIVE MARKET
- HIGH PERFORMANCE ELECTRONIC IGNITION DARLINGTON
- HIGH RUGGEDNESS



TO-3



SOT-93
(TO-218)

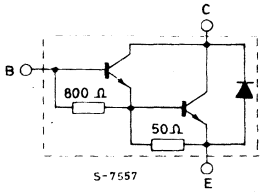


ISOWATT 218

DESCRIPTION

These devices are multiepitaxial biplanar NPN transistors in monolithic darlington configuration mounted in TO-3, SOT-93 and ISOWATT218 packages. They are specially intended for automotive ignition applications and invertes circuits for motor controls. Controlled performances in the linear region make them particularly suitable for car ignitions where current limiting is achieved desaturing the darlington.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
	TO-3 SOT-93 ISOWATT218	BU931R BU931RP BU931RPFI		BU932R BU932RP BU932RPFI	
V_{CES}	Collector-emitter Voltage (V_{BE} = 0)	450		500	V
V_{CEO}	Collector-emitter Voltage (I_{BE} = 0)	400		450	V
V_{EBO}	Emitter-base Voltage (I_C = 0)	5			V
I_C	Collector Current	15			A
I_{CM}	Collector Peak Current ($t_p \leq 10$ ms)	30			A
I_B	Base Current	1			A
I_{BM}	Base Peak Current ($t_p \leq$ 10 ms)	5			A
		TO-3	SOT-93	ISOWATT218	
P_{tot}	Total Dissipation at $T_C \leq 25°C$	175	125	60	W
T_{stg}	Storage Temperature	−40 to 200	−40 to 150	−40 to 150	°C
T_J	Max. Operating Junction Temperature	200	150	150	°C

THERMAL DATA

			TO-3	SOT-93	ISOWATT218	
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1	1	2.08•	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

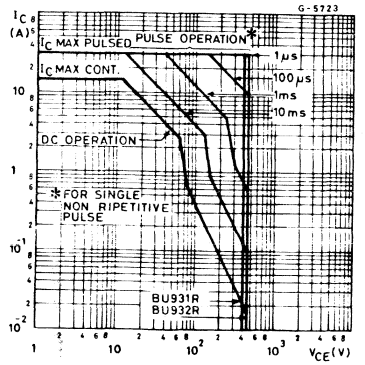
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cutoff Current (V_{BE} = 0)	for **BU931R/BU931RP/BU931RPFI**				
		V_{CE} = 450 V			1	mA
		V_{CE} = 450 V T_c = 125 °C			5	mA
		for **BU932R/BU932RP/BU932RPFI**				
		V_{CE} = 500 V			1	mA
		V_{CE} = 500 V T_c = 125 °C			5	mA
I_{CEO}	Collector Cutoff Current (I_B = 0)	for **BU931R/BU931RP/BU931RPFI**				
		V_{CE} = 400 V			1	mA
		for **BU932R/BU932RP/BU932RPFI**				
		V_{CE} = 450 V			1	mA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{EB} = 5 V			50	mA
$V_{CEO(sus)}$*	Collector-emitter Sustaining Voltage	I_C = 100 mA				
		for **BU931R/BU931RP/BU931RPFI**	400			V
		for **BU932R/BU932RP/BU932RPFI**	450			V
$V_{CE(sat)}$*	Collector-emitter Saturation Voltage	for **BU931R/BU931RP/BU931RPFI**				
		I_C = 7 A I_B = 70 mA		1.05	1.6	V
		I_C = 8 A I_B = 100 mA		1.09	1.8	V
		I_C = 10 A I_B = 250 mA		1.13	1.8	V
		for **BU932R/BU932RP/BU932RPFI**				
		I_C = 8 A I_B = 150 mA		1.09	1.8	V
$V_{BE(sat)}$*	Base-emitter Saturation Voltage	for **BU932R5BU932RP/BU932RPFI**				
		I_C = 8 A I_B = 100 mA		1.75	2.2	V
		I_C = 10 A I_B = 250 mA		1.92	2.5	V
		for **BU932R/BU932RP/BU932RPFI**				
		I_C = 8 A I_B = 150 mA		1.77	2.2	V
h_{FE}*	DC Current Gain	I_C = 5 A V_{CE} = 10 V	300			
V_F*	Diode Forward Voltage	I_F = 10 A		1.43	2.8	V
	USE TEST (see fig. 2)	V_{CC} = 24 V V_{clamp} = 400 V L = 7 mH	8			A

INDUCTIVE LOAD

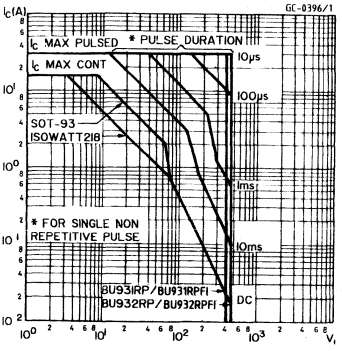
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
		V_{CC} = 12 V V_{clamp} = 300 V				
	(see fig. 3)	L = 7 mH				
t_s	Storage Time	I_C = 7 A I_B = 70 mA		15		µs
t_f	Fall Time	V_{BE} = 0 R_{BE} = 47 Ω		0.5		µs

* Pulsed : pulse duration = 300 µs, duty cycle = 1.5 %.

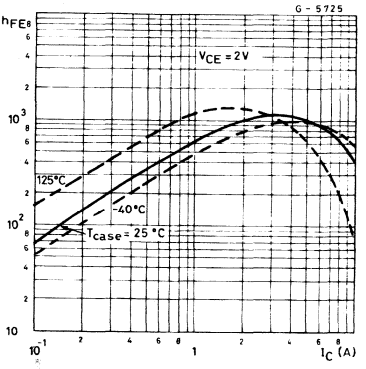
Safe Operating Areas.



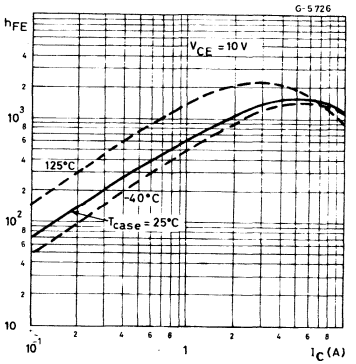
Safe Operating Areas.



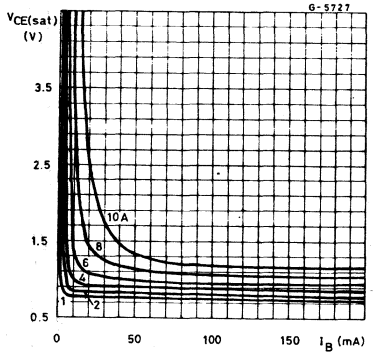
DC Current Gain.



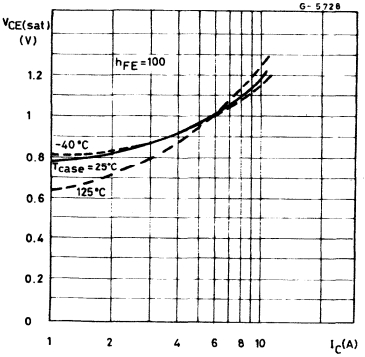
DC Current Gain.



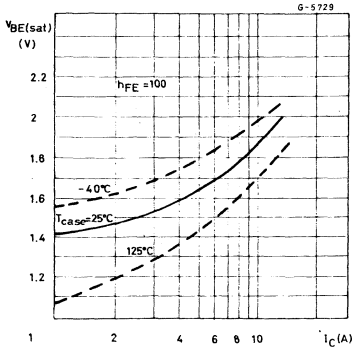
Collector-emitter Saturation Voltage.



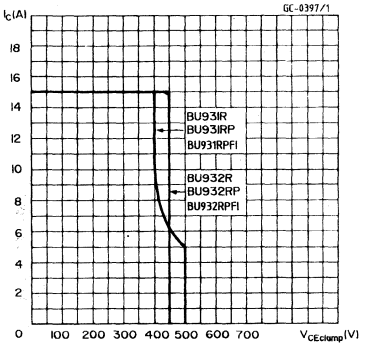
Collector-emitter Saturation Voltage.



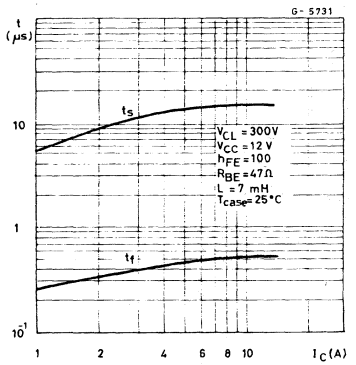
Base-emitter Saturation Voltage.



Clamped Reverse Bias Safe Operating Areas (see fig. 4).



Saturated Switching Characteristics (inductive load) (see fig. 3).



Switching Times Percentage Variation vs. T_{case} Inductive Load.

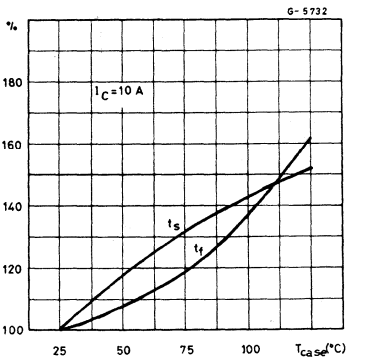


Figure 1: Functional Test Circuit.

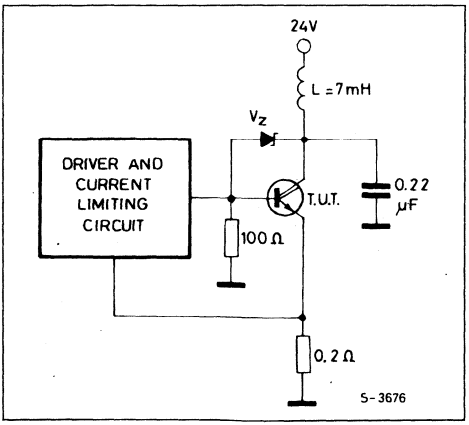


Figure 2 : Functional Test Waveforms.

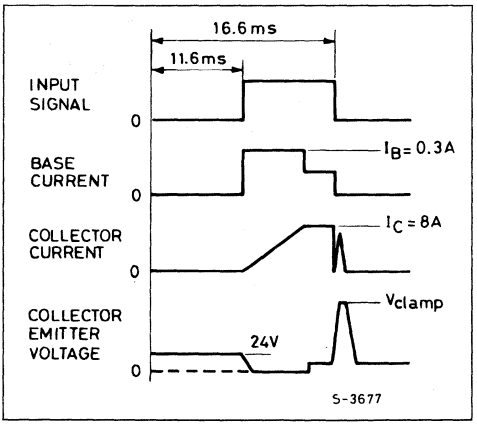


Figure 3 : Switching Times Test Circuit.

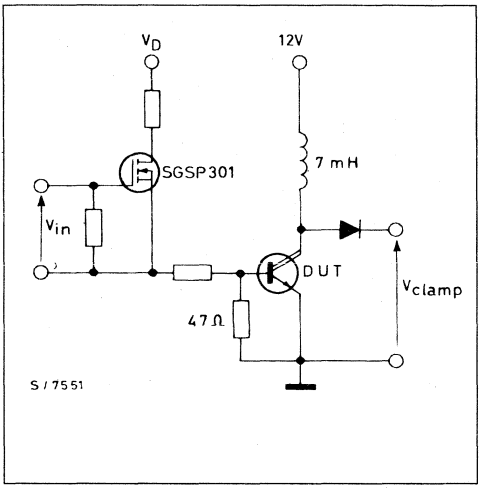
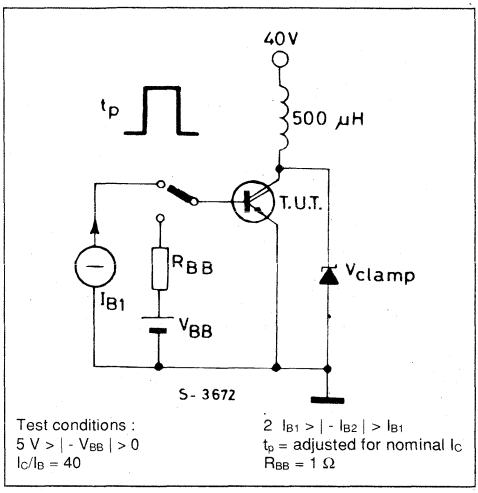


Figure 4 : Clamped $E_{s/b}$ Test Circuit.



ISOWATT 218 PACKAGE CHARACTERISTICS AND APPLICATION

ISOWATT218 is fully isolated to 4000 V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.

The structure of the case ensures optimum distances between the pins and heatsink. These distances are in agreement with VDE and UL creepage and clearance standards. The ISOWATT218 package eliminates the need for external isolation so reducing fixing hardware.

The package is supplied with leads longer than the standard TO-218 to allow easy mounting on pcbs. Accurate moulding techniques used in manufacture assures consistent heat spreader-to-heatsink capacitance.

ISOWATT218 thermal performance is better than that of the standard part, mounted with a 0.1 mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT218 packages is determined by :

$$P_D = \frac{T_j - T_c}{R_{th}}$$

THERMAL IMPEDANCE OF ISOWATT 218 PACKAGE

Fig. 5 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT218 package.

The total thermal resistance $R_{th(tot)}$ is the sum of each of these elements.

The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows :

1. for a short duration power pulse less than 1 ms ;

$$Z_{th} < R_{thJ\text{-}C}$$

2. for an intermediate power pulse of 5 ms to 50 ms ;

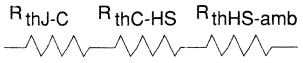
$$Z_{th} = R_{thJ\text{-}C}$$

3. for long power pulses of the order of 500 ms or greater :

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

It is often possible to discern these areas on transient thermal impedance curves.

Figure 5



SGS-THOMSON MICROELECTRONICS

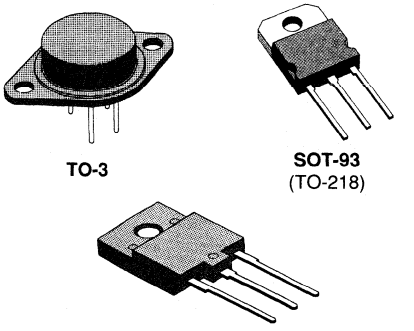
BU931Z/ZP/ZPFI

NPN POWER DARLINGTON

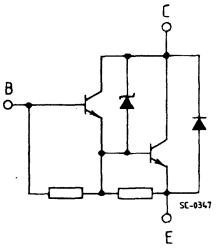
- HIGH RUGGEDNESS
- INTEGRATED HIGH VOLTAGE ZENER

AUTOMOTIVE MARKET

- APPLICATION IN HIGH PERFORMANCE ELECTRONIC CAR IGNITION



INTERNAL SCHEMATIC DIAGRAM



DESCRIPTION

The BU931Z, BU931ZP and BU931ZPFI are silicon multiepitaxial biplanar NPN transistors in monolithic darlington configuration mounted respectively in TO-3 metal case, SOT-93 plastic package and ISOWATT218 fully isolated package.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
V_{CBO}	Collector-base Voltage (I_E = 0)	350			V
V_{CER}	Collector-emitter Voltage (R_{BE} = 100 Ω)	350			V
V_{CES}	Collector-emitter Voltage (V_{BE} = 0)	350			V
V_{CEO}	Collector-emitter Voltage (I_B = 0)	350			V
V_{EBO}	Emitter-base Voltage (I_C = 0)	5			V
I_C	Collector Current	20			A
I_B	Base Current	5			A
		TO-3	SOT-93	ISOWATT218	
P_{tot}	Total Dissipation at $T_c \leq 25$ °C	175	125	60	W
T_{stg}	Storage Temperature	– 40 to 200	– 40 to 150	– 40 to 150	°C
T_j	Max. Operating Junction Temperature	200	150	150	°C

THERMAL DATA

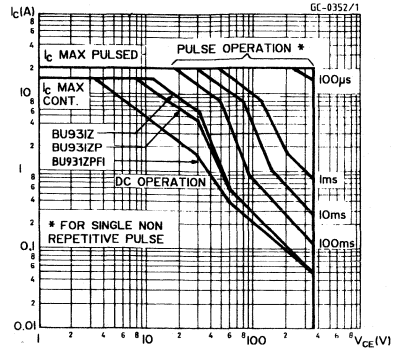
			TO-3	SOT-93	ISOWATT218	
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1	1	2.08•	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

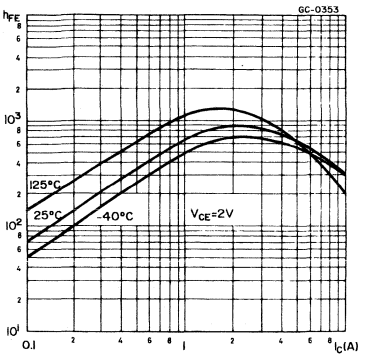
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CL}	Clamping Current	V_{CE} = 350				
		either I_B = 0			250	μA
		or V_{BE} = 0			250	μA
$I_{CE(off)}$	Collector-emitter off State Current (I_B = 0)	V_{CC} = 16 V T_j = 125 °C V_{BE} = 300 mV			0.5	mA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{EB} = 5 V			50	mA
V_{CL}	Clamping Voltage	either I_B = 0 or V_{BE} = 0				
		and I_C = 100 mA	350		500	V
		same T_j = 125 °C	350		500	V
$V_{CE(sat)}$*	Collector-emitter Saturation Voltage	I_C = 7 A I_B = 70 mA		1.25	1.6	V
		I_C = 8 A I_B = 100 mA		1.45	1.8	V
		I_C = 10 A I_B = 150 mA		1.65	2	V
		T_j = 125 °C				
		I_C = 7 A I_B = 70 mA		1.6		V
		I_C = 8 A I_B = 100 mA		1.8		V
		I_C = 10 A I_B = 150 mA		2		V
$V_{BE(sat)}$*	Base-emitter Saturation Voltage	I_C = 8 A I_B = 100 mA			2.2	V
		I_C = 10 A I_B = 250 mA			2.5	V
$V_{BE(on)}$*	Base-emitter Voltage	I_C = 5 A V_{CE} = 2 V		1.67		V
		T_j = – 40 °C			2.1	V
		T_j = 125 °C	1.1			V
		I_C = 10 A V_{CE} = 2 V		2		V
		T_j = – 40 °C			2.4	V
		T_j = 125 °C	1.4			V
V_F*	Diode Forward Voltage	I_F = 10 A			2.5	V
$E_{s/b}$	Second Breakdown Energy Unclamped	L = 10 mH I_C = 10 A		500		mJ
$I_{s/b}$	Second Breakdown Collector Current	V_{CE} = 30				
		t = 500 ms for **BU931Z**	6			A
		t = 250 ms for **BU931ZP**	4			A
		t = 250 ms for **BU931ZPFI**	1.7			A
	USE TEST (see fig. 2)	V_{CC} = 24 V L = 7 mH	8			A

* Pulsed : pulse duration = 300 μs, duty cycle = 1.5 %.

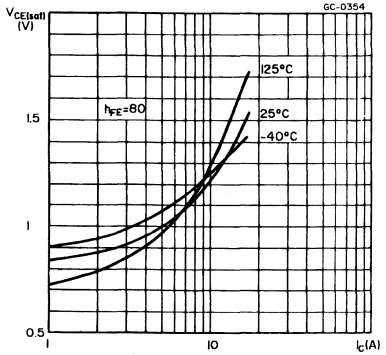
Safe Operating Areas.



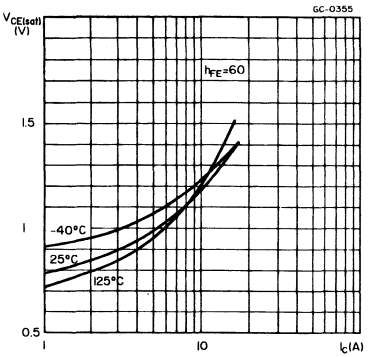
DC Current Gain.



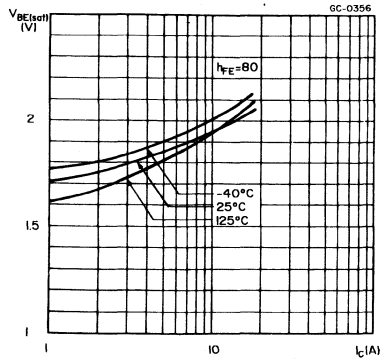
Collector-emitter Saturation Voltage.



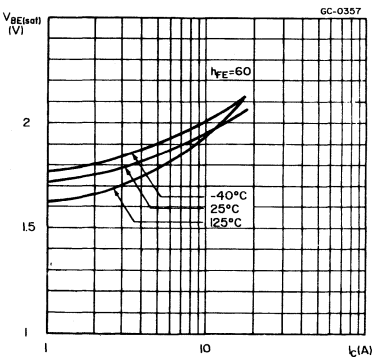
Collector-emitter Saturation Voltage.



Base-emitter Saturation Voltage.



Base-emitter Saturation Voltage.



Collector-emitter Saturation Voltage.

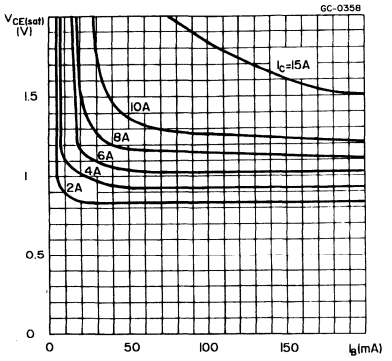


Figure 1 : Functional Test Circuit.

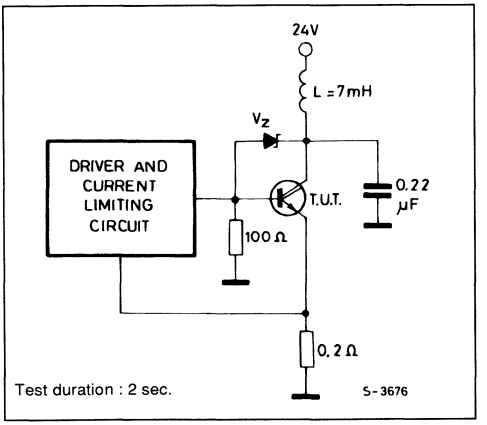
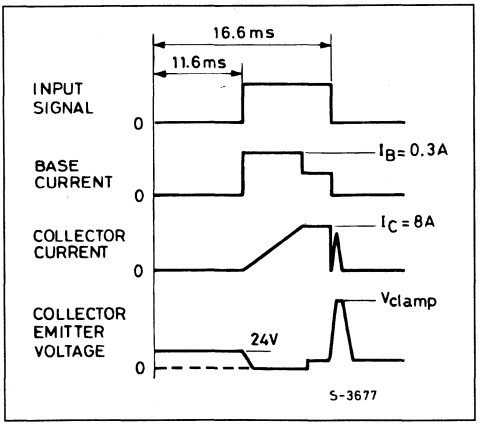


Figure 2 : Functional Test Waveforms.



ISOWATT 218 PACKAGE CHARACTERISTICS AND APPLICATION

ISOWATT218 is fully isolated to 4000 V dc. Its thermal impedance, given in the data sheet, is optimized to give efficient thermal conduction together with excellent electrical isolation.

The structure of the case ensures optimum distances between the pins and heatsink. These distances are in agreement with VDE and UL creepage and clearance standards. The ISOWATT218 package eliminates the need for external isolation so reducing fixing hardware.

The package is supplied with leads longer than the standard TO-218 to allow easy mounting on pcbs. Accurate moulding techniques used in manufacture assures consistent heat spreader-to-heatsink capacitance.

ISOWATT218 thermal performance is better than that of the standard part, mounted with a 0.1 mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT218 packages is determined by :

$$P_D = \frac{T_j - T_c}{R_{th}}$$

THERMAL IMPEDANCE OF ISOWATT 218 PACKAGE

Fig. 3 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT218 package.

The total thermal resistance $R_{th(tot)}$ is the sum of each of these elements.

The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows :

1. for a short duration power pulse less than 1 ms ;

$$Z_{th}\ R_{thJ\text{-}C}$$

2. for an intermediate power pulse of 5 ms to 50 ms :

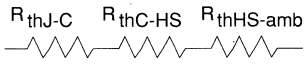
$$Z_{th} = R_{thJ\text{-}C}$$

3. for long power pulses of the order of 500 ms or greater :

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

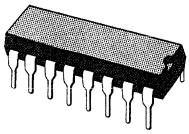
It is often possible to discern these areas on transient thermal impedance curves.

Figure 3.

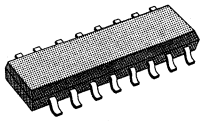


HALL–EFFECT PICKUP IGNITION CONTROLLER

- DIRECT DRIVING OF THE EXTERNAL POWER DARLINGTON
- COIL CURRENT CHARGING ANGLE (DWELL) CONTROL
- COIL CURRENT PEAK VALUE LIMITATION
- CONTINUOUS COIL CURRENT PROTECTION
- CONDUCTION AND DESATURATION TIME OUTPUT SIGNALS
- PERMANENT CONDUCTION PROTECTION RESET OUTPUT SIGNAL
- OVERVOLTAGE PROTECTION FOR EXTERNAL DARLINGTON
- LOAD DUMP PROTECTION



DIP–16



SO–16J

ORDER CODES : L482 (DIP–16)
L482D1 (SO–16J)

DESCRIPTION

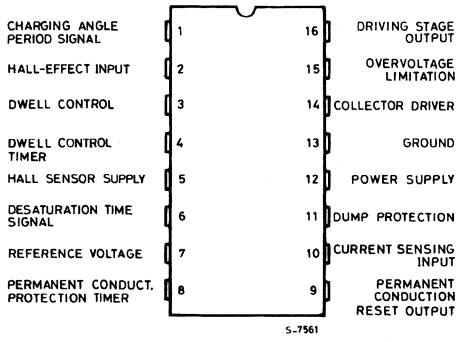
The L482 is an integrated circuit designed for use with an NPN darlington in breakerless ignition systems with hall-effect pickup sensors and high energy ignition coils.

It controls the energy stored in the ignition coil and the desaturation time of the external darlington to limit the power dissipation.

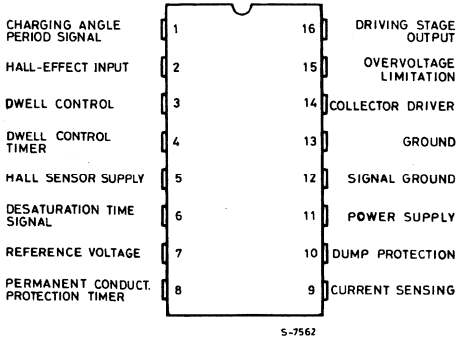
The L482 is also particularly suitable for use as ignition control and driving stage in more sophisticated car electronic systems which employ microprocessor circuits.

PIN CONNECTIONS (top views)

DIP–16



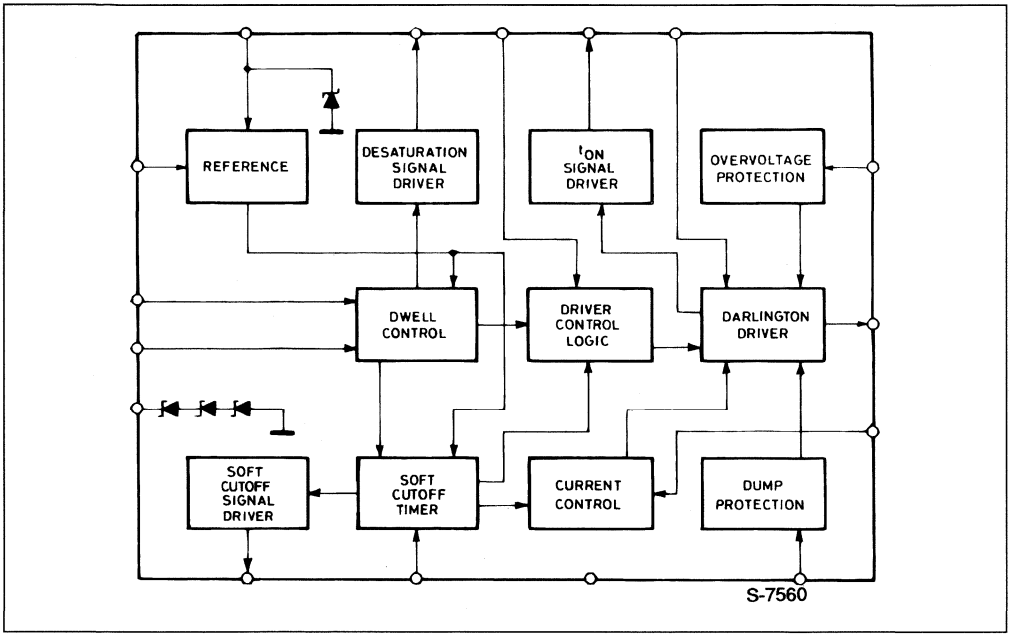
SO–16J



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_R	Reverse Battery Voltage	– 14	V
V_D	Dump Voltage (t_n = 5ms, τ_f = 100ms)	100	V
P_{tot}	Power Dissipation at T = 90°C S016 DIP	1.2 0.65	W W
T_j, T_{stg}	Junction and Storage Temperature	– 55 to 150	°C

BLOCK DIAGRAM



THERMAL DATA (DIP-16)

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	90	°C/W

THERMAL DATA (SO-16J)

$R_{th\ j\text{-}alumina}$*	Thermal Resistance Junction-alumina	Max	50	°C/W

(*) Thermal resistance junction-aluminia with the device soldered on the middle of an aluminia supporting substrate measuring 15 x 20mm ; 0.65mm thickness with infinite heatsink.

PIN FUNCTIONS (refer to fig. 3 for DIP-16 package)

N°	Name	Function
1	CONDUCTION TIME SIGNAL	A low level on this output signal indicates when the external darlington is in the ON condition i.e. when the current flows through the coil (t_{on} in fig. 1).
2	HALL-EFFECT INPUT	Hall-effect Pickup Input. A high level on this pin enables the current driving into te coil. The effective coil charge will be a function of the dwell control logic. A High to Low transition from the Hall-effect pickup is the signal for ignition actuation. The input signal, supplied by the open collector output stage of the Hall-effect sensor, has a duty cycle typically about 70%.
3	DWELL CONTROL	The average voltage on the capacitor C_2 connected between this pin and ground depends on the motor speed and the voltage supply. The comparison between V_{C2} and V_{C5} voltages determines the timing for the dwell control. The recommended value is 100nF using a 100KΩ resistor at pin 7. For the optimized operation of the device, C_2=C_5.
4	DWELL CONTROL TIMER	The capacitor C_5 connected between this pin and ground is charged when the Hall-effect output is high and is discharged at the High to Low transition of the Hall-effect signal. The recommended value is 100nF using a 100KΩ resistor at pin 7.
5	HALL SENSOR SUPPLY	This pin can be used to project the Hall-effect pickup against the voltage transients. The resistor R_a limits the currrent into the internal zener.
6	DESATURATION TIME SIGNAL	Open Collector Output Signal. This output is high when the external darlington is in desaturatiuon condition (current limitation), see t_d pulse in fig. 1.
7	REFERENCE VOLTAGE	A resistor R_{11} connected between this pin and ground sets the internal current used to drive the external capacitors of the dwell control (C_2 and C_5) and permanent conduction protection (C_1). The recommended value is 100KΩ.
8	PERMANENT CONDUCT. PROTECTION TIMER	A capacitor C_1 connected between this pin and ground determines the intervention delay of the permanent conduction protection, t_{pc} of the figure 2. With a 1μF capacitor and 100KΩ resistor R_{11} at pin 7 the typical delay is 1s.
9	PERMANENT CONDUCT. RESET OUTPUT (no available in Micropackage) (*)	A low pulse on this output detects the intervention of the permanent conduction protection, as shown in figure 2. Typically the duration of the time t_r is more than 100μs.
10	CURRENT SENSING INPUT (*)	Connection for coil current limitation. The current is measured on the sensing resistor R_s and divided on R_1/R_2 resistors. The current limitation value is given by : $I_{SENS} = \mathbf{Vsens} \frac{R_1 + R_2}{R_s \cdot R_2}$
11	DUMP PROTECTION (*)	The device is protected against the load dump. In load dump condition an internal circuit, based on a zener diode and a darlinton transistor, switches off the external darlington and short circuits the supply. By means of the external divider R8/R9 the protection threshold can be changed and is given as first approximation by : $V_{Dth} = 8.5 \cdot \frac{R_8 + R_9}{R_9} + 5 \cdot 10^{-4} \cdot R_8$ (the resistor R8 value must be higher than 4KΩ).
12	POWER SUPPLY (*)	Supply Voltage Input. A 7V (typ) zener is present at the input. The external resistor R_7 limits the current through the Zener for high supply voltages.

PIN FUNCTIONS (continued)

N°	Name	Function
13	GROUND	This pin must be connected to ground.
14	DRIVER COLLECTOR	The collector current of the internal driver which drives the external darlington is supplied through this pin. The external resistor R_{10} limits the dissipation in the I.C. The value of the resistor is a function of the darlington used and of the limiting current in the coil.
15	OVERVOLTAGE LIMITATION	The darlington is protected against overvoltage by means of an internal zener available at this pin. The external divider R_5/R_6 defines the limitation value, given as first approximation by : $V_{ovp} = (\frac{30}{R_5} + 5 \cdot 10^{-3}) \cdot R_6 + 30$
16	DRIVING STAGE OUTPUT	Current driver for the external darlington. To ensure stability and precision of T_{desat} C_3 and R_3 must be used. Recommended value for R_3 is 2KΩ in order not to change the open loop gain of the system. R_C may be added to C_3 to obtain greater flexibility in various application situations. C_3 and R_C values ranges are 1 to 100nF and 5 to 30KΩ depending on the external darlington type.

(*) These pins refer only to the DIP package type.
For the SO 16 version the permanent conduction reset output signal is not available and the pin 9 becomes the current sensing input. Pin 10 replaces the pin 11 function, pin 11 becomes the power supply input and pin 12 is used as the signal ground.

ELECTRICAL CHARACTERISTICS (V_S = 14 V, – 40°C ≤ T_j ≤ 125°C referred to application circuit of figure 3 regarding DIP-16 package version)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage		6		28	V
I_S	Supply Current	V_{12} = 4.5V			25	mA
V_Z	Zener Voltage (pin 12)	I_Z = 80mA	6.5		8.8	V
V_I	Sensor Input (pin 2) LOW Voltage HIGH		 2.5		 0.5	 V V
I_I	Sensor Input Current (pin 2)	V_I = LOW V_S = 6 to 16V	–12		–1	mA
V_{Hz}	Hall-cell Supply Zener Voltage (pin 5)	I_{Hz} = 10mA	19	22	25	V
I_{HZ}	Hall-cell Supply Zener Current (pin 5)	t = 10ms T_{AMB} = 25°C	100			mA
$V_{CE\ sat}$ (V_{14}–V_{16})	Series Darlington Driver Sat. Voltage	I_o = 70mA I_o = 150mA		 0.4	0.6 1.0	V V
V_{SENS}	Current Limit. Sensing Voltage (pin 10)	V_S = 6 to 16V	200		330	mV
I_{3D} I_{3C} I_{3C}/I_{3D}	C2 Discharge Current C2 Charge Current	V_S = 6 to 16V (*) Note 1	0.2 7 6		3.4 20 35	µA µA
V_{OVZ}	External Darlington Overvoltage Protection Zener Voltage	I_{OVZ} = 5mA to 15mA T_{AMB} = 25°C	25	30	35	V
V_7	Reference Voltage		2.5		3.5	V

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PC}	Permanent Conduction Protection Time (pin 8) (see fig. 2)	V_I = H C_I = 1µF	0.5	1	2	s
V_1	Charging Angle Output Voltage LOW HIGH	 I_{SINK} = 0 I_{SINK} = 1mA I_{SOURCE} = 1.5mA I_{SOURCE} = 2.5mA	 3 5		 0.5 1.2 	 V V V V
V_6	Desat. Time Output Low Voltage	$I_{6\ (sink)}$ = 0.5mA			0.7	V
I_{6L}	Desat. Time Leakage Current (pin 6)	V_6 = 5V			10	µA
I_{9L}	Permanent Conduction Reset Leakage Current (pin 9)	V_9 = 5V			10.5	µA
V_{DZ}	Zener Dump (pin 11)	I_{DZ} = 2mA	7.5		9.5	V

(*) Note 1 : TD/T is given by the formula :

$$t_d / T = \frac{1}{1 + I_{3C}/I_{3D}} \quad \text{see fig. 1}$$

APPLICATION INFORMATION

Figure 1 : Main Waveforms.

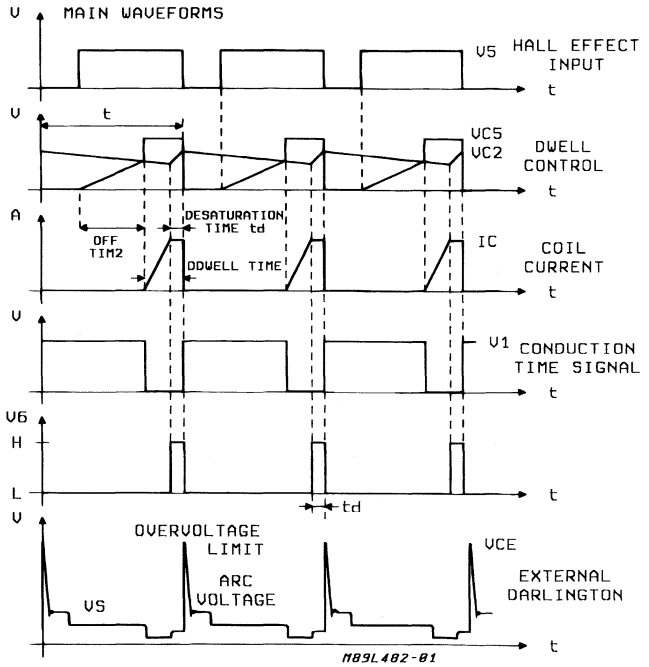


Figure 2 : Low Frequency Condition and Permanent Conduction Protection.

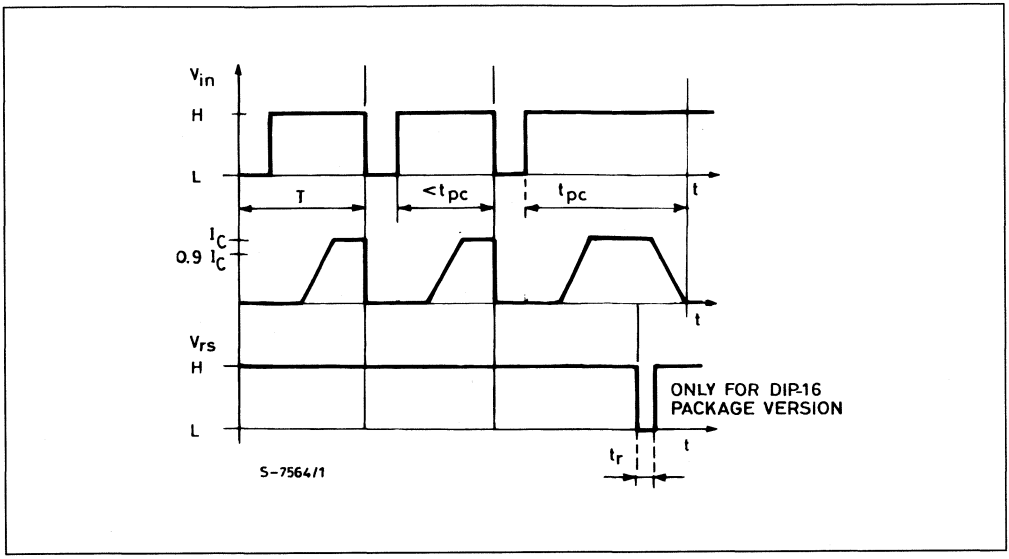


Figure 3 : Application circuit (DIP–16).

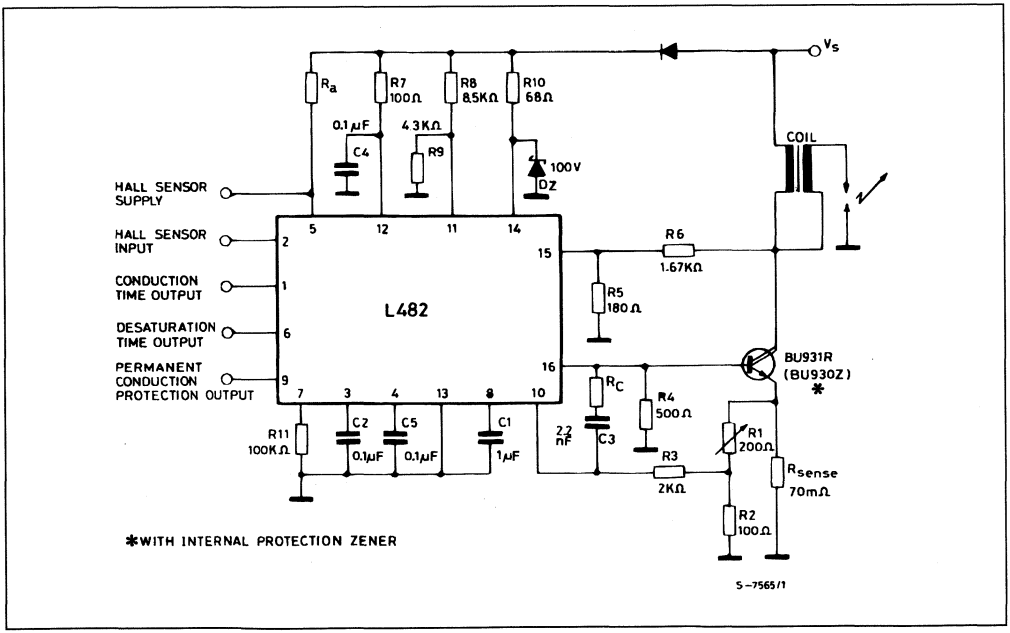
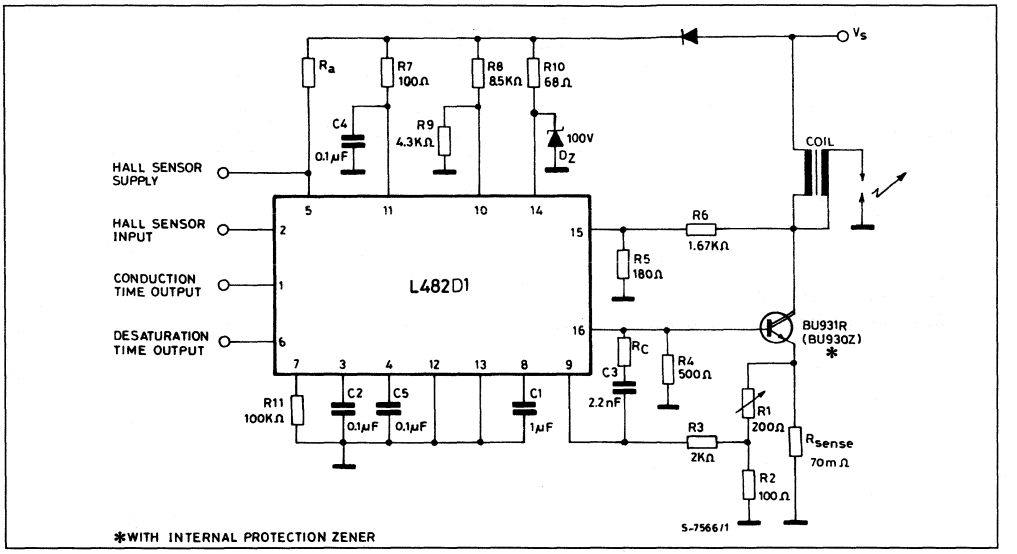


Figure 4 : Application Circuit (SO–16).



CIRCUIT OPERATION

The L482 control the conduction time (dwell) and the peak value of the primary current in the coil over the full range of operating conditions.

The coil current is limited to a predetermined level by means of a negative feedback circuit including a current sensing resistor, a comparator, the driver stage and the power switch.

The dwell control circuit maintains the output stage in its active region during current limitation. The time the output stage is in the active region (desaturation time) is sufficient to compensate for possible variations in the nergy stored due to the acceleration of the motor ; moreover this time is limited to avoid excessive power dissipation.

CONTROL OF THE DWELL ANGLE (fig. 1 and 4)

The dwell angle control circuit calculates the conduction time D for the output transistor in relation to the speed of rotation, to the supply voltage and to the characteristic of the coil.

On the negative edge of the Hall-effect input signal the capacitor C_2 begins discharging with a constant current I_{3D}. When the set peak value of the coil current is reached, this capacitor charges with a constant current $I_{3C} = 13.3 \times I_{3D}$ and the coil current is kept constant by desaturating the driver stage and the external darlington.

The capacitor C_5 starts charging on the positive edge of the Hall-effect input signal with a constant current I_{4C}.

The dwell angle, and consequently the starting point of the coil current production, is decided by the comparison between V_{C2} and V_{C5}. A positive hysteresis is added to the dwell comparator to avoid spurious effects and C_5 is rapidly discharged on the negative edge of Hall-effects input signal.

In this way the average voltage on C_2 increases if the motor speed decreases and viceversa in order to maintain constant the ratio $\frac{td}{T}$ at any motor speed.

td is kept constant (and not d = cost) to control the power dissipation and to have sufficient time to avoid low energy sparks during acceleration.

The charging time D – td depends on the coil and the voltage supply.

DESATURATION TIMES IN STATIC CONDITIONS.In static conditions, if $C_2 = C_5$ as recommended and if the values of the application circuit of fig. 3, 4 are used.

$$\frac{td}{T} = \frac{1}{1 + I_{3C}/I_{3D}}$$

DESATURATION TIMES IN LOW AND HIGH FREQUENCY OPERATION. Due to the upper limit of the voltage range of pin 3, if the components of fig. 3, 4 are used, below 10Hz (300RPM for a 4 cylinder engine) the OFF time reaches its maximum value (about 50ms) and then the circuit gradually loses the control of the dwell angle because D = T – 50ms

Over 200Hz (6000RPM for a 4 cylinder engine) the available time for the conduction is less than 3.5ms.

If the used coil is 6mH, 6A, the OFF time is reduced to zero and the circuit loses the dwell angle control.

TRANSIENT RESPONSE. The ignition system must deliver constant energy even during the condition of acceleration and deceleration of the motor below 80Hz/s. These conditions can be simulated by means of a signal generator with a linearly modulated frequency between 1Hz and 200Hz (this corresponds to a change between 30 and 6000RPM for a 4 cylinders engine.

CURRENT LIMIT. The current in the coil is monitored by measuring the I_{sense} current flowing in the sensing resistor R_S on the emitter of the external darlington. I_{sense} is given by :

$$I_{sense} = I_{coil} + I_{16}$$

When the voltage drop across R_S reaches the internal comparator threshold value the feedback loop is activated and I_{sense} kept constant (fig. 1) forcing the external darlington in the active region. In this condition :

$$I_{sense} = I_{coil}$$

When a precise peak coil current is required R_5 must be trimmed or an auxiliary resistor divider (R_1, R_2) added :

$$Icpeak\ (A) = \frac{V_{SENS}}{R_S} \left(\frac{R_1}{R_2} + 1 \right)$$

PROTECTION CIRCUIT

PERMANENT CONDUCTION PROTECTION

The battery voltage is applied to ignition module by means of the ignition key. In these conditions, with the motor stopped, it is necessary that there is no permanent conduction in the ignition coil irrespective of the polarity of the input signal.

The L482 incorporates a timing circuit to implement this protection ; the duration of the intervention is set by means of a capacitor C_1 at pin 8 = 1μF, and R_{11} = 100kΩ, when the input signal is high for more than 1 s, the coil current gradually decreases down to zero to avoid spurious sparks (see fig. 2).

This timing allows normal operation of the module above 30RPM.

DARLINGTON OVERVOLTAGE LIMITATION

The darlington is protected against overvoltage by means of an external divider R_5/R_6 (pin 15) and an internal zener. This zener drives the external darlington in order to limit the collector voltage.

REVERSE BATTERY PRTOTECTION. Due to the presence of external impedance at pin 5, 10, 11, 14, 15, L482 is protected against reverse battery voltage.

DUMP PROTECTION.

The load dump protection withstands up to 100V with a decay time ≤ 300ms. The intervention threshold for load dump is fixed by means of an external divider connected to pin 11 (DIP-16 package version) or to pin 10 using a Micropackage type.

NEGATIVE SPIKE PROTECTION.If correct operation is requested also during short negative spikes, the diode DS and capacitor C_S must be used.

USE OF THE IC ELECTRONIC ADVANCE SYSTEM

When the device is digitally controlled the control unit transmits a suitable input signal to the power module, receiving in turn information that allows the control of the dwell and the on time of the final transistor.

For this reason L482 provides the following outputs :

- a time signal equal to the time in which the final Darlington is in the active region i.e. when the coil current is limited (V_{ds}) as shown in figure 1. This signal must be TTL compatible.
- a TTL compatible output from the timing circuit (V_{rs} in figure 2). This pulse, available only using the DIP-16 package version is present after the protection against cranking transients.
- a time signal equal to the time in which the final Darlington, is in "on" condition (V_{on}) i.e. when the current flows through the coil, see fig. 1.

OTHER APPLICATION INFORMATION

If the supply voltage is disconnected - or the battery wire is broken - while the current is flowing through the coil, the external diode D_1 keeps the coil current from recirculating into the device : in this way both device and darlington are protected.

The zener diode D_Z, connected between pin 14 and GND, allows to withstand positive spikes up to 200V.

The device - used in the recommended application circuit - satisfies the ISO/DP 7637/1 overvoltage standard.

MAGNETIC PICKUP IGNITION CONTROLLER

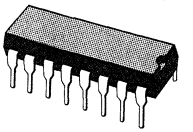
- DIRECT DRIVING OF THE EXTERNAL DARLINGTON
- OPERATES WITH A WIDE RANGE OF MAGNETIC PICKUP TYPES
- CHARGING ANGLE (DWELL) CONTROL
- COIL CURRENT PEAK LIMITATION
- CONTINUOUS COIL CURRENT PROTECTION
- TACHOMETER SIGNAL OUTPUT
- EXTERNAL DARLINGTON OVERVOLTAGE PROTECTION
- LOAD DUMP AND REVERSE BATTERY PROTECTION
- POSSIBILITY OF SPARK POINT DELAYING (ANTI KNOCK SYSTEM)

DESCRIPTION

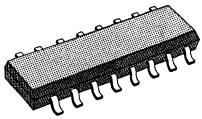
The L484 is an integrated circuit designed for use with an NPN darlington in breakerless ignition systems with magnetic pickup sensors and high energy ignition coils.

A key feature of the L484 is flexibility. It can be used with a wide variety of magnetic sensors thanks to the special design which has two input pins from the pickup ; the first is the zero crossing detector for the ignition command and the second pin is used to calculate the dwell time. Moreover another pin is used to adapt the L484 to various pickup types.

Other features of the device include darlington overvoltage protection, dump protection, a supply voltage range of 6-28 V.



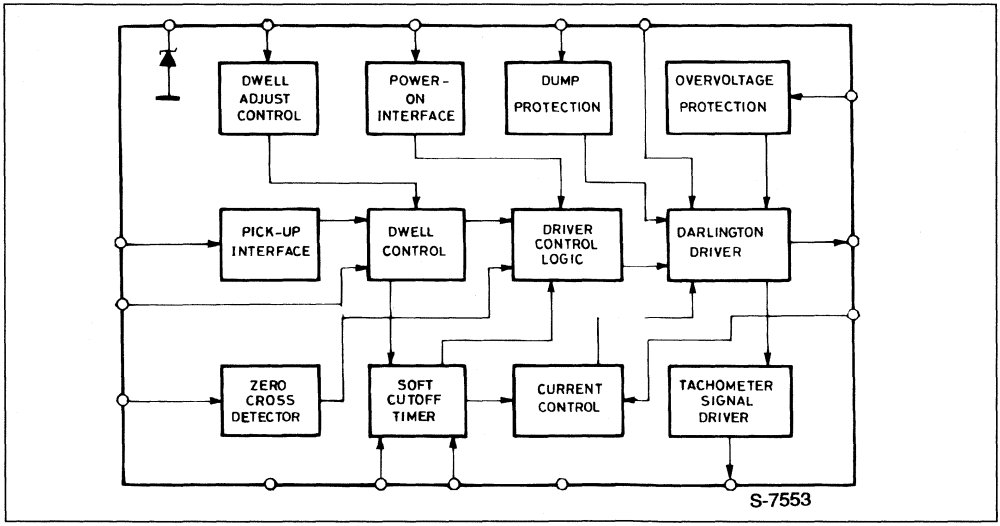
DIP–16



SO–16J

ORDER CODES : L484 (DIP–16)
L484D1 (SO–16J)

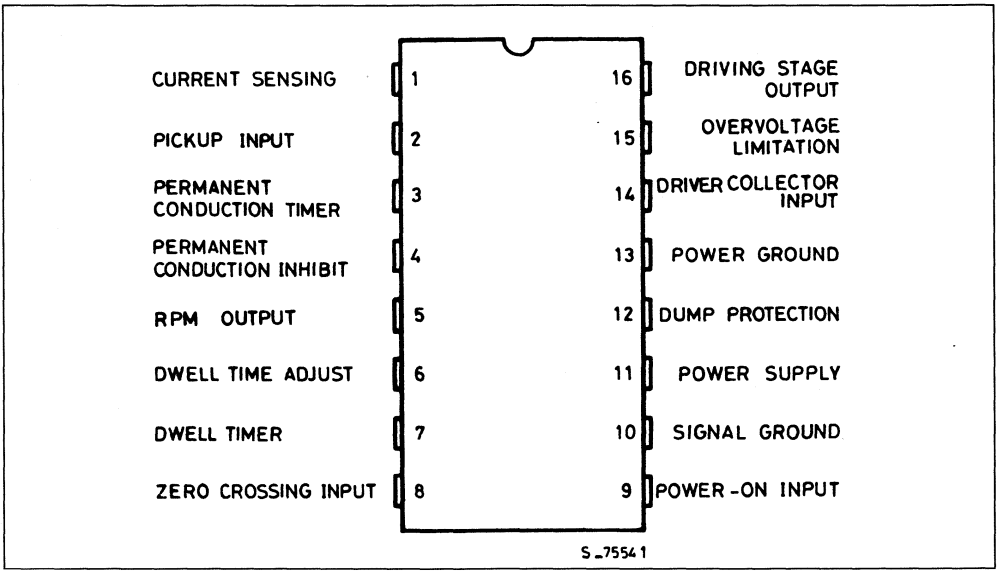
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_R	Reverse Battery Voltage	– 14	V
V_D	Dump Voltage	100	V
P_{tot}	Power Dissipation at T_{amb} = 90°C	0.75	W
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

PIN CONNECTION



THERMAL DATA (DIP-16)

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

THERMAL DATA (SO-16J)

$R_{th\ j\text{-}al}$	Thermal Resistance Junction-alumina	Max	50	°C/W

PIN FUNCTIONS (refer to fig. 2)

N°	Name	Function
1	CURRENT SENSING INPUT	Connection for Coil Current Limitation. The current is measured on the sense resistor R_{SENS} and divided on R1/R2. The current limitation value is given by : $I_{SENS} = \frac{R1 + R2}{R_{SENS}\ R2}$
2	PICKUP INPUT	Magnetic Pickup Signal Input. This pin sets the dwell time, i.e. the max negative pickup voltage value starting from which the device can drive the current into the coil. The real dwell time will be a function of the dwell control logic. Increasing the resistor R11 the maximum conduction time increases. The max input current foreseen is 2mA.
3	PERMANENT CONDUCT. PROTECTION TIMER	A capacitor C1 connected between this pin and ground sets the delay of the permanent conduction protection in the coil current. Using a 50nF capacitor the typical desaturation time delay for the protection is 75ms.
4	PERMANENT CONDUCT. PROTECTION INHIBIT	A low level on this input (max 0.7V) disables the protection, irrespective of the state of pin 3. If the protection is used this pin must be left open.
5	RPM OUTPUT	Open collector output signal which is at a low level when the final darlington is in ON status. The current is internally limited at 10mA.
6	DWELL TIME ADJUST	At high motor rotation speeds, i.e. when the peak value of the magnetic pick-up signal exceedes 6V using R12 = 100KΩ, this pin may be used to vary the dwell ratio. Adding a resistor in series R_a between this pin and pin 11 the desaturation time is reduced. It is therefore possible to use this pin to adapt the L484 to various pickup types. The maximum value of the resistor R_a is 200KΩ.
7	DWELL CONTROL TIMER	A capacitor C2 connected between this pin and ground sets the timing for the dwell control. The recommended value is 100nF. The resistors R_b/R_c provide an hysteresis to confirm ON state and avoid spurious sparks.
8	ZERO CROSSING INPUT	Zero cross detector input of the magnetic pickup signal for the ignition actuation. At high motor rotation speeds, the external resistor R12 may be used to vary the desaturation time ratio, to adapt the L484 to various signal waveforms of time magnetic pick-up. Reducing the resistor value the dwell time increases. Typically the range of values for resistor R12 is from 50KΩ to 150KΩ.
9	POWER-ON INPUT	A low level on this pin forces the external darlington into conduction particularly useful in anti knock system. This function is particularly useful in antiknock system because provides a spark time delay. Anyway the current limitation, the permanent conduction protection and the dump protection are operating even when pin 9 is at a low level. If this function is not used it must be left open.
10	SIGNAL GROUND	This pin must be connected to ground.
11	POWER SUPPLY	Supply Voltage Input. A 7V (typ) zener is present at the input. The external resistor R9 limits the current through the zener for higher supply voltages.

* this function is particularly useful in antiknock systeme because provides a spark time delay. anyway the current limitation, the pemanent con duction protection and the dump protection are operating even when pin 9 is at a low level.

PIN FUNCTIONS (continued)

N°	Name	Function
12	DUMP PROTECTION	The device is protected against the load dump. In load dump condition an internal circuit, based on a zener diode and a darlington transistor, switches off the external darlington and short circuits the supply. By means of the external divider R8/R9 the protection threshold can be changed and is given as first approximation by : $V_{Dth} = 8.5 \left(\frac{R8 + R9}{R9} \right) + 5 \cdot 10^{-4} R8$ (the resistor R9 value must be higher than 4KΩ).
13	POWER GROUND	This pin must be connected to ground.
14	DRIVER COLLECTOR INPUT	The collector current for the internal driver which drives the external darlington is supplied through this pin. The external resistor R10 limits the dissipation in the IC. The value this resistor depends on the darlington used and on the limiting current in the coil.
15	OVERVOLTAGE LIMITATION	The external darlington is protected against overvoltage by means of an internal zener available at this pin. The external divider R5/R6 defines the limitation value, typically given by : $V_{ovp} = \left(\frac{30}{R5} + 5 \cdot 10^{-3} \right) \cdot R6 + 30$
16	DRIVING STAGE OUTPUT	Current Driver for the External Darlington. To ensure stability on the current limitation loop a capacitor C3 (typically 2.2nF, this value depending on the darlington used) must be connected between this pin and the current sensing input (pin 1).

ELECTRICAL CHARACTERISTICS (V_S = 14.4V ; T_J = - 40 to 125°C unless otherwise specified ; referred to the test circuit)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage		6		28	V
V_{IS}	Input Stage Voltage (pin 2 with 10KΩ resistor)		160	200	240	mV
V_{TH}	On Pick-up Thresh. Voltage at LOW RPM (pin 2)		V_{IS}–30		V_{IS}+30	mV
V_{SENS}	Current Limitation Sensing Voltage (pin 1)	V_S = 6 to 16V	200		320	mV
V_{ZC}	Zero Crossing Thresh. Voltage (pin 8)		3	20	60	mV
V_H	Hysteresis Voltage (pin 8)		100		200	mV
I_{7C}	$C_{D\ WELL}$ Charge Current	at LOW RPM	0.7		3	µA
I_{7D}	$C_{D\ WELL}$ Discharge Current	$V_{pick\text{-}up}$ = 0.5V ; or pin 6 not connected	7		30	µA
I_{7D}/I_{7C}		(*) Note 1	7		15	
I_{7C}	$C_{D\ WELL}$ Charge Current	at HIGH RPM	8		33	µA
I_{7D}	$C_{D\ WELL}$ Discharge Current	$V_{pick\text{-}up}$ = 9V	13		44	µA
I_{7D}/I_{7C}		(**) Note 2	0.7		3.2	
V_{pin3}	Threshold Voltage	T_{amb} = 25°C	1		3	V
I_3	Output Current	(***) Note 3			3	µA
V_{Cp}	Continuous Coil Current Protection Inhibit LOW Voltage (pin 4).		0		0.7	V
V_{CEsat}	Series Darlington Driver Saturation Voltage ($V_{pin\ 14\ -\ 16}$)	I_{pin14} = 150mA		0.4	1	V
		I_{pin14} = 50mA			0.6	V
V_Z	Zener Volt. Pin 11	I_{pin11} = 140mA	6.5		8.8	V
V_{OVZ}	External Darlington Overvoltage Protection Zener Voltage	T_{amb} = 25°C ; I_{pin15} = 5 to 15mA	25		35	V
I_{09}	Pin 9 Output Current in Low Status	V_9 = 0V			3	mA
V_{CH}	Tachometer Signal Output LOW Voltage. (pin 5)	ON Condition I_{sink} = 0.5mA			0.7	V
I_{CH}	Output Leakage (pin 5)	OFF Condition V_{pin5} = 5V			10	µA

DUMP PROTECTION

Symbol	Paramater	Test Conditions	Min.	Typ.	Max.	Unit
V_{DZ}	Zener Dump (pin 12)	I_{pin12} = 2mA	7.5		9.5	V

(*) Note 1 : TD/T is given by the formula :

$$\frac{TD}{T} = \frac{1}{1 + I7D/I7C}$$

(**) Note 2 :

$$\frac{TD}{T} = \frac{K}{1 + I7D/I7C}$$

K value depends on the pick-up used in the application ; typically K = 0.1
(***) Note 3 : the permanent conduction protection is guaranteed over the full temperature range

CIRCUIT OPERATION

The L484 controls the charging angle (dwell) and the peak value of the primary current in the coil over the full range of operating conditions.

The coil current is limited to a predetermined level by means of a negative feedback circuit including a current sensing resistor, a comparator, the driver stage and the power switch.

The dwell control circuit keeps the output stage in its active region during current limitation. The time the output stage is operating in the active region (desaturation time), is sufficient to compensate for possible variation in the energy stored due to the acceleration of the motor ; moreover this time is limited to avoid excessive power dissipation.

MAGNETIC PICK–UP CHARACTERISTICS

The typical magnetic pickup waveforms are shown in fig. 1, the amplitude of the signal being a function of the frequency. However on the market there are many types of magnetic pickup, of which the waveforms may differ very much. Adjusting the value of the resistor R_{11} on pin 2 and/or adding a resistor R_a between the pin 6 (dwell adjust) and pin 11, as shown in the application circuit, it is possible to adapt the L484 to a wide range of magnetic pickup waveforms.

Particularly by means of the resistor R_{11} on pin 2 it is possible to define the maximum advance of the conduction start into the coil . This is very useful at high pick–up frequency.

CONTROL OF THE DWELL ANGLE

The dwell angle control circuit defines the conduction time of the output darlington, versus the speed of rotation, the supply voltage and the characteristics of the coil.

In each cycle the time the transistor operates in the active region is compared with a reference time and the error signal amplified to advance or delay the conduction in the next cycle. To limit the power dissipation the desaturation time is typically fixed to 10% of the period T.

At very low frequencies the ON thershold is fixed at 200mV of the input signal and the desaturation time is mainly determined by the peak waveform. This positive threshold also prevents permanent conduction when the motor is stopped. When the input frequency increases the dwell control gradually sets the desaturation time to 10% of the period. At higher frequencies the ON threshold becomes negative to permit a conduction angle of more than 50% always keeping desaturation time to 10% of the period.

CURRENT LIMITING

The current in the coil is measured by means of a voltage drop across a suitable resistor in the emitter lead of the power transistor. When the threshold voltage (260mV typ) is reached, the coil current is kept constant via a feedback loop.

DARLINGTON OVERVOLTAGE LIMITATION

The darlington is protected against overvoltage by means of an external divider R_5/R_6 (pin 15) and an internal zener. This zener drives the external darlington in order to limit the collector voltage.

CHARGING ANGLE SIGNAL OUTPUT

This signal is intended for tachometer applications (pin 5). It consists of an open collector stage with current internally limited at 10mA

"POWER ON" SIGNAL INPUT

In the low status this input forces the external darlington into conduction (pin 9). This control input can be used together with the conduction time information coming from pin 5 to bypass the normal dwell time calculation. When an external logic control is used to recognize particular engine condition (as in anti Knock system).

PROTECTION CIRCUITS

PERMANENT CONDUCTION PROTECTION

This function is intended to prevent continuous current conduction in the final stage when the magnetic pickup is open or intermittent. The duration of the intervention is set by means of a capacitor 1 at pin 3. Grounding pins 3 or 4, this protection is eliminated. The inhibit function at pin 4 is particularly useful when an external logic control is used to disable the permanent conduction protection.

REVERSE BATTERY AND DUMP PROTECTION

Due to the external resistors R_6, R_7, R_8, R_{10} the device is protected against reverse battery. The load dump protection withstands up to 100V with a decay time ≤ 300ms. The intervention threshold for load dump is fixed by means of an external divider connected to pin 11.

OTHER APPLICATION INFORMATION

If the supply is voltage disconnected - or the battery wire is broken - while the current is flowing through the coil, the external diode D_1 keeps the coil current from recirculating into the device : in this way both device and darlington are protected.

The zener diode Dz, connected between pin 14 and GND, allows to withstand positive spikes up to 200V.

The device - used in the recommended application circuit - satisfies the ISO/DP 7637/1 overvoltage standard.

Figure 1 : Typical Magnetic Pick–up Waveform and L484 Response at low and high fequency.

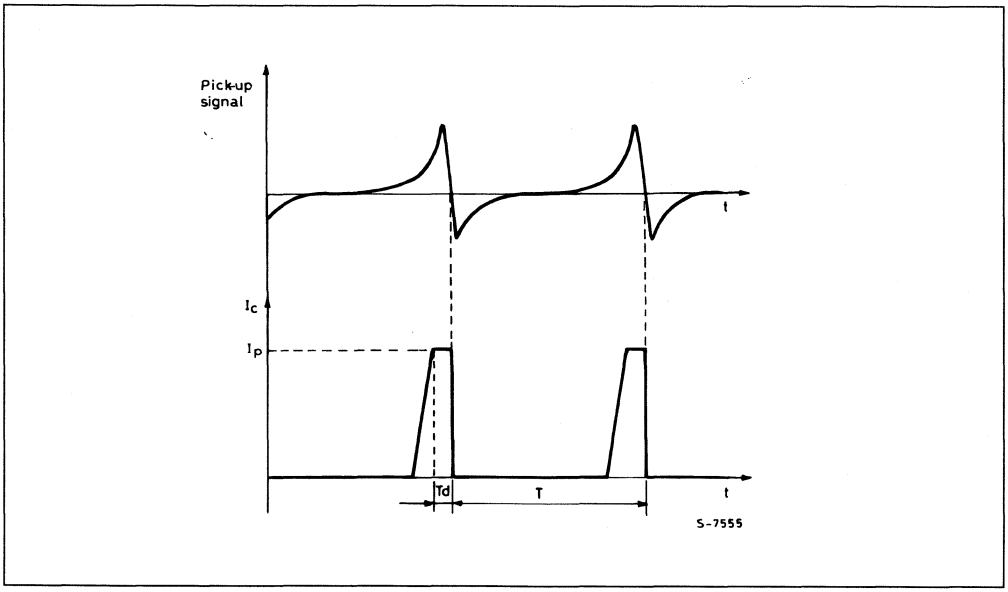


Figure 1 : Typical Magnetic Pick-up Waveform and L484 Response at Low and High Frequency (continued).

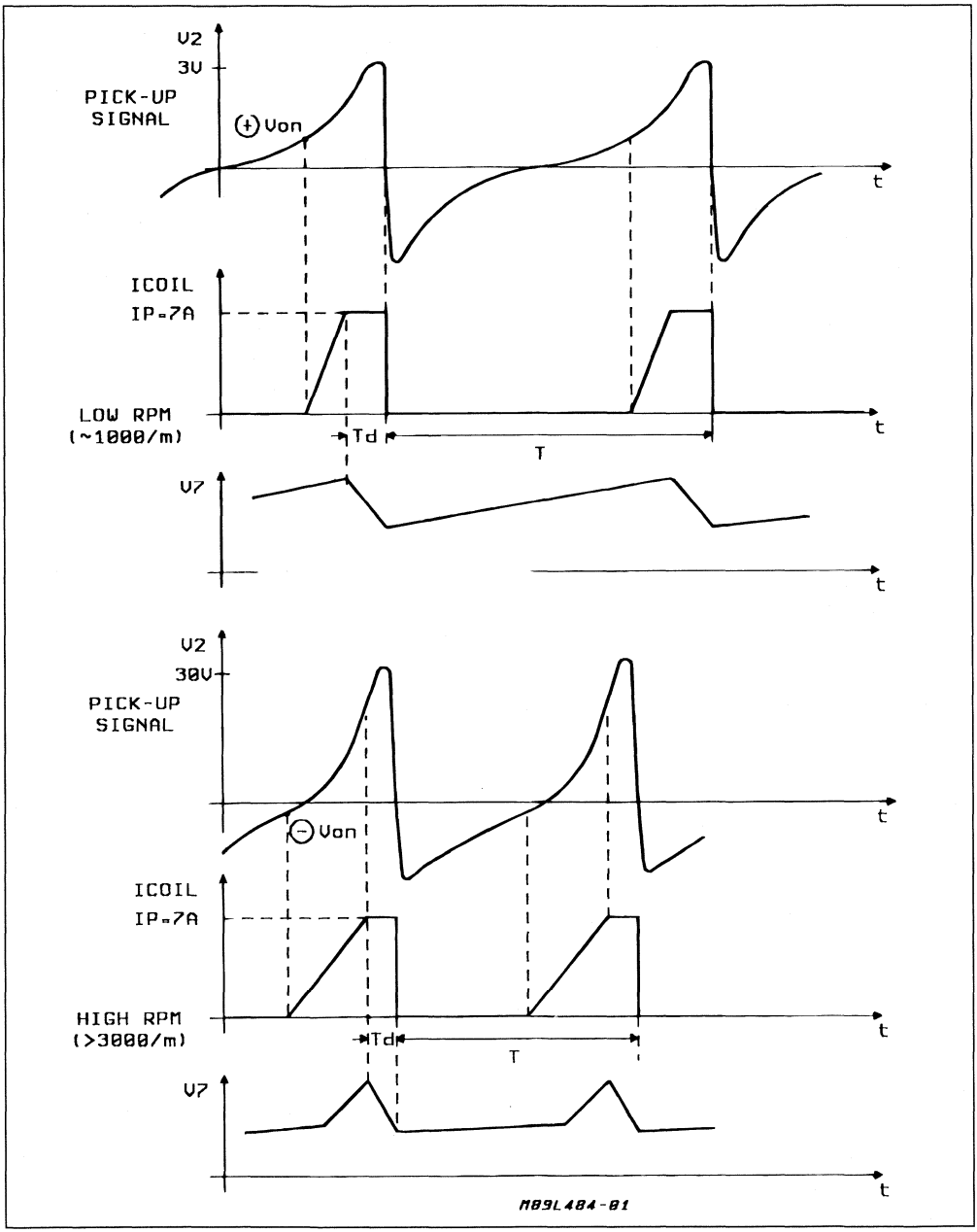
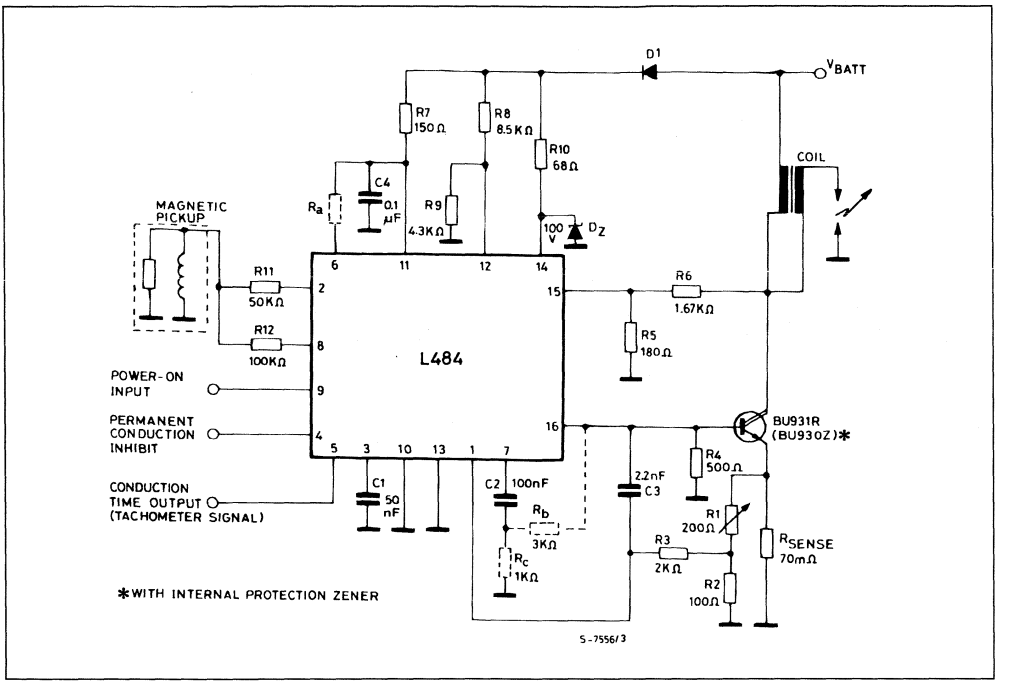


Figure 2 : Application Circuit.



HALL EFFECT PICKUP IGNITION CONTROLLER

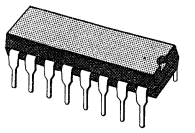
- DIRECT DRIVING OF THE EXTERNAL POWER DARLINGTON
- COIL CURRENT CHARGING ANGLE (dwell) CONTROL
- PROGRAMMABLE COIL CURRENT PEAK LIMITATION
- PROGRAMMABLE DWELL RECOVERY TIME WHEN 94% NOMINAL CURRENT NOT REACHED
- RPM OUTPUT
- PERMANENT CONDUCTION PROTECTION
- OVERVOLTAGE PROTECTION FOR EXTERNAL DARLINGTON
- INTERNAL SUPPLY ZENER
- REVERSE BATTERY PROTECTION

DESCRIPTION

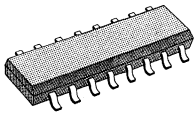
The L497 is an integrated electronic ignition controller for breakerless ignition systems using Hall effect sensors.

The device drives an NPN external darlington to control the coil current providing the required stored energy with low dissipation.

A special feature of the L497 is the programmable time for the recovery of the correct dwell ratio t_d/T when the coil peak current fails to reach 94% of the nominal value. In this way only one spark may have an energy less than 94% of the nominal one during fast acceleration or cold starts.



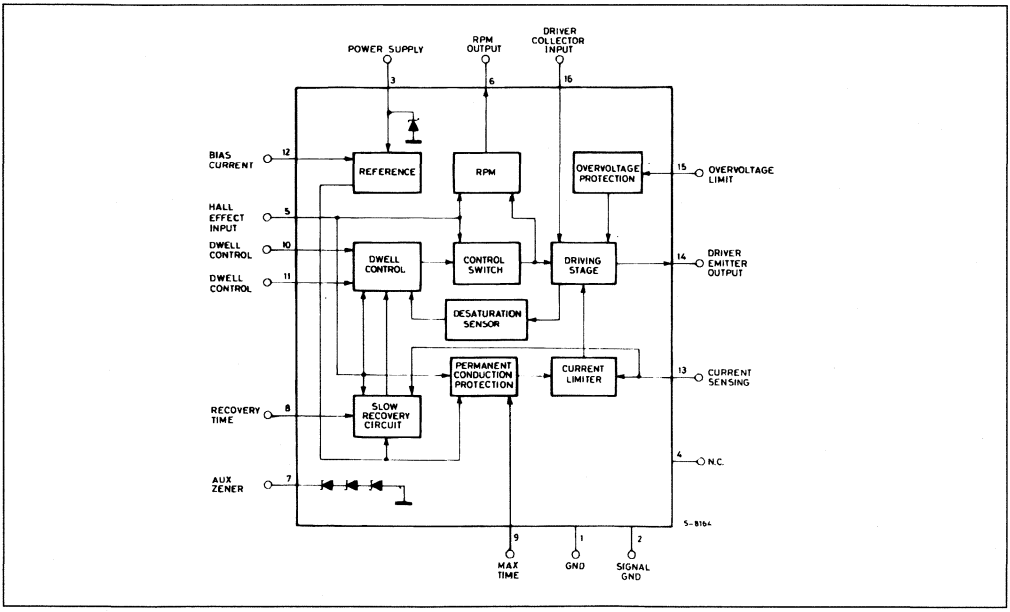
DIP-16



SO-16J

ORDER CODES : L497B (DIP-16)
L497D1 (SO-16)

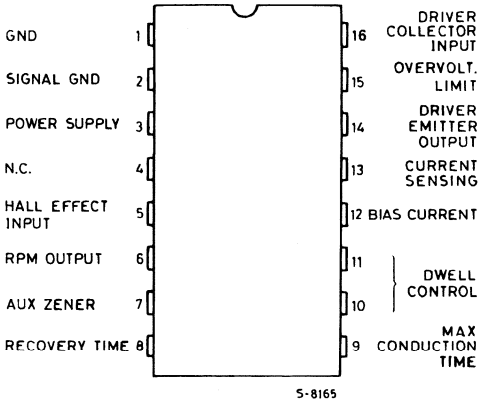
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_3	D.C. Supply current Transient Supply Current (t_f fall time constant = 100ms)	200 800	mA mA
V_3	Supply Voltage	Int. Limited to V_{z3}	
V_6	RPM Voltage	28	V
I_{16}	D.C. Driver Collector Current Pulse " " ($t \leq 3ms$)	300 600	mA mA
V_{16}	Driver Collector Voltage	28	V
V_{15}	D.C. Overvoltage Zener Current Pulse " "$t_{fall} = 300\mu s$, t_{reo} Repetition Time $\geq$ 3ms	 15 35	 mA mA
V_R	Reverse Battery Voltage if Application Circuit of Fig. 4 is used	−16	V
T_j, T_{stg}	Junction and Storage Temperature Range	−55 to 150	°C
P_{tot}	Power Dissipation at $T_{aluminia}$ = 90°C for SO-16 T_{amb} = 90°C for DIP-16	 1.2 0.65	 W W

PIN CONNECTION (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient for DIP-16	Max	90	°C/W
$R_{th\ j\text{-}alumin}$ (*)	Thermal Resistance Junction-alumina for SO-16J	Max	50	°C/W

(*) Thermal resistance junction-aluminia with the device soldered on the middle of an aluminia supporting substrate mesuring 15 x 20 ; 0.65mm thickness.

PIN FUNCTIONS (refer to fig. 4)

N°	Name	Function
1	GND	This pin must be connected to ground.
2	SIGNAL GND	This pin must be connected to ground.
3	POWER SUPPLY	Supply Voltage Input. An internal 7.5V (typ. value) zener limits the voltage at this pin. The external resistor R_5 limits the current through the zener for high supply voltages.
4	N.C.	This pin must be connected to ground or left open.
5	HALL-EFFECT INPUT	Hall-effect Pickup Signal Input. This input is the dwell control circuit output in order to enable the current driving into the coil. The spark occurs at the high-to-low transition of the hall-effect pickup signal. Furthermore this input signal enables the slow recovery and permanent conduction protection circuits. The input signal, supplied by the open collector output stage of the Hall effect sensor, has a duty cycle typically about 70%. V_5 is internally clamped to V_3 and ground by diodes.
6	RPM OUTPUT	Open collector output which is at a low level when current flows in the ignition coil. For high voltages protection of this output, connection to the pin 7 zener is recommended. In this situation R_8 must limit the zener current, too, and R_1 limits pin 6 current if RPM module pad is accidentally connected to V_S.
7	AUX. ZENER	A 21V (typ) General Purpose Zener. Its current must be limited by an external resistor.
8	RECOVERY TIME	A capacitor connected between this pin and ground sets the slope of the dwell time variation as it rises from zero to the correct value. This occurs after the detection of $I_{coil} \leq 94\% I_{nom}$, just before the low transition of the hall-effect signal pulse. The duration of the slow recovery is given by : $t_{src} = \mathbf{12,9\ R_7\ C_{src}}$ (ms) where R_7 is the biasing resistor at pin 12 (in KΩ) and C_{src} is the delay capacitor at pin 8 (in µF).
9	MAX CONDUCTION TIME	A capacitor connected between this pin and ground determines the intervention delay of the permanent conduction protection. After this delay time the coil current is slowly reduced to zero. Delay Time T_p is given by : $T_p = \mathbf{16\ C_p\ R_7}$ (ms) where R_7 is the biasing resistor at pin 12 (in KΩ) and C_P is the delay capacitor at pin 9 (in µF).
10	DWELL CONTROL TIMER	The capacitor C_T connected between this pin and ground is charged when the Hall effect output is High and is discharged at the High to Low transition of the Hall effect signal. The recommended value is 100nF using a 62KΩ resistor at pin 12.
11	DWELL CONTROL	The average voltage on the capacitor C_W connected between this pin and ground depends on the motor speed and the voltage supply. The comparison between V_{CW} and V_{CT} voltage determines the timing for the dwell control. For the optimized operation of the device $C_T = C_W$; the recommended value is 100nF using a 62kΩ resistor at pin 12.
12	BIAS CURRENT	A resistor connected between this pin and ground sets the internal current used to drive the external capacitors of the dwell control (pin 10 and 11), permanent conduction protection (pin 9) and slow recovery time (pin 8). The recommended value is 62KΩ.

PIN FUNCTIONS (continued)

N°	Name	Function
13	CURRENT SENSING	Connection for the Coil Current Limitation. The current is measured on the sensing resitor R_S and divided on R_{10}/R_{11} resistors. The current limitation value is given by : $I_{sens} = 0.32 \cdot \frac{R_{10} + R_{11}}{R_S \cdot R_{11}}$
14	DRIVER EMITTER OUTPUT	Current Driver for the External Darlington. To ensure stability and precision of T_{desat} C_c and R_9 must be used. Recommended value for R_9 is 2 KΩ in order not to change the open loop gain of the system. R_c may be added to C_c to obtain greater flexibility in various application situations. C_c and R_c values ranges are 1 to 100nF and 5 to 30KΩ depending on the external darlington type.
15	OVERVOLTAGE LIMIT	The darlington is protected against overvoltage by means of an internal zener available at this pin and connected to pin 14. The external divider R_3/R_2 defines the limitation value given by : $V_{ovp} = (\frac{22.5}{R_3} + 5.10^{-3})\ R_2 + 22.5$
16	DRIVER COLLECTOR INPUT	The collector current of the internal driver which drives the external darlington is supplied through this pin. Then the external resistor R_6 limits the maximum current supplied to the base of the external darlington.

ELECTRICAL CHARACTERISTICS (V_S = 14.4 V, – 40 °C ≤ T_j ≤ 125 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_3	Min Op. Voltage		3.5			V
I_3	Supply Current	V_3 = 6V V_3 = 4V	5 7	18	25 16	mA mA
V_S	Voltage Supply				28	V
V_{Z3}	Supply Clamping Zener Voltage	I_{Z3} = 70mA	6.8	7.5	8.2	V
V_5	Input Voltage Low Status Input Voltage High Status		 2.5		0.6	 V V
I_5	Input Current	V_5 = LOW	– 510		– 280	µA
V_{16-14}	Darlington Driver Sat. Current	I_{14} = 50mA I_{14} = 180 mA			0.5 0.9	V V
V_{SENS}	Current Limit. Sensing Voltage	V_S = 6 to 16V	260	320	370	mV
I_{11C}	C_w Charge Current	V_S = 5.3 to 16V V_{11} = 0.5V T = 10 to 33ms	– 11.0	– 9.3	– 7.8	µA
I_{11D}	C_w Discharge Current	V_S = 5.3 to 16V V_{11} = 0.5V T = 10 to 33ms	0.5	0.7	1.0	µA
I_{11C}/I_{11D}		V_S = 5.3 to 16V V_{11} = 0.5V T = 10 to 33ms See note 1	7.8		22.0	
$\frac{I_{SRC}}{I_{SENS}}$	Percentage of Output Current Determining the Slow Recovery Control Start (fig. 2), note 2		90	94	98	%
T_{SRC}	Duration of Altered t_d/T Ratio after SRC Function Start (fig. 2)	C_{SRC} = 1µF R_7 = 62KΩ		0.8		s
V_{Z15}	External Darlington over Voltage Protection Zener Voltage	I_{15} = 5mA I_{15} = 2mA	19 18	22.5 21.5	26 25	V V
T_P	Permanent Conduction Time	V_5 = High C_P = 1µF R_7 = 62KΩ	0.4	1.1	1.8	s
V_{6SAT}	RPM Output Saturation Voltage	I_6 = 18.5mA I_6 = 25mA			0.5 0.8	V V
$I_{6\ leak}$	RPM Output Leakage Current	V_6 = 20V			50	µA
V_{Z7}	Auxiliary Zener Voltage	I_7 = 20mA	19		27	V
V_{12}	Reference Voltage		1.20	1.25	1.30	V

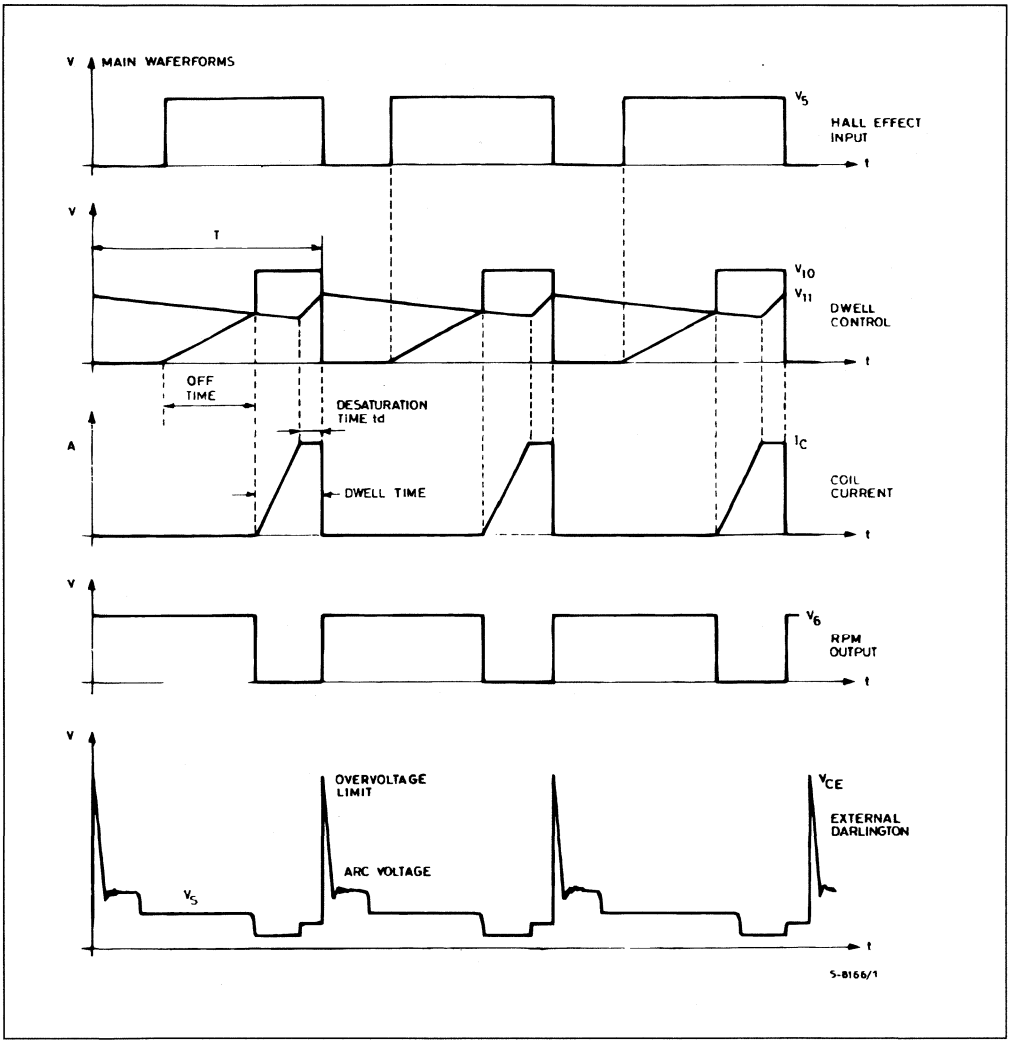
Notes : 1. t_d/t desaturation ratio is given by :

$$\frac{td}{T} = \frac{1}{1 + I_{11C}/I_{11D}}$$

2. $I_{SENSE} = I_{COIL}$ when the external Darlington is in the active region.

APPLICATION INFORMATION

Figure 1 : Main Waveforms.



DWELL ANGLE CONTROL

The dwell angle control circuit calculates the conduction time D for the output transistor in relation to the speed of rotation, to the supply voltage and to the characteristics of the coil.

On the negative edge of the Hall-effect input signal the capacitor C_W begins discharging with a constant current I_{11D}. When the set peak value of the coil current is reached, this capacitor charges with a constant current $I_{11C} = 13.3 \times I_{11D}$, and the coil current is kept constant by desaturathing the driven stage and the external darlington.

The capacitor C_T starts charging on the positive edge of the Hall-effect input signal with a constant current I_{10C}. The dwell angle, and consequently the starting point of the coil current conduction, is decided by the comparison between V_{10} and V_{11}.

A positive hysteresis is added to the dwell comparator to avoid spurious effects and C_T is rapidly discharged on the negative edge of Hall-effects input signal.

In this way the average voltage on C_W increases if the motor speed decreases and viceversa in order to maintain constant the ratio $\frac{t_d}{T}$ at any motor speed.

$\frac{t_d}{T}$ is kept constant (and not $\frac{D}{T}$ = cost) to control the power dissipation and to have sufficient time to avoid low energy sparks during acceleration.

DESATURATION TIMES IN STATIC CONDITIONS

In static conditions, if $C_T = C_W$ as recommended and if the values of the application circuit of fig. 4 are used,

$$\frac{t_d}{T} = \frac{1}{1 + I_{11C}/I_{11D}}$$

DESATURATION TIMES IN LOW AND HIGH FREQUENCY OPERATION

Due to the upper limit of the voltage range of pin 11, if the components of fig. 4 are used, below 10Hz (300 RPM for a 4 cylinder engine) the OFF time reaches its maximum value (about 50ms) and then the circuit gradually loses control of the dwell angle because D = T – 50ms.

Over 200Hz (6000 RPM for a 4 cylinder engine) the available time for the conduction is less than 3.5ms.

If the used coil is 6mH, 6A, the OFF time is reduced to zero and the circuit loses the dwell angle control.

TRANSIENT RESPONSE

The ignition system must deliver constant energy even during the condition of acceleration and deceleration of the motor below 80Hz/s. These conditions can be simulated by means of, a signal gene-rator with a linearly modulated frequency between 1Hz and 200Hz (this corresponds to a change bet-ween 30 and 6000 RPM for a 4 cylinders engine).

CURRENT LIMIT

The current in the coil is monitored by measuring the I_{sense} current flowing in the sensing resistor R_S on the emitter of the external darlington. I_{sense} is given by :

$$I_{sense} = I_{coil} + I_{14}$$

When the voltage drop across Rs reaches the internal comparator threshold value the feedback loop is activated and I_{sense} kept constant (fig. 1) forcing the external darlington in the active region. In this condition :

$$I_{sense} = I_{coil}$$

When a precise peak coil current is required R_S must be trimmed or an auxiliary resistor divider (R_{10}, R_{11}) added :

$$Icpeak\ (A) = \frac{0.320}{RS} \cdot \left(\frac{R10}{R11} + 1\right)$$

SLOW RECOVERY CONTROL (fig. 2)

If I_{sense} has not reached 94% of the nominal value just before the negative edge of the Hall-effect input signal, the capacitor C_{src} and C_W are quickly discharged.

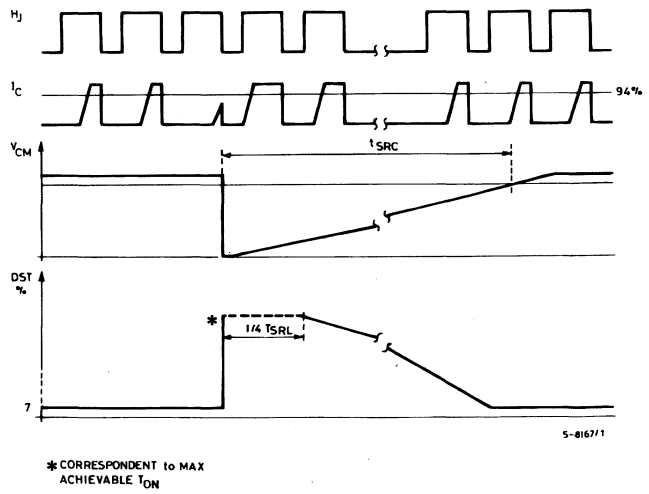
These capacitors remain discharged as long as the pick-up signal is "low". At the next positive transition of the input signal the load current starts immediately, producing the maximum achievable T_{desat} ; then the voltage on C_{SRC} increases linearly until the standby value is reached. During this recovery time the C_{SRC} voltage is converted into a current which, subtrated from the charging current of the dwell capacitor, produces a T_{desat} modulation. This means that the T_{desat} decreases slowly until its value reaches, after a time T_{SRC}, the nominal 7% value.

The time T_{SRC} is given by :

$$T_{rsc} = 12{,}9\ R_7\ C_{SRC} \qquad (ms)$$

where R_7 is the biasing resistor at pin 12 (in KΩ) and C_{src} the capacitor at pin 8 (in μF).

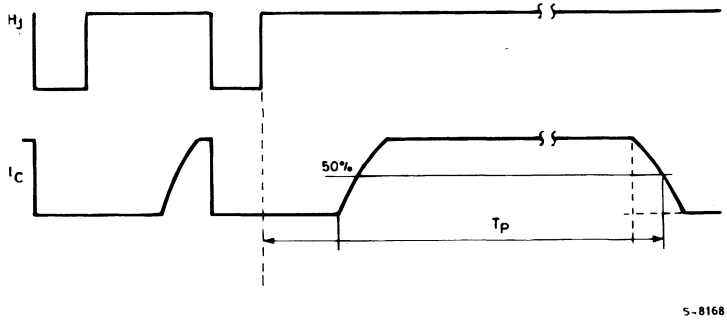
Figure 2 : SRC : I_{coil} Failure and Time Dependence of Active Region.



H_J : Input signal
I_C : Coil current

V_{CM} : Voltage on capacitor C_{SRC}.
D_{ST} : Percentage of imposed desaturation time.

Figure 3 : Permanent Conduction Protection.



PERMANENT CONDUCTION PROTECTION (fig. 3)

The permanent conduction protection circuit monitors the input period, charging C_P with a constant current when the sensor signal is high and discharging it when the sensor signal is low. If the input remains high for a time longer than T_P the voltage across C_P reaches an internally fixed value forcing the slow decrease of coil current to zero. A slow decrease is necessary to avoid undesired sparks. When the input signal goes low again C_P is swiftly discharged and the current control loop operates normally.

The delay time T_P is given by :

$$T_P \text{ (sec)} = 18\ C_P\ R_7$$

Where R_7 is the biasing resistor on pin 12 (in KΩ) and Cp the delay capacitor at pin 9 (in μF).

OTHER APPLICATION NOTES

DUMP PROTECTION

Load dump protection must be implemented by an external zener if this function is necessary. In fig. 4 DZ_2 protects the driver stage, the connection between pin 6 and 7 protects the output transistor of pin 6. Moreover DZ_1 protects both the power supply input (pin 3) and Hall-effect sensor.

Resistor R_4 is necessary to limit DZ_1 current during load dump.

OVERVOLTAGE LIMITATION

The external darlington collector voltage is sensed by the voltage divider R_2, R_3. The voltage limitation increases rising R_2 or decreasing R_3.

Due to the active circuit used, an R_o C_o series network is mandatory for stability during the high voltage condition.

R_o C_o values depend on the darlington used in the application.

Moreover the resistor R_{13} is suggested to limit the overvoltage even when supply voltage is disconnected during the high voltage condition.

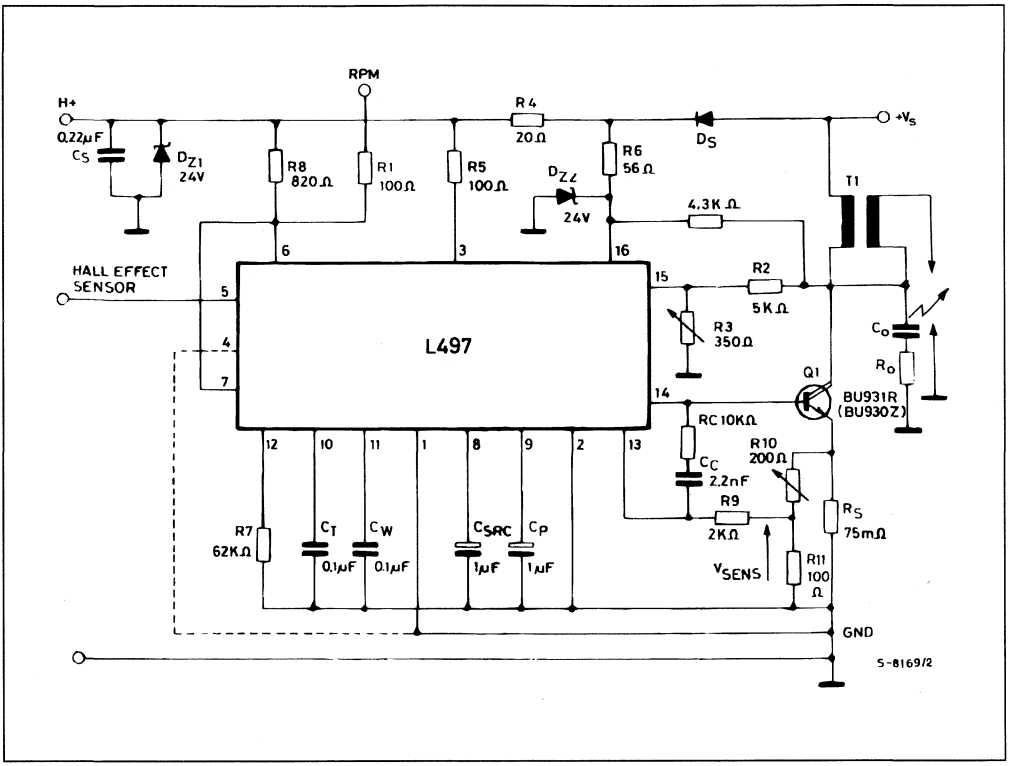
REVERSE BATTERY PROTECTION

Due to the presence of external impedance at pin 6, 3, 16, 15, L497 is protected against reverse battery voltage.

NEGATIVE SPIKE PROTECTION

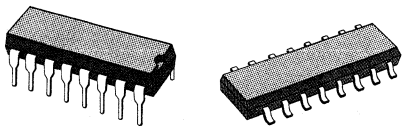
If correct operation is requested also during short negative spikes, the diode D_S and capacitor C_S must be used.

Figure 4 : Application Circuit.



ELECTRONIC IGNITION INTERFACE

- DIRECT DRIVING OF THE EXTERNAL POWER DARLINGTON
- SEPARATE INTERFACE FOR HALL EFFECT OR INDUCTIVE SENSOR
- SEPARATE OPEN COLLECTOR BOOSTER
- COIL CURRENT PEAK VALUE LIMITER
- SIGNAL TO μP WHEN 85% AND FULL NOMINAL COIL CURRENT ARE REACHED
- CONTINUOUS COIL CURRENT PROTECTION
- EXTERNAL DARLINGTON OVERVOLTAGE PROTECTION



DIP 16 **SO-16J**

ORDER CODES : L530
L530 D1

DESCRIPTION

The L530 is an integrated circuit designed for use with an NPN darlington in microprocessor controller ignition systems.

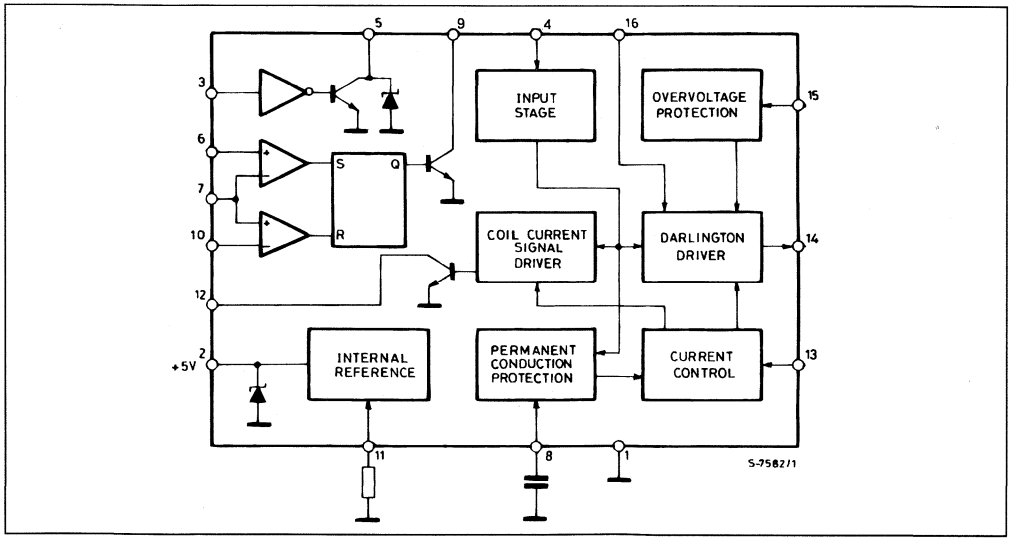
Primarily it acts as an independent controller for the current in the high voltage spark coil.

Charging of the coil is enabled under control of the micro. The device generates a feedback signal for the micro when a fixed percentage and the full nominal current into the coil are reached.

If the enable coil current input signal is active for more than a programmable time, the coil current is switched off slowly to protect the coil and avoid spurious pulses.

The L530 also contains a pulse shaper for the position sensor (both hall effect or magnetic) and an open collector booster which may be used, for example, for the RPM output.

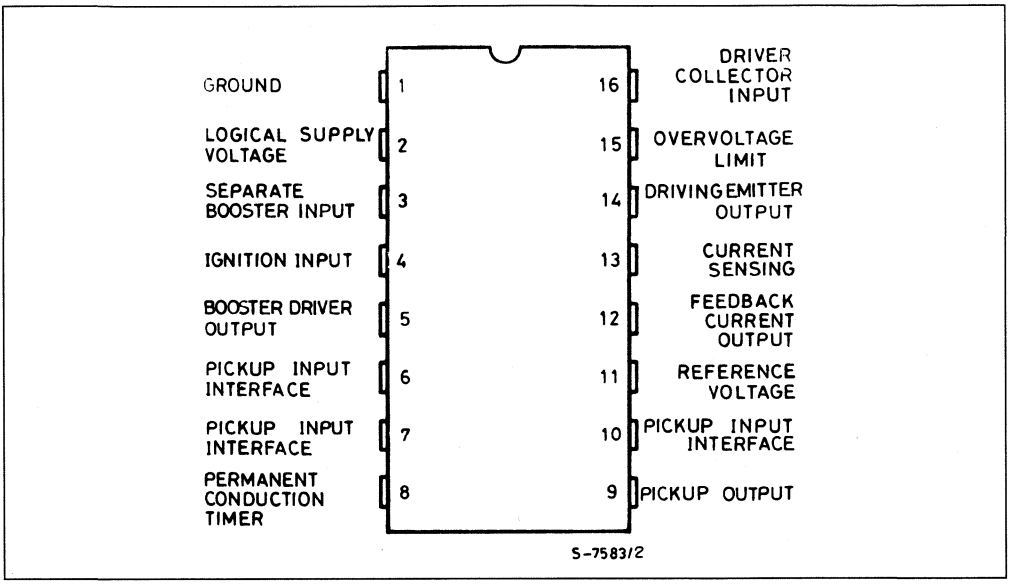
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Max. Supply Voltage (pin 16)	24	V
V_R	Reverse Battery Voltage	– 16	V
P_{tot}	Power Dissipation at T = 90°C	1.2	W
T_j, T_{stg}	Junction and Storage Temperature	– 55 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

$R_{th\ j\text{-}alumina}$ (*)	Thermal Resistance Junction-alumina for SO 16	Max	50	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient for DIP 16	Max	80	°C/W

(*) Thermal resistance junction-pins with the middle of an alumina supporting substrate measuring 15x20mm ; 0.65mm thickness and infinite heathsink.

ELECTRICAL CHARACTERISTICS (V_B = 14.4V, – 40°C ≤ T_J ≤ 125°C unless otherwise specified ; referred to the application circuit of fig. 2)

Symbol	Parameter	Test Conditons	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage (pin 2)		4.5		5.5	V
I_S	Operating Supply Current (pin 2)	V_S = 5V, V_{4H}	8	13	18	mA
V_Z (*)	Internal Zener Voltage (pin 2)	I_S = 80mA	6	7.5	9	V
I_3	Input Current (pin 3)	V_3 = 2V		0	230	µA
V_{REF}	Reference Voltage at pin 11	I_{11} = – 20µA	1.18	1.23	1.35	V
V_{L3}	Input Low Voltage (pin 3)				0.4	V
V_{H3}	Input High Voltage (pin 3)		2.0			V
V_{L4}	Input Low Voltage (pin 4)				0.4	V
V_{H4}	Input High Voltage (pin 4)		2.0			V
V_{SENS}	Current Limit. Sensing Voltage (pin 13)		210	260	310	mV
V_{CEsat}	Series Darlington Driver Sat. Voltage (pin 16-14).	I_O = 50mA I_O = 180mA			0.5 1.0	V V
P_{ON}	Percentage of Coil Current Determining the Feedback ON (pin 12).		75	85	90	%
V_{OVP}	Overvoltage Protect. Zener Voltage (pin 15)	I_{OVP} = 7mA	21	25	30	V
T_{PC}	Permanent Conduction Protection Time (**)		0.25	0.35	0.5	sec.
V_{FL}	Feedback Ouptut Sat. Voltage (pin 12)	$V_{pin\ 4}$ = H $I_{pin\ 12}$ = 5mA			1.0	V
I_{L12}	Leakage Current (pin 12)	V_S = 5V			10	µA
V_{ZRPM}	RPM Output Int. Zener Voltage (pin 5)	I_Z = 20mA	19		29	V
V_{SATRPM}	RPM Output Sat. Voltage (pin 5)	I_{RPM} = 10mA I_{RPM} = 20mA			0.5 1.0	V V
V_{OS}	Comparator Inputs Offset Voltage (pins 6, 7, 10)				± 15	mV
I_{BIAS}	Comparator Inputs Bias Current			– 50	– 300	mA
I_{OS}	Comparator Inputs Offset Current			± 20	± 100	nA
CMR	Common Mode Range		0		V_S – 1.6	V
V_{PF}	Pulse Former Output Low Voltage (pin 9)	$V_{pin\ 6} - V_{pin\ 7}$ > 10mV $V_{pin\ 6} = V_{pin\ 10}$			0.8	V
I_{L9}	Pulse Former Output Leakage Current	$V_{pin\ 7} - V_{pin\ 6}$ > 10mV $V_{pin\ 6} = V_{pin\ 10}$ $V_{pin\ 9}$ = 5V			20	µA
I_4	Output Current (pin 7)		– 650	– 380	– 180	µA
I_{L5}	Leakage Current (pin 5)	V_S = 16V			22	µA

(*) This parameter measurement must be considered if the IC is not directly supplied by 5V voltage regulator. In this case a suiited external resistor must be used to limit pin 2 current.

(**) See Fig.4.

PIN FUNCTIONS (refer to fig. 2)

N°	Name	Function
1	GROUND	This pin must be connected to ground.
2	SUPPLY VOLTAGE	5V Supply input.
3	BOOSTER INPUT SIGNAL	Input signal to separate booster stage. This drive circuit may be used, for example, for the RPM output signal of the micro.
4	IGNITION INPUT SIGNAL	When this pin is kept low the external darlington is switched on and the current flows through the coil for all the time the input is low, being active the internal current limitation.
5	BOOSTER DRIVER OUTPUT	Open collector output signal of the separate booster circuit. The phase is the same as the input command at pin 3.
6-7	PICKUP INPUT INTERFACE	Together with pin 10, these inputs realize a separate interface stage for both hall effect or magnetic sensor. Pin 6 is the non-inverting input of the internal comparator which sets, the internal flip-flop. Pin 7 is connected both to the inverting input of the comparator setting the latch and the non-inverting input of the second internal comparator which resets the flip-flop. See fig. 4.
8	PERMANENT CONDUCT. TIMER	A capacitor C_1 connected between this pin and ground sets the delay of the permanent conduction protection in the coil current. The typical delay time value T_{PC} is given by : $T_{PC} = 17\ C_1\ R_{10}$ Where R_{10} is the biasing resistor at pin 11 (in kΩ) and C_1 is the delay capacitor at pin 8 (in μF).
9	PICKUP OUTPUT	Open collector output from the internal flip-flop of the interface circuit for the sensor. This memory is set by the comparator connected to pin 6 and 7 and it is reset by the second comparator connected to pin 7 and 10. The output is a negative logic. See fig. 4.
10	PICKUP INPUT INTERFACE	Inverting input of the second comparator which resets the internal flip-flop of the sensor interface circuit. See pin 6 and 7 Description.
11	REFERENCE VOLTAGE	A resistor R_{10} connected between this pin and ground sets the current used for the internal references and to drive the external capacitor of the permanent conduction protection. The recommended value is 62kΩ.
12	FEEDBACK CURRENT OUTPUT	Open collector output that indicates to micro when the 85% (typ) and the full current flows through the coil. As shown in the fig. 3, this signal goes high when the fixed percentage is reached and goes low when the full programmed coil current is detected.
13	CURRENT SENSING	Connection for coil current limitation. The current is measured on the sense resistor R_{sense} and divided on R_1/R_2. The current limitation value is given by : $I_{SENS} = 0.26 \frac{R_1 + R_2}{R_{sens}\ R_2}$
14	DRIVER EMITTER OUTPUT	Current driver for the external darlington. To ensure stability and precision of T_{desat} C_a and R_3 must be used. Recommended value for R_3 is 2kΩ in order not to change the open loop gain of the system. R_a may be added to C_a to obtain greater flexibility in various application situations. C_a and R_a values ranges are 1 to 100nf and 5 to 30kΩ depending on the external darlington type.

PIN FUNCTIONS (refer to fig. 2) (continued)

N°	Name	Function
15	OVERVOLTAGE LIMIT	The darlington is protected against overvoltage by means of an internal zener available at this pin and connected to pin 14. The external divider R_4/R_5 defines the limitation value given as first approximation by : $V_{ovp} = (\frac{22.5}{R_5} + 7 \cdot 10_{-3}) R_4 + 22.5$
16	DIRVER COLLECTOR INPUT	The collector current of the internal driver which drives the external darlington is supplied through this pin. The maximum current supplied through this pin. Then the external resistor R_6 limits the maximum current supplied to the base of the external darlington.

CIRCUIT OPERATION

As shown in the fig.1, the L530 is particularly suitable for use with a microprocessor as an electronic ignition interface, driving the current through the coil by means of an external darlington.

The device takes the ignition input signal (pin 4) from the microprocessor to drive the darlington, and the output active for all the time in which the input is low.

The ignition input signal (active Low) coming from the microprocessor switches on the device output stage driving the external darlington.

The peak value of the primary current flowing into the coil is limited to a predetermined level by means of a negative feedback circuit including a current sensing resistor, a comparator, the driver stage and the power switch.

An output signal, High when the current flowing into the coil has reached 85% of the final value and Low when the full nominal current has been reached is available at pin 12. This signal is used by the microprocessor to control the dwell time. As shown in the fig. 3 three cases are possible.

In the first case the current limitation is reached ; then, when the input command goes high (spark command) the feedback to microprocessor has already gone low.

In the second case the full current is not reached (very high speed/acceleration or very low battery voltage). Then the output signal goes low together with the spark command.

In the last case a feedback pulse is not present ; this means that the 85% of the programmed current is not reached.

Figure 1 : Typical System Configuration.

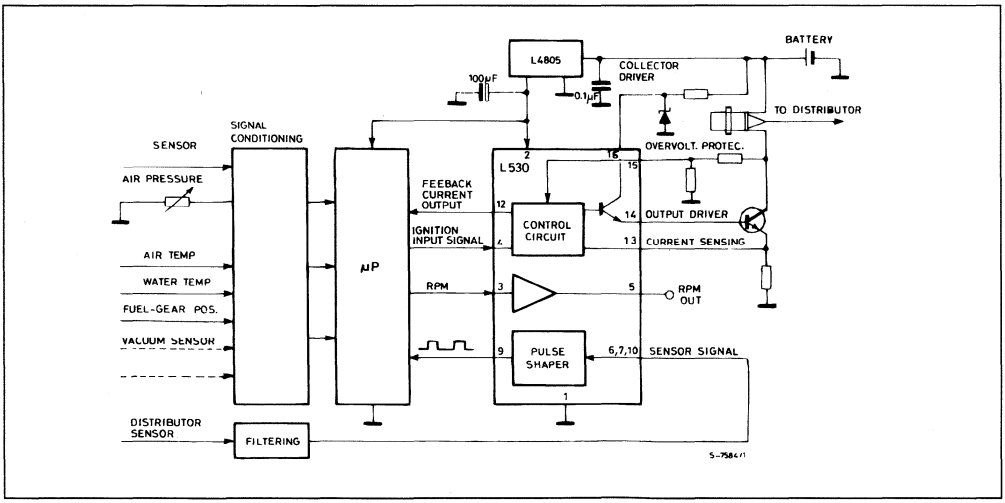


Figure 2 : Application Circuit.

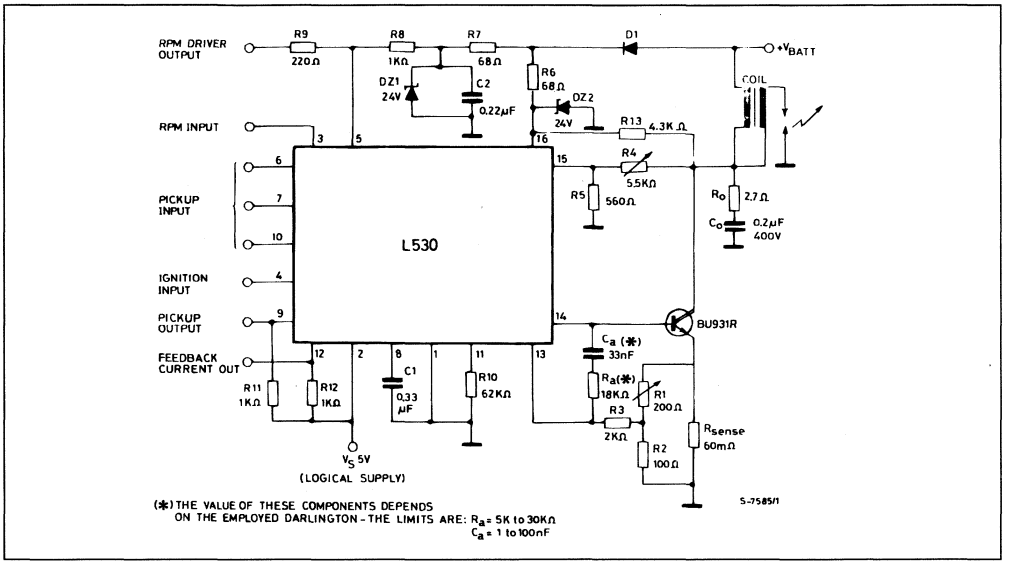
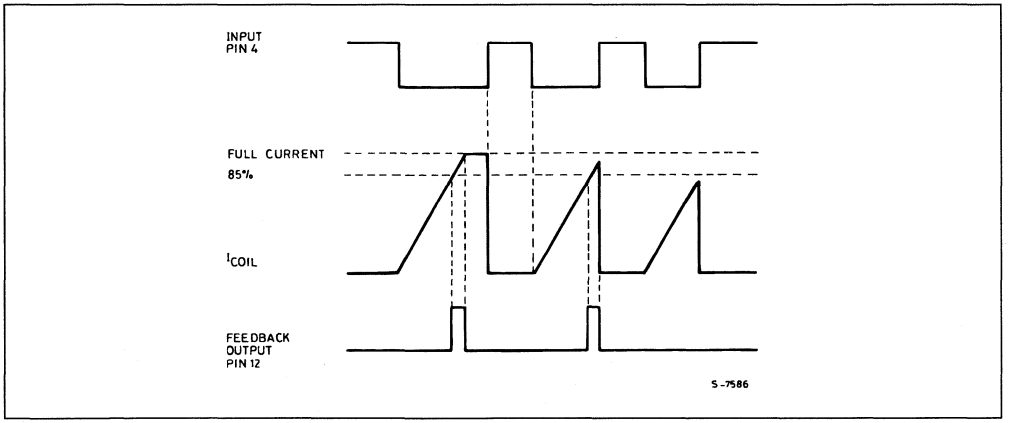


Figure 3 : Typical Operation Waveforms.



CURRENT LIMIT

The current in the coil is monitored by measuring the I_{sense} current flowing in the sensing resistor R_{sense} on the emitter of the external darlington. I_{sense} is given by :

$$I_{sense} = I_{coil} + I_{14}$$

When the voltage drop across R_{sense} reaches the internal comparator threshold value the feedback loop is activated and I_{sense} kept constant (fig. 3) forcing the external darlington in the active region. In this condition :

$$I_{sense} = I_{coil}$$

When a precise peak coil current is required R_{sense} must be trimmed or an auxiliary resistor divider (R_1, R_2)added :

$$I_{cpeak}\,(A) = \frac{V_{sense}}{R_{sense}} \cdot \left(\frac{R_1}{R_2} + 1\right)$$

PERMANENT CONDUCTION PROTECTION (fig.4)

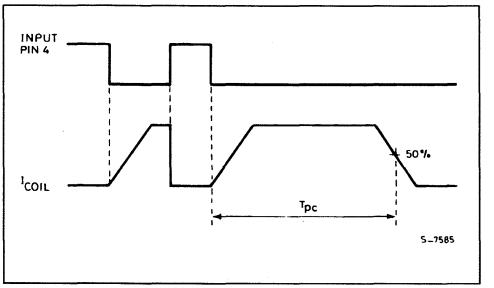
The permanent conduction protection circuit monitors the input period, charging C_1 with a constant current when the sensor signal is Low and discharging it when the sensor signal is High. If the input remains Low for a time longer than T_{PC} the voltage across C_1 reaches an internally fixed value forcing the slow decrease of coil current to zero. A low decrease is necessary to avoid undesired sparks. When the input signal goes High again C_1 is swiftly discharged and the current control loop operates normally.

The typical delay time value T_{PC} is given by :

$$T_{PC}\ (ms) = 17\ C_1\ R_{10}$$

Where R_{10} is the biasing resistor on pin 11 (in K ohm) and C_1 the delay capacitor at pin 8 (in uF).

Figure4 : Permanent Conduction Protection Timing.



OTHER APPLICATION NOTES

DUMP PROTECTION

Load dump protection must be implemented by an external zener if this function is necessary. In fig. 2 DZ_2 protects the driver stage.

OVERVOLTAGE LIMITATION

The external darlington collector voltage is sensed by the voltage divider R_4, R_5. The voltage limitation increases rising R_4 or decreasing R_5.

Due to the active circuit used, an Ro Co series network is mandatory for stability during the high voltage condition.

Ro Co values depend on the darlington used in the application.

Moreover the resistor R_{13} is suggested to limit the overvoltage even when supply voltage is disconnected during the high voltage condition.

REVERSE BATTERY PROTECTION

Due to the presence of external impedance at pin 5, 16, 15 L530 is protected against reverse battery voltage.

NEGATIVE SPIKE PROTECTION

If correct operation is requested also during short negative spikes, the diode D_1 and capacitor C_2 must be used.

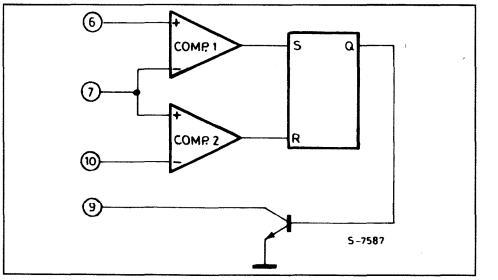
SENSOR INTERFACE

The device contains a separate pulse shaper for the sensor. As shown in fig. 5, this circuit is made by two comparators and flip-flop.

The internal flip-flop is set by the first comparator and reset by the second one. In this way it is possible to interface both the Hall effect and the magnetic pick-up sensor. Fig. 6 shows a typical solution that implements an input comparator with hysteresis able to detect the zero crossing during the input's negative edge (fig. 7). A small positive theshold guarantees the correct switch-on at low RPM.

Three pins allow the use of this interface in a wide range of configurations and, thanks to internal memory, it is possible to obtain a behaviour with hysteresis in order to have a good noise immunity.

Figure 5 : Interface for Hall Effect or Inductive Sensor.



BOOSTER OUTPUT

An independent booster output is also included in the L530 to permit a separate driving stage from the microprocessor (typically employed for RPM output signal).

The open collector output is protected with an internal zener diode that allows the connection a unstabilized voltage by means of a limiting resistor.

Figure 6 : Input Comparator with Hysteresis.

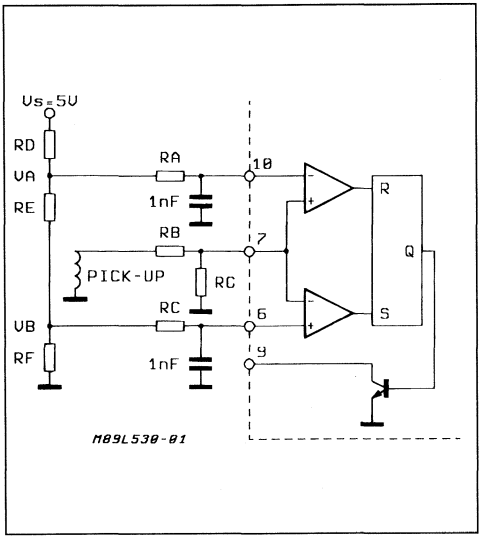
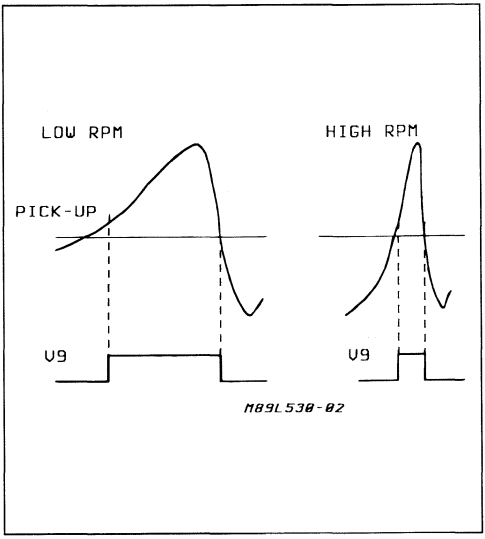


Figure 7 : Zero Crossing Detection.



SGS-THOMSON MICROELECTRONICS

STHI07N50
STHI07N50FI

HIGH INJECTION N-CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS (IGBT)

PRELIMINARY DATA

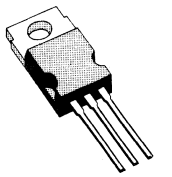
TYPE	V_{DSS}	I_D
STHI07N50	500 V	7 A
STHI07N50FI	500 V	7 A

- HIGH INPUT IMPEDANCE
- LOW ON-VOLTAGE
- HIGH CURRENT CAPABILITY

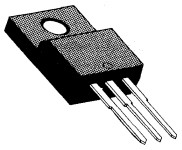
APPLICATIONS:

- AUTOMOTIVE IGNITION
- DRIVERS FOR SOLENOIDS AND RELAYS

N - channel High Injection POWER MOS transistors (IGBT) which features a high impedance insulated gate input and a low on-resistance characteristic of bipolar transistors. This low resistance is achieved by conductivity modulation of the drain. These devices are particularly suited to automative ignition switching. They can also be used as drivers for solenoids and relays.

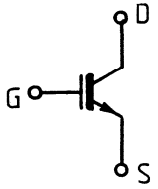


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	500		V
V_{GS}	Gate-source voltage	±20		V
I_D(•)	Drain current (contin.) at $T_c=25°C$	7		A
I_{DM}	Drain current (pulsed)	20		A
		STHI07N50	**STHI07N50FI**	
P_{tot}	Total dissipation at $T_c<25°C$	100	35	W
	Derating factor	0.8	0.28	W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1.25	3.6	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

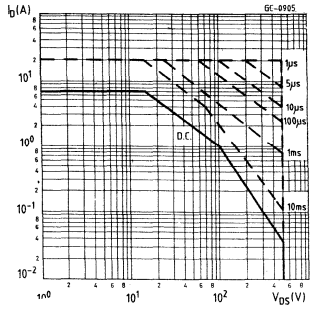
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8	T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON (*)							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10 V	I_D = 7 A			2.7	V
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 20 V	I_D = 7 A	2.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		850 90 40	950 140 80	pF pF pF
SWITCHING							
	RESISTIVE LOAD						
$t_{d\ (on)}$	Turn-on delay time	V_{DD} = 400 V	I_D = 10 A		100	150	ns
t_r	Rise time	V_g = 10 V	R_g = 100 Ω		700	1000	ns
$t_{d\ (off)}$	Turn-off delay time				500	700	ns
t_f	Fall time				800	1500	ns

ELECTRICAL CHARACTERISTICS (Continued)

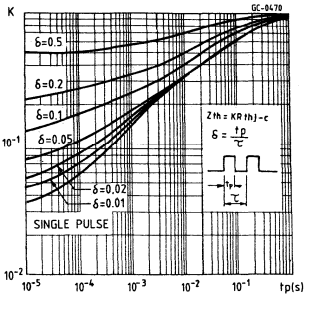
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING (continued)					
INDUCTIVE LOAD $t_{d\ (off)}$ Turn-off delay time t_f Fall time	V_{DD} = 12 V $V_{DS\ clamp}$ = 350 V I_D = 7 A V_{GS} = 10 V R_g = 100 Ω L = 10 mH T_j = 100°C		1 1.1	1.4 1.5	µs µs
USE TEST	V_{CC} = 14 V $V_{DS\ clamp}$ = 400 V L = 7 mH	6			A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1,5%
■ See note on ISOWATT220 or this datasheet

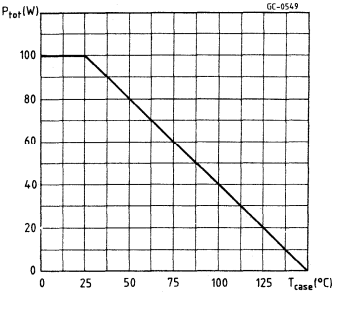
Safe operating areas (standard package)



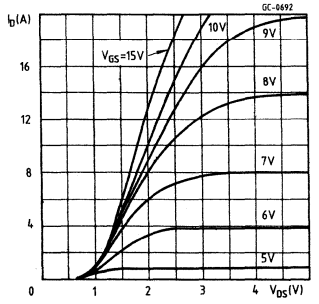
Thermal impedence (standard package)



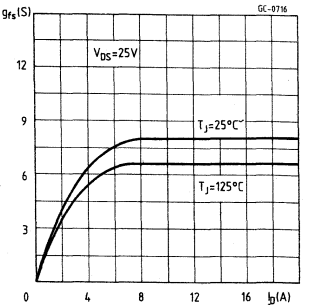
Derating curve (standard package)



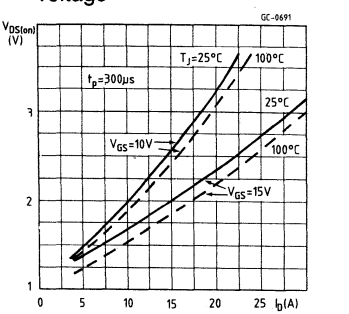
Output characteristics



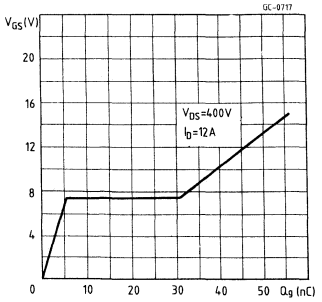
Transconductance



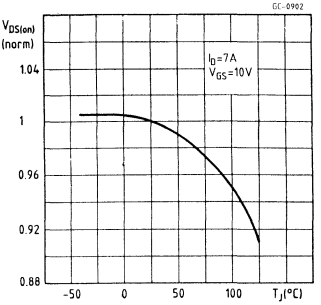
Static drain-souce on voltage



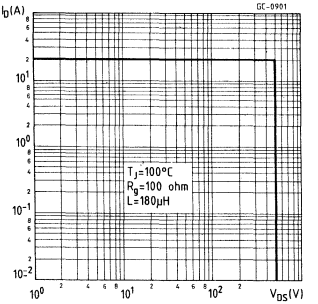
Gate charge vs gate-source voltage



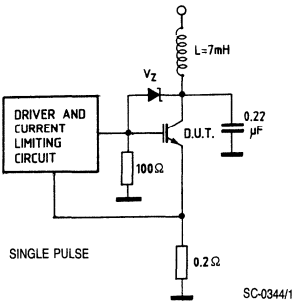
Normalized on voltage vs temperature



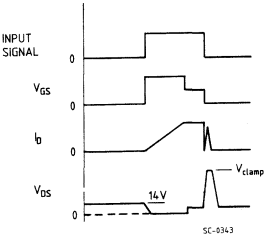
Reverse biased SOA



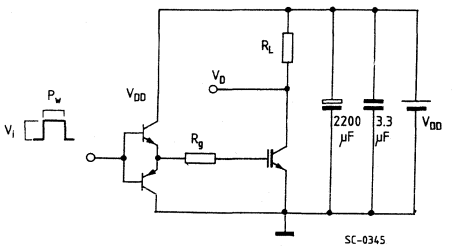
Functional test circuit



Functional test waveforms

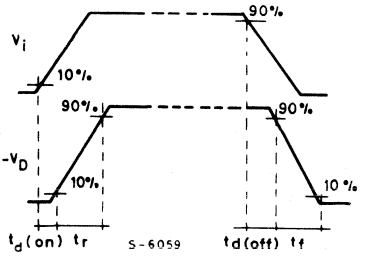


Switching times test circuit for resistive load

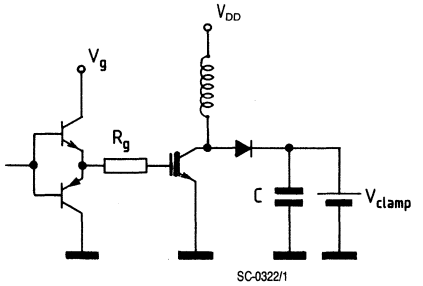


Pulse width ≤ 100 μs
Duty cycle ≤ 2%

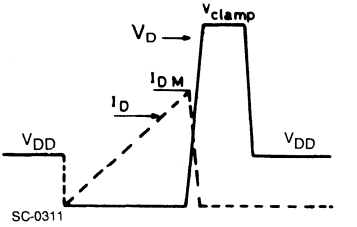
Switching time waveforms for resistive load



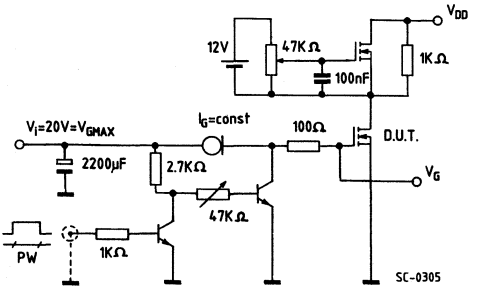
Clamped inductive load and RBSOA test circuit



Clamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

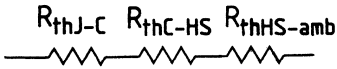
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

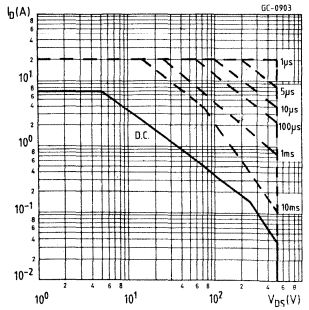
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

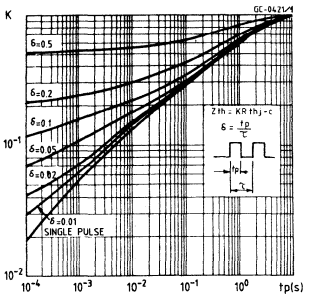


ISOWATT DATA

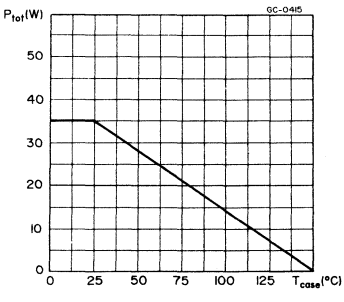
Safe operating areas



Thermal impedance



Derating curve



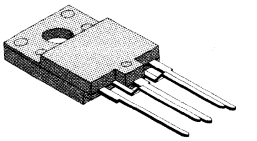
SGS-THOMSON MICROELECTRONICS

VB020

FULLY INTEGRATED HIGH VOLTAGE DARLINGTON FOR ELECTRONIC IGNITION

ADVANCE DATA

- PRIMARY COIL VOLTAGE UP TO 450 V
- COIL CURRENT LIMIT INTERNALLY SET
- TTL/CMOS COMPATIBLE INPUT
- BUILT-IN COLLECTOR-EMITTER VOLTAGE CLAMPING
- OVERVOLTAGE PROTECTION OF THE DRIVING CIRCUIT
- FULLY INSULATED FIVE LEAD POWER PACKAGE



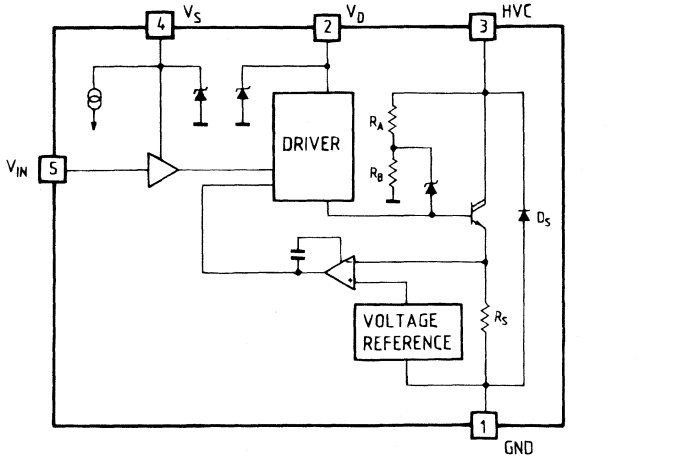
ISOWATT 5

DESCRIPTION

The VB020 is a monolithic high voltage integrated circuit made using SGS-THOMSON Microelectronics Vertical Intelligent Power Technology, which combines a vertical current flow power darlington with a TTL/CMOS compatible input driving circuit.

Built-in protection circuits for coil current limiting and collector voltage clamping allows the VB020 to be used as a smart, high voltage, high current interface in advanced electronic ignition systems.

SCHEMATIC DIAGRAM



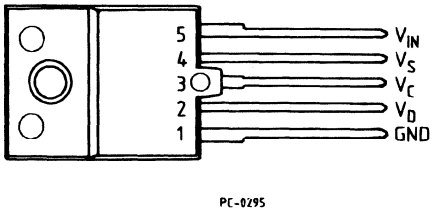
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_C	Collector Current (internally limited)	6.25	A
V_D	Driving Stage Supply Voltage	24	V
V_S	Control Circuit Supply Voltage	24	V
I_D	Control Circuit Supply Current	200	mA
V_{IN}	Maximum Input Voltage	V_S	V
P_{tot}	Maximum Power Dissipation at $T_{case} \leq 25°C$	50	W
T_{op}	Operating Junction Temperature Range	– 40 to 150	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	2.5	°C/W

CONNECTION DIAGRAM



PC-0295

PIN FUNCTION

N°	Name	Function
1	GND	Emitter and Control Ground
2	V_D	Driver Stage Supply Voltage
3	V_C	High Voltage Open Collector Output
4	V_S	Control Circuit Supply Voltage
5	V_{IN}	Logical Input

ELECTRICAL CHARACTERISTICS : $V_B = V_{CC} = 12$ V ; $T_{amb.} = 25$ °C ; $V_{IN} = 0.4$ V ; $R_C = 0.5\ \Omega$; $R_S = 300\ \Omega$; $R_D = 50\ \Omega$; unless otherwise specified see fig 1

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CL}	High Voltage Clamp	Functional Test See Figs 3, 4	380		450	V
$V_{CE(sat)}$	Saturation Voltage of the Power Stage	$I_C = 5$ A, $I_D = 40$ mA $V_{IN} = 5$ V pulsed $t_{on} = 300\ \mu s$, $f_{osc} = 1$ Hz		1.5	2	V
V_D	Base Driver Stage Supply Voltage		4.5		18	V
$I_{D(stdby.)}$	Base Driver Stage Standby Current	$V_{IN} = 0.4$ V			1	mA
$V_{D(sw.on)}$	Base Driver Stage Current at Switch-on	$V_{IN} = 4$ V		80	200	mA
V_S	Control Circuit Supply Voltage		5.6		9	V
I_S	Control Circuit Standby Current			2.5	10	mA
I_{CL}	Coil Current Limit at Switch-on	Functional Test See Figs 3, 4	5.5	6	6.5	A
V_{INH}	High Level Input Voltage	$I_C = 5$ A	2.4		V_S	V
V_{INL}	Low Level Input Voltage	$I_C < 2$ mA, $V_{3,1} = V_B$	0		0.8	V
I_{INH}	High Level Input Current	$V_{IN} = 2.4$ V			100	μA
t_s	Storage Time	$I_C = I_{CL}$; $V_{CL} = 350$ V $V_{IN} = 12$ V, See Figs 1, 2		12		μs
t_f	Fall Time	$I_C = I_{CL}$; $V_{CL} = 350$ V $V_{IN} = 12$ V, See Figs 1, 2		1		μs
$E_{5/6}$	Second Breakdown Energy Clamped	$I_C = I_{CL}$; $V_{CC} = 12$V	300			mJ

Figure 1 : Test Circuit.

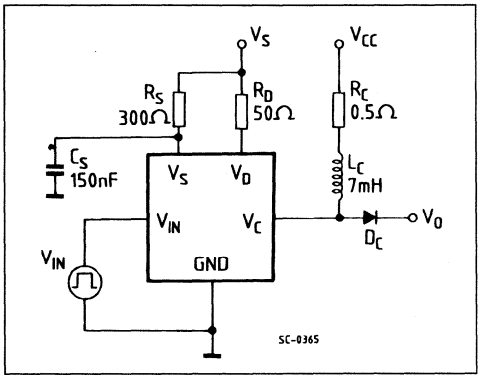


Figure 2 : Resistive Switching Waveform.

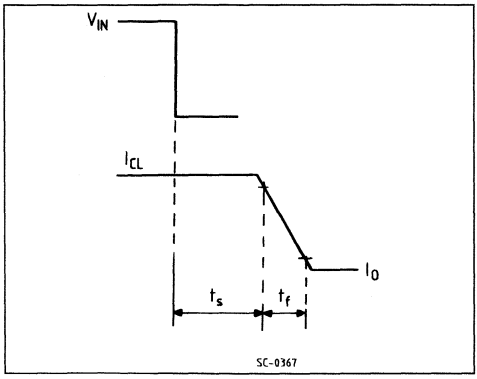
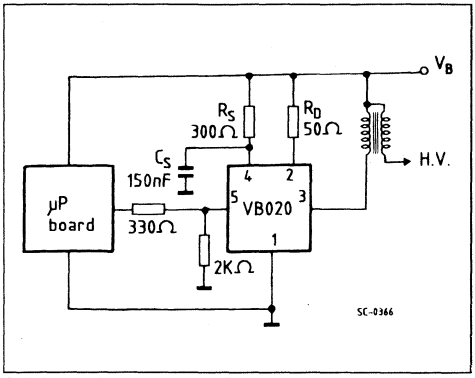
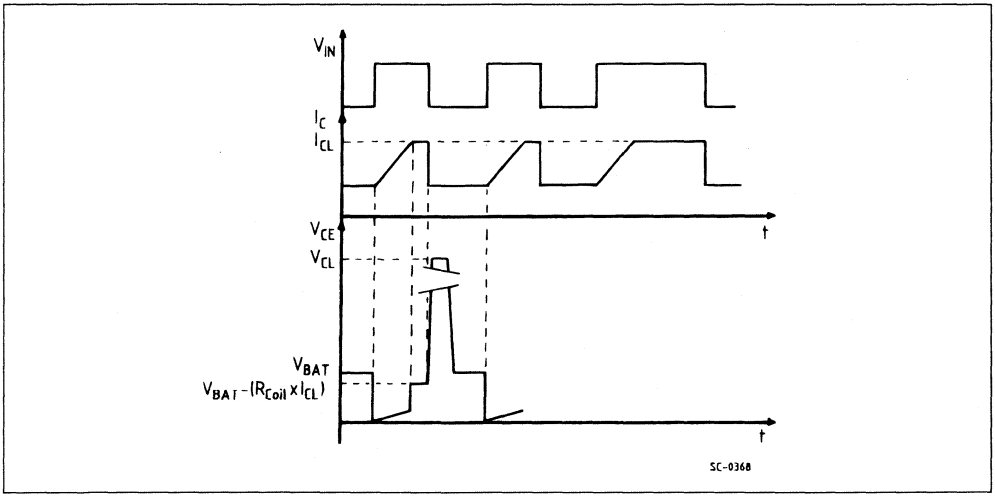


Figure 3 : Application Circuit.

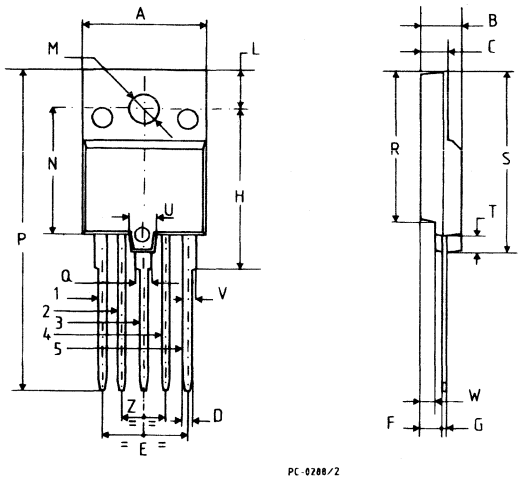


Coil data : primary resistance R_C = 0.4 - 0.5 ohm.
primary inductance L_C = 6 - 8 mH.

Figure 4 : Input Voltage and Output Current Waveform.



PACKAGE MECHANICAL DATA



	Dimensions			
	mm		Inches	
	Min.	Max.	Min.	Max.
A	15.8	16.2	0.622	0.637
B	5.35	5.65	0.210	0.222
C	3.3	3.8	0.130	0.149
D	0.85	1	0.033	0.039
E	10.16 Typ.		0.400 Typ.	
F	2.9	3.1	0.114	0.122
G	0.5	0.75	0.019	0.029
H	20.25	20.75	0.797	0.817
L	4.85	5.25	0.190	0.206
M	3.5	3.7	0.137	0.145
N	16 Typ.		0.630 Typ.	
P	35.4	36.4	1.393	1.433
Q	1.3 Typ.		0.051 Typ.	
R	19.1	19.9	0.752	0.783
S	22.8	23.6	0.897	0.929
T	2.1	2.3	0.082	0.090
U	3.1 Typ.		0.122 Typ.	
V	1.4 Typ.		0.055 Typ.	
W	1.88	2.08	0.074	0.081
Z	5.08 Typ.		0.200 Typ.	

The VB020 is a high voltage, power integrated circuit (P.I.C.) with a TTL/CMOS compatible input. The device intended for use as an interface between microprocessor and ignition coil in electronic ignition systems.

The input, Vin, of the VB020 is fed with a TTL/CMOS signal generated by an external controller or processor that determines both dwell time and ignition point. When vin is high (> 2.4V) the VB020 power output transistor conducts and a current controlled by the IC logic flows in the ignition coil. The current is held by the IC logic flows in the ignition coil. The current is held constant at a level set internally by the P.I.C. until the ignition point, when Vin is driven low. During the turn–off of the transistor, the primary voltage is clamped at an internally set value, Vcl, typically 415V, in case accidental secondary open circuit conditions occur.

The transition from saturation to desaturation coil current limiting phase implies a maximum overshoot of 0.85 times the supply voltage without requiring an external RC network for frequency compensation.

MULTIFUNCTION INJECTION INTERFACE

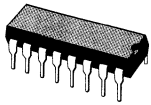
PRELIMINARY DATA

- DRIVES ONE OR TWO EXTERNAL DARLINGTONS
- DUAL AND SINGLE LEVEL CURRENT CONTROL
- SWITCHMODE CURRENT REGULATION
- ADJUSTABLE HIGH LEVEL CURRENT DURATION
- WIDE SUPPLY RANGE (4.75 - 46V)
- TTL-COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION
- DUMP PROTECTION

DESCRIPTION

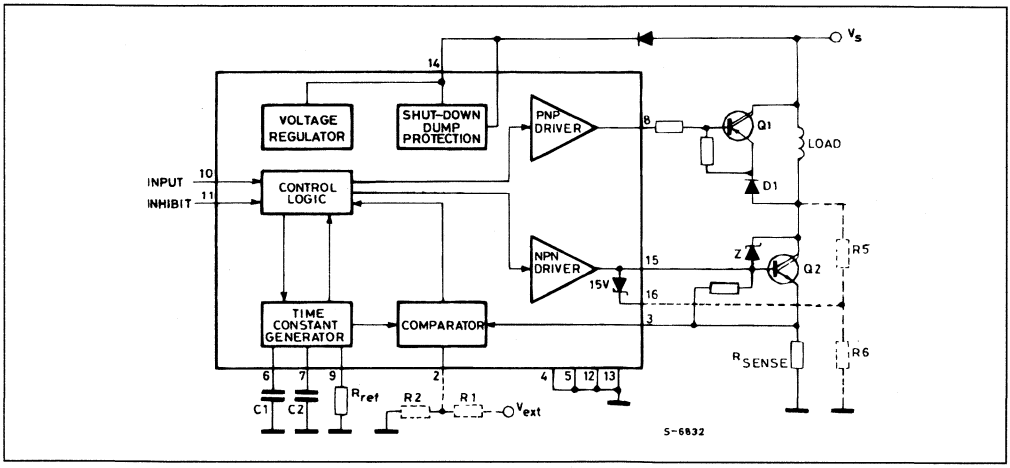
The L584 is designed to drive injector solenoids in electronic fuel injection systems and generally inductive loads for automotive applications. The device is controlled by two logic inputs and features switchmode regulation of the load current driving an external darlington and an auxiliary one for the current recirculation. A key feature of the L584 is flexibility. It can be used with a variety of darlingtons to match the requirements of the load and it allows both simple and two level current control. Moreover, the drive waveshape can be adjusted by external components. Other features of the device include dump protection, thermal shutdown, a supply voltage range of 4.75 - 46V and TTL-compatible inputs. The L584 is supplied in a 16 lead Powerdip package which uses the four center pins to conduct heat to the PC board copper.

DIP-16
(12 + 2 + 2)

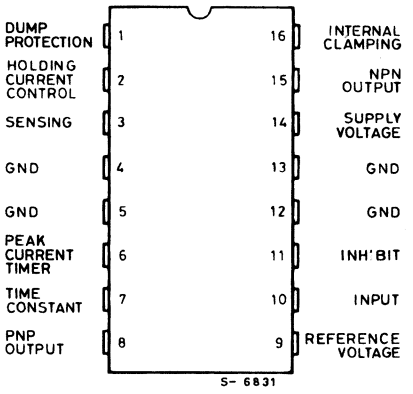


ORDER CODE : L584

BLOCK DIAGRAM



PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value
V_s	DC Supply Voltage (pin 1 open) Positive Transient Voltage (pin 1 connected to V_S, τ_f fall time constant = 100ms) (5ms ≤ t_{rise} ≤ 10ms, R_{source} ≥ 0.5Ω)	– 0.2V min ; + 50V MAX + 60V MAX
V_1	Input Voltage (pins 10, 11)	– 0.2V min ; + 7V MAX
V_r	External Reference Voltage (pin 2)	– 0.2V min ; + 7V MAX
V_{sens}	Sense Voltage (pin 3)	– 0.2V min ; + 7V MAX
V_8	Max D. C. and Transient Voltage	50V
I_r	Reference Current (pin 9)	5mA MAX
T_{stg}, T_j	Storage and Junction Temperature Range	– 55 to 150°C

THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W*

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

N°	Name	Functions
1	Dump Protection	With pin 1 connected to pin 14 the device is protected against dump voltage ≤ 60V. The protection operates at $V_s \geq 32V$ (typ.). If this protection is not used the pin must be left open.
2	Holding Current Control	The voltage V_{set} applied to this pin sets the holding current level.
3	Sensing	Connection for load current sense resistor. Value sets the peak and holding current levels. $I_p = 0.45/R_s$ (typ.) ; $I_h = V_{set}/R_s$. (see block diagram and fig. 4).
4	Ground	Ground Connection. With pins 5, 12 and 13 conducts heat to pc board copper.
5	Ground	See pin 4.
6	Peak Current Timer	A capacitor connected between this pin and ground sets the duration of the high level current (t_2 in fig. 4). If left open, the switchmode control of the peak is suppressed. If grounded, the current does not fall to the holding level.
7	Discharge Time Constant	A capacitor connected between this pin and ground sets the duration of t_{off} (fig. 4). If grounded, the current switchmode control is suppressed.
8	PNP Driving Output	Current sink for external PNP darlington (for recirculation). $I_{dp} = 35\ I_r$ (typ.).
9	Reference Voltage	A resistor connected between this pin and ground sets the internal current reference, I_r. The recommended value is 1.2kΩ, giving I_r = 1mA (typ.).
10	Input	TTL-compatible Input. A high level on this pin activates the output, driving the load.
11	Inhibit	TTL-compatible Inhibit Input. A high level on this input disables the output stages and logic circuitry, irrespective of the state of pin 10.
12 & 13	Ground	See Pin 4
14	Supply Voltage	Supply Voltage Input
15	NPN Driving Output	Current Source for External NPN Darlington (load driver). $I_{dn} = 100\ I_r$ (typ.)
16	Internal Clamping	Internal Clamp Zener for Fast Turnoff

ELECTRICAL CHARACTERISTICS (V_s (pin 14) = 14.4 V ; $-40 \leq T_j \leq 105$ °C ; R_{ref} = 1.20 kΩ unless otherwise noted ; refer to fig. 1)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Operating Supply Voltage	Pin 1 Open		4.75		44	V
		Pin 1 & 14 Connected		4.75		27	V
V_d	Dump Protection Threshold	Pin 1 = V_s		28		36	V
R_d	Dump Protection Input Resistance	Pin 1 to GND		18			kΩ
I_q	Quiescent Current	Pin 14				45	mA
V_I	Input Threshold Voltages	Pin 10 & 11	Low			0.8	V
			High	2.0			
I_I	Input Current	Pin 10 & 11	Low	– 100			µA
			High			– 250	
V_r	Reference Voltage	Pin 9		1.15		1.35	V
R_r	Reference Resistor Range	Pin 9 to GND $I_r = V_r/R_r$		1		3.3	kΩ
I_6	Peak Duration Control Current	Pin 6 $V_{pin\ 6} \leq 1.8V$		I_r / 9.50		I_r / 6.00	A
V_{6th}	Peak Duration Control Comparator Threshold	Pin 6		1.20		1.60	V
V_{6SAT}	Pin 6 Saturation Voltage	Pin 6 (discharge state)				200	mV
I_7	Off Duration Control Current	Pin 7 $V_{pin\ 7} \leq 1.8V$		$(I_{r\ min})$/ 9.50		$(I_{r\ MAX})$/6.00	A
V_{7th}	Off Duration Control Comparator Threshold	Pin 7		1.20		1.60	V
V_{7SAT}	Pin 7 Saturation Voltage	Pin 7 (discharge state)				200	mV
V_{spt}	Peak Current Threshold Voltage	Pin 3		400		500	mV
V_{set}	Holding Current Set Voltage Range	Pin 2		0		2	V
V_{set}	Holding Current Threshold Voltage	Pin 3, Peak Value, $dV/dt \leq 1V/_s$		V_{set} – 0.01		V_{set} + 0.01	V
I_3	Pin 3 Bias Current	$V_{pin\ 3}$ = 500mV		– 200			µA
I_2	Pin 2 Bias Current	$V_{pin\ 2}$ = 200mV		– 50			µA
V_{cl}	Recirculation Zener Clamping Voltage	Pin 16 to Pin 15 @ 200µA into Pin 16		13.5		18.5	V
I_{dn}	NPN Driver Source Current	$V_{pin\ 15}$ = 0V		70 x I_r		140 x I_r	A
I_{dp}	PNP Driver Sink Current	$V_{pin\ 8} \geq 4.75V$		25 x I_r		60 x I_r	A

APPLICATION INFORMATION

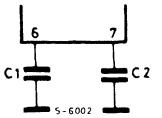
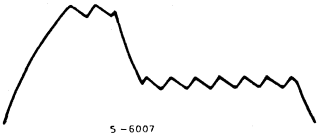
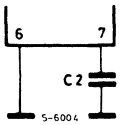
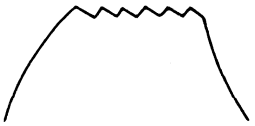
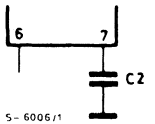
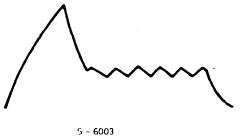
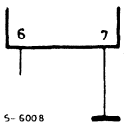
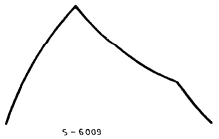
Controlled by a logic input and an inhibit input (both TTL compatible), the device drives the external darlington(s) to produce a load current waveform as shown in figure 4. This basic waveform shows that the device produces an initial high level current in order to ensure a fast opening, followed by a holding level current as long as the input is active. Both the peak and holding current are regulated by the L584's switchmode circuitry.

The duration of the high level current and the values of the peak and the holding currents can be adjusted by external components.

Moreover, by omitting C1, C2 or both it is possible to realize single-level current control, a transitory peak followed by a regulated holding current or a simple peak (figure 1).

The peak and holding current values are always

Figure 1 : Components Connected to Pins 6 and 7 Determine the Load Current Waveshape.

COMPONENTS ON PINS 6 AND 7	LOAD CURRENT WAVEFORM
	
	
	
	

referred, in the following formula, to I_E, emitter current of the external darlington Q2,

$$I_E = I_{LOAD} + I_{dn}$$

because the sensing detection is on the darlington emitter (not directly on the load).

The peak current level I_p, is set by the sensing resistor, R_S, and is found from :

$$I_p = 0.45 / R_S \text{ (typ)}$$

The peak value of holding current level, I_h, is set by a voltage (V_{set}) applied to pin 2, giving :

$$I_{hp} = V_{setth} / R_S = (V_{set} \pm 10mV)/R_S$$

The peak to hold current ratio is fixed by V_{set} :

$$I_p / I_{hp} = 0.45 / V_{setth}$$

V_{set} is fixed by an external reference and a voltage divider (V_{ext}, R1, R2 in fig 2) :
$V_{set} = V_{ext} * R2 / (R1 + R2)$

Due to the particular darlington storage time and the device reaction time not very significant differences can be found between I_p and I_h values based on the previous formula and the real values seen in the applications.

If the holding current function is not used, pin 2 cannot be left floating and it must be connected to GND.

Figure 2 : Application Circuit Showing the Optional Components. In particular it illustrates how the holding current level is adjusted independently of the peak current (with R1, R2, V_{ext}) and how the internal zener clamp is connected. This circuit produces the waveforms shown in Fig. 4.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
12	BDV64	BDV65

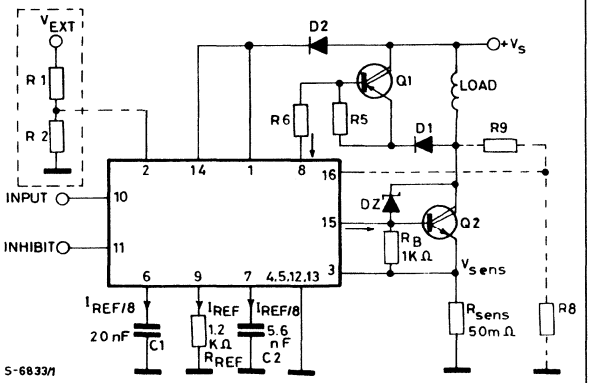
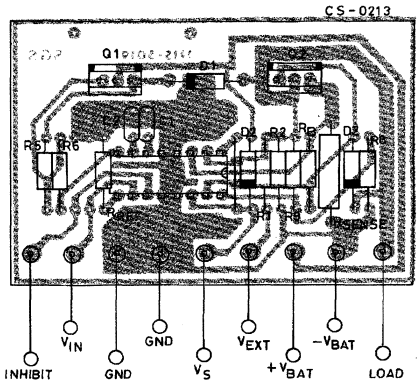


Figure 3 : P.C. Board and Components Layout of the Circuit of Fig. 2 (1 : 1 scale).



The drive current for the two darlingtons and the waveform time constants are all defined in turn by a resistor between pin 9 and ground.

The recommended value for I_r is 1mA which is obtained with a 1.2KΩ resistor. The darlington drive currents are given by :

PNP : $I_{dp} = 35\ I_r$ typ. NPN : $I_{dn} = 100\ I_r$ typ.

The duration of the high current level (t_2 in fig 4) is set by a capacitor connected between pin 6 and ground. This capacitor, C1 is related to the duration, t_2, by :

$$t_2 = C_1 \frac{V_{6th} - V_{6sat}}{I_6} = 12 \frac{C_1}{I_{ref}} \text{ (typ.)}$$

The discharge time constant (t_{off} in fig 4) is set by a capacitor C_2 between pin 7 and ground and is found from :

$$t_{off} = C2 \cdot \frac{V_{7th} - V_{7sat}}{I_7} = 12 \frac{C_r}{I_{ref}} \text{ (typ)}$$

Figure 4 : Waveforms of the Typical Application Circuit of Fig. 2.

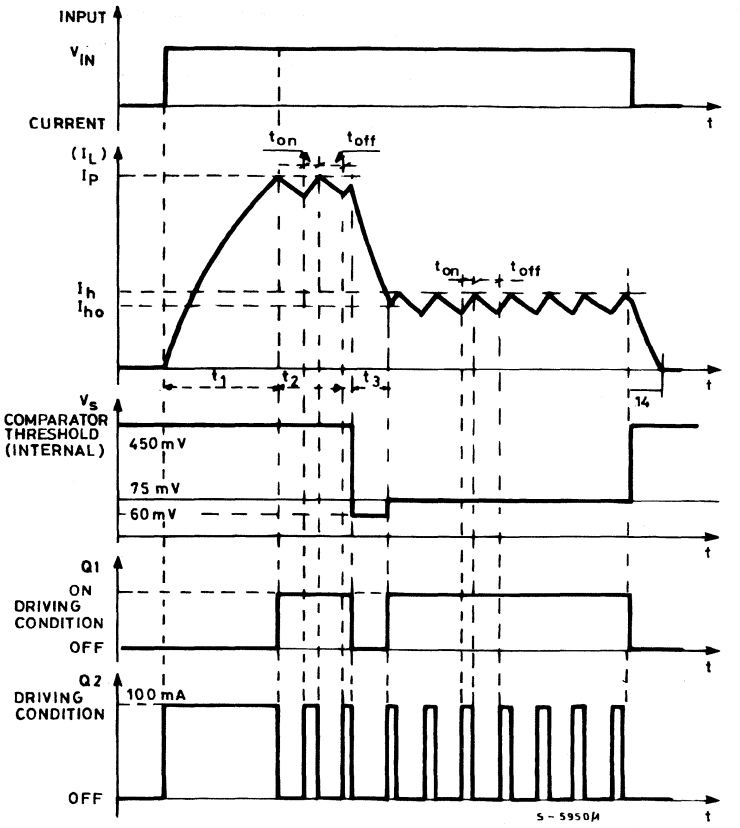
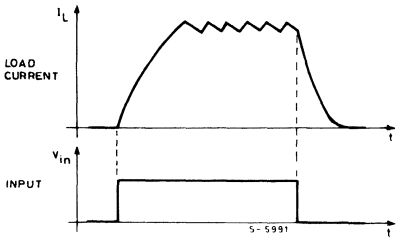


Figure 5 : When pin 6 is grounded, as shown here, the injector current is regulated at a single level.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65



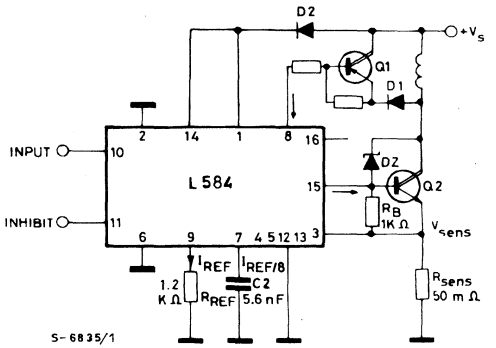
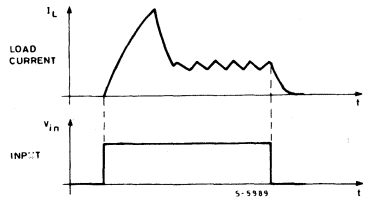


Figure 6 : In this application circuit, pin 6 is left open to give a single peak followed by a regulated holding current.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDX54	BDX53
16	BDW94	BDV65



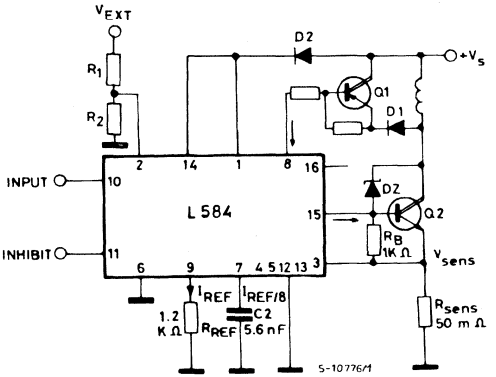
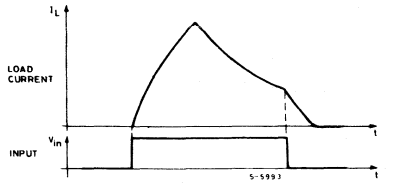


Figure 7 : Switchmode control of the current can be suppressed entirely by leaving pin 6 open and grounding pin 7. the peak current is still controlled.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65



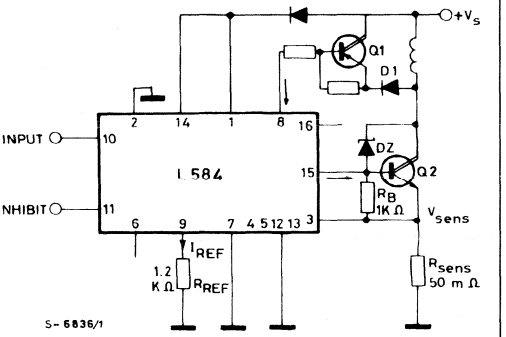
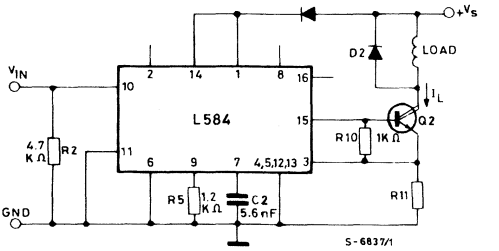
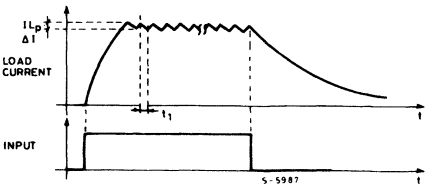


Figure 8 : Applications circuit using only one darlington with a single level of the injector current.





To have a very short off time when the L584 input goes LOW, an internal zener is available on pin 16. This zener is used with an external divider, R8, R9, as shown in figure 2. Suitable values can be found from :

$$V_{pin\ 16} \cong 15V + V_{BEQ2} + VRsense$$

$$V_{CQ2} \cong V_{pin\ 16} \cdot \frac{R9 + R8}{R8}$$

(V_{CQ2} is the voltage at the collector of Q2. V_{CQ2} max is 47V if the pin 8 is used for slow recirculation as in fig. 2).

To ensure stability, a small capacitor (about 200pF) must be connected between the base and collector of Q2 when pin 16 is used.

A different opportunity for a fast off time is based on the use of the external zener diode Dz. In this case also the maximum Dz voltage value is 47V.

LOAD DUMP PROTECTION

To protect the device against the positive load dump it is necessary to connect pin 1 to V_S. In this case, if V_S is higher than 32V, the device turns off Q_2 and turns on Q_1. The external resistor R_6 must be used (see application circuit) to avoid that pin 8 voltage exceeds 50V during load dump. R_6 must be :

$$R_6 > \frac{V_{DUMP} - V_8}{I_{dp}}$$

where V_{DUMP} is the dump voltage value and V_8 : $4.75V < V_8 < 47V$.

For this R_6 value, the minimum supply voltage V_{Smin} guaranteeing Q1 operation is given by :

$$V_{Smin} = R6 \left(\frac{Ip}{B_{Q1}} \quad (+2) \frac{V_{BEQ1}}{R_5} \right) + V_{8sat}$$

In relation to V_{Smin} it is no more verified $I_{dp} = 35\ I_{ref}$ (typ) even if the system correct operation is completely guaranteed.

The L584 application circuit suggested in these notes allows the use of inductive loads with the lowest possible series resistance (compatible with constructional requirements) and therefore reduces notably the power dissipation.

For example, an electronic injector driven from 14.4V which draws 2.4A has a series resistance of 6Ω and dissipates 34.56W. Using this circuit a injector with a 1Ω series resistance can be used and the power dissipation is :

$$P_d = R_L I_L^2 + V_D I_L (1 - \sigma) + V_{sat} \cdot IL\ \sigma + R_S\ I_L^2\ \sigma$$

where R_L = resistance of injector = 1Ω

V_D = drop across diode, $V_D \cong 1V$

V_{sat} = saturation voltage of Q2, ≅ 1V

R_S = R11 = 185mΩ

σ = duty cycle = 20%

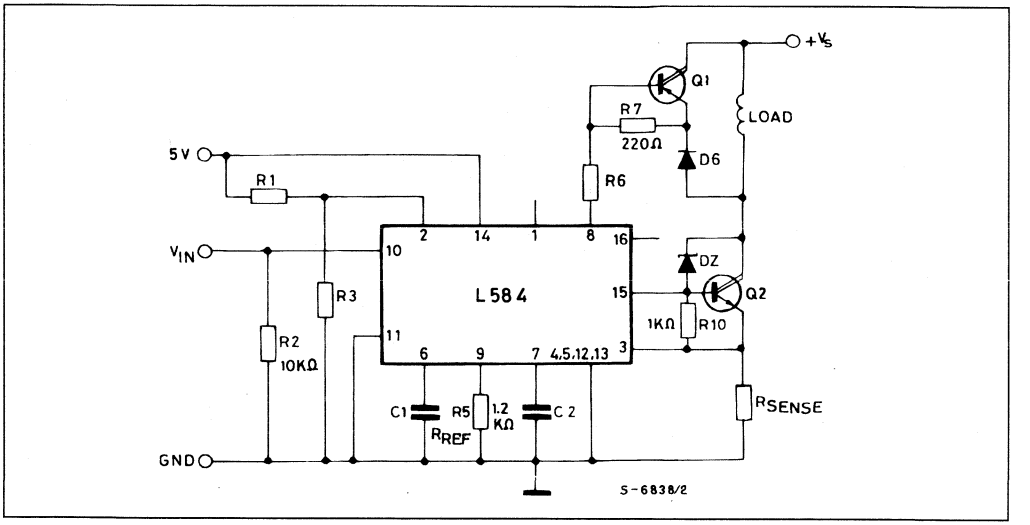
therefore :

$Pd \cong 5.76 + 1.92 + 0.48 + 0.21 = 8.37W$

This given two advantages : the size (and cost) of the injector is reduced and the drive current is reduced from 2.4A to about 0.4A.

The application circuit of figure 9 is very similar to figure 2 except that it shows the use of two supplies : one for the control circuit, one for the power stage.

Figure 9 : Application Circuit Showing How Two Separate Supplies Can Be Used.



In this application it is assumed that the 5V supply for L584 is taken from a logic supply, which is already protected, against load dump transients and vol-tage reversal.

Pin 1 must be left open, as shown in fig. 9, if V_S is always lower than 46V even during the voltage transients.

Note that t_{off} is also related to the required current ripple ΔI on the peak or on the holding current level by :

$$t_{off} = -L \ln \frac{(I_o - \Delta I) R_L + V_{off}}{I_o R_L + V_{off}}$$

Where : Io is the initial current value in OFF condition (equal to Ip or IH in accordance to the current level considered),

$$V_{OFF} = V_{DIODE} + V_{CEQ1}$$

R_L is the series resistance value of the inductance L :

Therefore C_2 can be dimensioned directly by :

$$C_2 = \frac{I_{REF} L}{12} \frac{\ln}{R_L} \frac{(I_o - \Delta I) R_L + V_{OFF}}{I_o R_L + V_{OFF}}$$

Note that t_{off} is the same for both the peak and holding current.

t_{on} time is given by :

$$t_{on} = \frac{L}{R} \ln \frac{V_{on} - R(I1 - \Delta I)}{V_{on} - RI1}$$

where : I1 is the final current value in ON condition (equal to I_p or I_H in accordance to the current level considered),

$$R = R_L + R_{SENSE}$$

$$V_{on} = V_S - V_{CE}satQ2$$

If the constant times are respectively

$$\frac{L}{R} 20\, t_{off} \quad \text{and} \quad \frac{L}{R} 20\, t_{on}$$

it is possible to consider a purely inductive load and therefore :

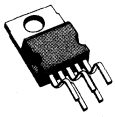
$$t_{off} = L \frac{\Delta I}{V_o} \; ; t_{on} = L \frac{\Delta I}{V_{on}}$$

SGS-THOMSON MICROELECTRONICS

L9335
L9336

INJECTOR DRIVER

- INTERNAL CURRENT SENSING
- PRECISION OUTPUT CURRENT LEVELS 2.4A/0.6A (L9335) AND 4A/1A (L9336)
- LOW OUTPUT SATURATION VOLTAGE 2.5V AT I_O = 1.5A (L9335) AND 3V AT I_O = 3A (L9336)
- MICROPROCESSOR COMPATIBLE INPUT
- DISABLE INPUT APPLICABLE FOR SWITCHING OFF DURING LOAD DUMP
- INTERNAL COMPENSATION
- INTERNAL SUPPLY STABILIZING ZENER DIODE



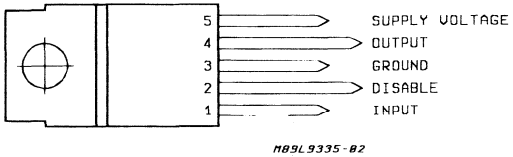
PENTAWATT

ORDER CODES : L9335
L9336

DESCRIPTION

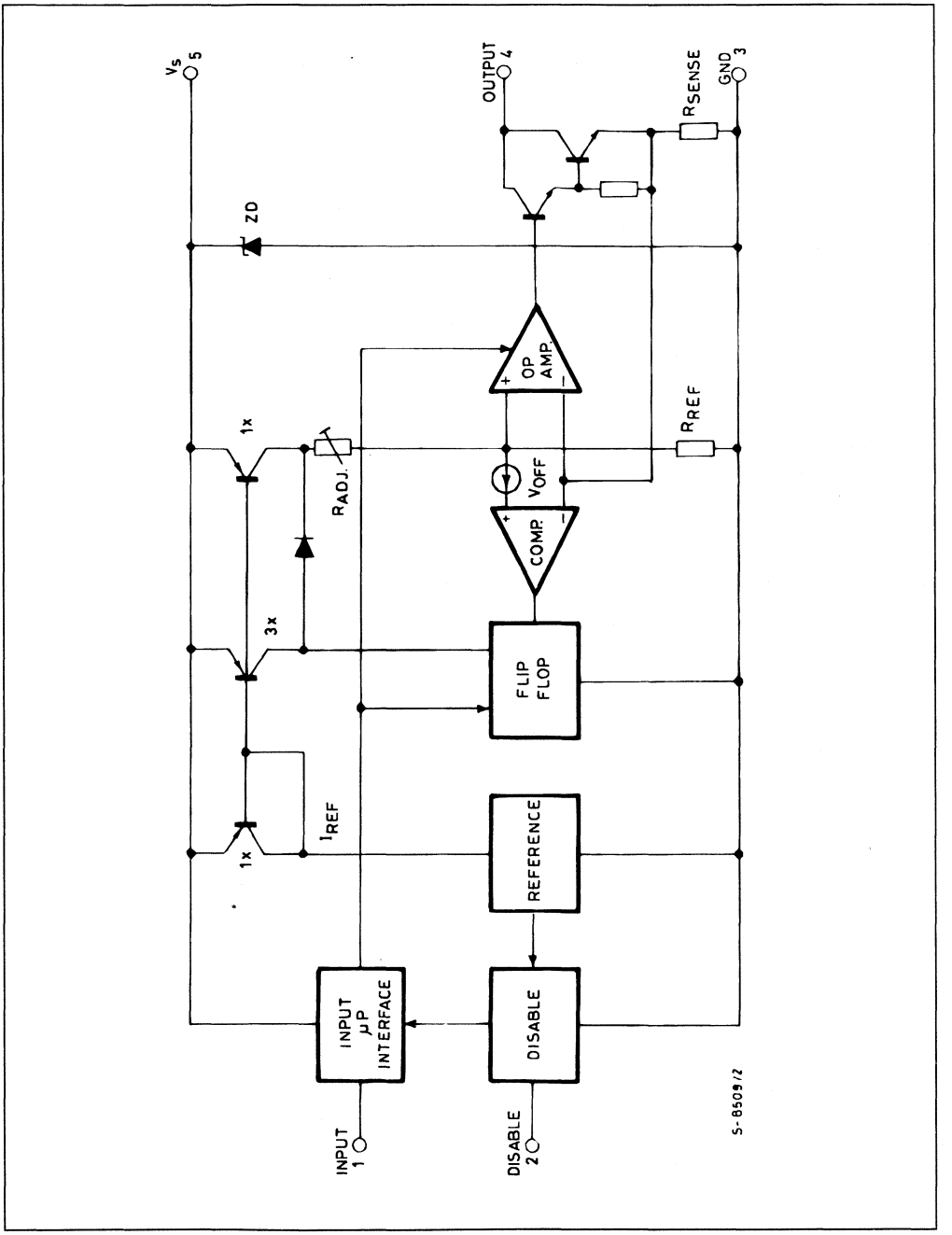
The L9335 and L9336 are monolithic integrated constant current sink drivers with internal current sensing and precision stable output current. The output current waveformfor inductive load with switching to the holding current level after the peak current level has been reached is fitted for driving fuel injectors.

PIN CONNECTION



M89L9335-82

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Pin 5 Voltage	min – 1	V
V_{IN}	Input Voltage	– 6 to 24	V
I_S	D.C. Supply Current	50	mA
	Pulse Supply Current (dump transient : 5 ms ≤ t_{rise} ≤ 10 ms, τ_f fall time constant = 100 ms)	150	mA
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

PIN DESCRIPTION

N°	Name	Functions
1	Input	A high voltage level at this pin activates the output sink stage.
2	Disable	Voltage at this pin higher than the disable threshold disables the output stage and resets the reference to the I_{OP} value.
3	Ground	Common Ground Terminal
4	Output	Open collector output of the current sink darlington transistor.
5	Supply	Internal zener diode between pin 5 and 3 stabilizes the supply voltage for the signal processing circuitry.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction Case	3	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 14.4 V ; – 40 °C ≤ T_j ≤ 125 °C unless otherwise specified)

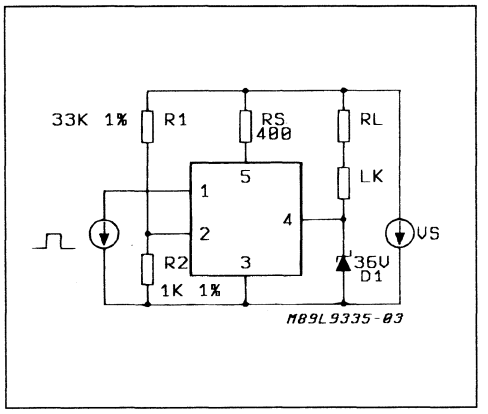
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{OP}	Output Peak Current (L9335) (L9336)	V_i = 5 V ; V_2 = 0	1.74 3.40	2.30 4.20	2.8 5.10	A
I_{OH}	Output Hold Current (L9335) (L9336)	V_i = 5 V ; V_2 = 0	0.51 0.95	0.6 1.10	0.69 1.30	A
V_{OS}	Output Saturation Voltage (L9335) (L9336)	I_O = 1.5 A ; V_i = 5 V I_O = 3 A ; V_2 = 0		1.0 1.5	2.5 3.0	V
I_{OL}	Output Leakage Current	V_i = 0 ; V_o = 17 V ; V_2 = 0			30	µA
BV_0	Output Sustaining Voltage	I_0 = 2 mA ; V_i = 0 ; V_2 = 0	42			V
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_I	Input Current	V_i = 2 V			200	µA
V_{2T}	Disable Input Thresh Voltage		1.10	1.5	1.90	V
V_{2H}	Disable Input Hyster.			50		mV
I_{DB}	Disable Input Bias Current		– 30		30	µA
V_{ZCL}	Supply Stabilizing Zener	I_S = 20 mA	6	7.5	9	V
I_Q	Quiescent Current	V_S = 5.5 V		2.5	10	mA

CIRCUIT OPERATION

L9335/6 are inductive load actuators particularly suited as automotive electronic fuel injectors, relays and solenoids drivers. The devices provide two driving output current levels : the peak and the holding current . During the switch on phase the output remains in saturation until the preset peak current, able to guaranteed the actuation (i.e. injectors opening), is reached : at this moment the internal reference is switched to the holding current value and the holding current is stabilized. In this way the injectors are held open and the load power dissipation is reduced.

The logical input, TTL compatible, in High status activates the output current sink stage.

Figure 1 : Application and Test Circuit.



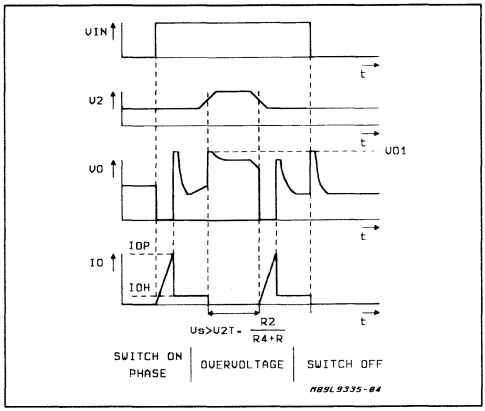
In the circuit in Fig. 1 the input voltage into the disable pin is :

$$V_2 = V_S \frac{R_2}{R_1 + R_2}$$

If overvoltage at VS causes the V2 to overcome the disable threshold, the output stage is switched off. After the supply voltage drops below the dump threshold (set with the R1, R2 ratio) the switch on phase takes place again if the input is still high.

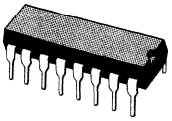
The switch off phase is characterized by the increase of the output voltage to the external clamping zener value as the output current when overvoltages occurs.

Figure 2 : Typical Waveforms.



QUAD INVERTING TRANSISTOR SWITCH

- OUTPUT VOLTAGE TO 50V
- OUTPUT CURRENT TO 1.2A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL SUPPRESSION DIODE



Powerdip (12 + 2 + 2)
ORDER CODE: L9222

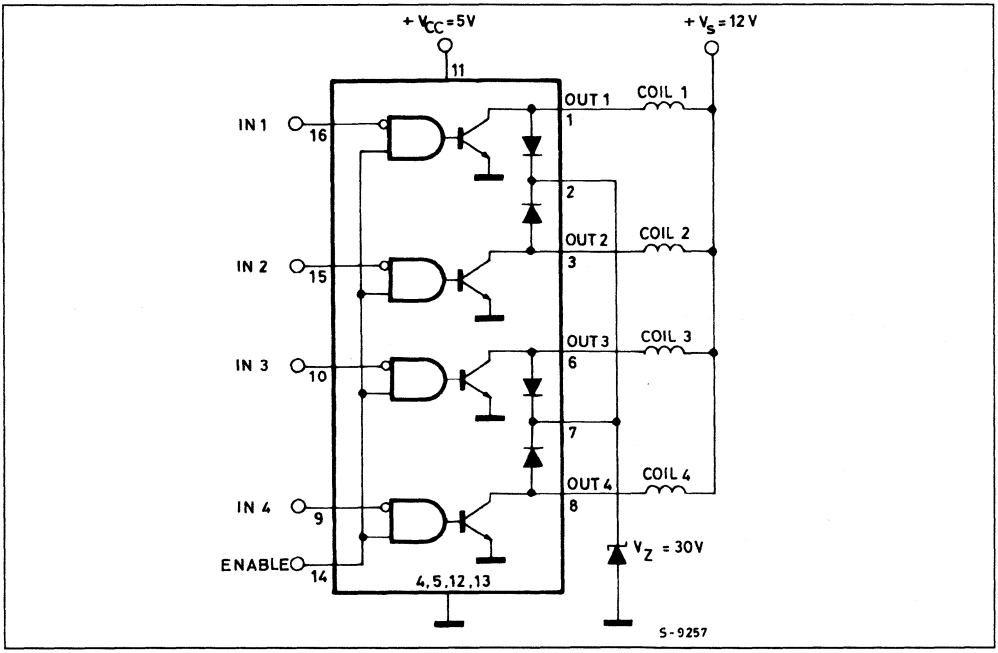
DESCRIPTION

The L9222 monolithic quad transistor switch is designed for high current, high voltage switching applications.

Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits. Each switch consists of an open-collector transistor plus a clamp diode for applications with inductive loads.

The emitters of the four switches are connected together to GND. The switches of the same device may be paralled. The device is intended to drive coils such as relays, solenoids, unipolar stepper motors, LED etc.

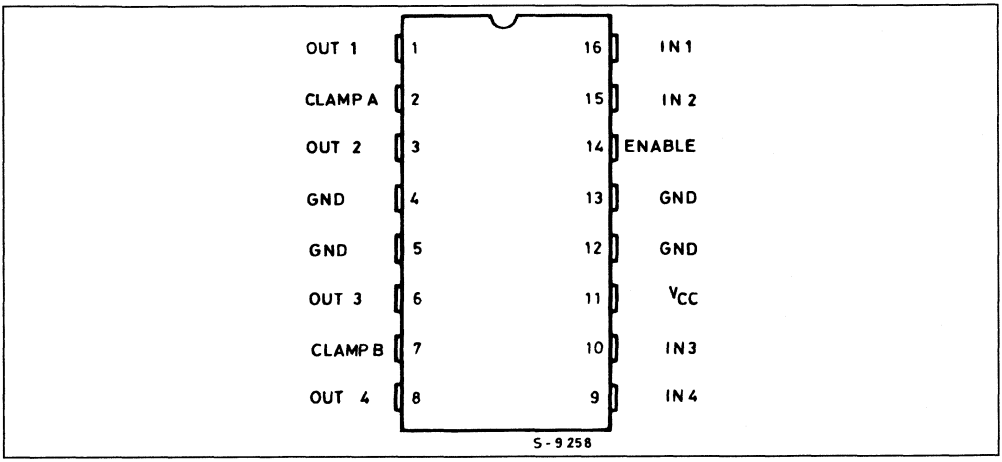
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{OUT}	Output Voltage	– 0.7 to 50	V
V_{CC}	Logic Supply Voltage	7	V
V_i	Input Voltage	– 0.7 to V_{CC} + 0.3	V
T_j, T_{ST}	Junction and Storage Temperature Range	– 55 to 150	°C

PIN CONNECTIONS (top view)



TRUTH TABLE

Enable	Input	Power Out
H	L	ON
H	H	OFF
L	X	OFF

For each input : H= High level
L= Low level
X = Don't care

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	90	°C/W
$R_{th\text{-}J\text{-}case}$	Thermal Resistance Junction-case	Max	14	°C/W

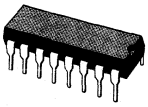
ELECTRICAL CHARACTERISTICS

(V_{CC} = 5Vdc ± 5% V_{EN} = 5V – 40 ≤ T_j ≤ 125°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CE(sus)}$	Output Sustaining Voltage	V_{IN} = 2V V_{EN} = 2V I_{OUT} = 100mA	46			V
I_{CEX}	Output Leakage Current	V_{CE} = 50V V_{IN} = 2V, V_{EN} = 0.8V			1	mA
$V_{CE(sat)}$	Collector Emitter Saturation	V_{IN} ≥ 0.8V; I_{OUT} = 0.1A			0.3	V
		I_{OUT} = 0.3A			0.5	
		I_{OUT} = 0.6A – 40 + 105°C			0.8	
V_{IL}	Input Low Voltage				0.8	V
I_{IL}	Input Low Current	V_{IN} = 0.4V	– 15			µA
V_{IH}	Input High Voltage		2.0			V
I_{IH}	Input High Current	V_{IN} ≥ 2.0V	– 15			µA
I_S	Logic Supply Current	All Outputs ON I_{OUT} = 06A		50	90	mA
		All Outputs OFF		10	20	mA
I_R	Clamp Diode Leakage Current	V_R = 50V Diode Reverse Voltage			100	µA
V_F	Clamp Diode Forward Voltage	I_F = 0.6A			1.8	V
		I_F = 1.2A			2.0	
I_{OUT}	Output Current	V_{IN} = 0.4V, V_S = 13V R = 10Ω	0.9	1.2		A
T_{PHL}	Propagation Delay Time (high to low transition)	T_j = 25°C I_L = 600mA			20	µs
T_{PHL}	Propagation Delay Time (low to high transition)	I_L = 600mA T_j = 25°C			20	µs
V_{ENL}	Low Enable Voltage				0.8	V
I_{ENL}	Low Enable Current	V_{EN} = 0.4V	– 15			µA
V_{ENH}	High Enable Voltage		2.0			V
I_{ENH}	High Enable Voltage	V_{EN} ≥ 2.0V	– 15		15	µA

DUAL HIGH CURRENT RELAY DRIVER

- HIGH OUTPUT CURRENT
- INPUT COMPARATOR WITH WIDE RANGE COMMON MODE OPERATION AND GROUND COMPATIBLE INPUTS
- INPUT COMPARATOR HYSTERESIS
- SHORT CIRCUIT PROTECTION OF OUTPUT TO 16V (for L9305) AND 12V (for L9305C)
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS
- INTERNAL OUTPUT OVERVOLTAGE CLAMPING
- SINGLE SUPPLY VOLTAGE (3.5V up to 18V)



POWERDIP
(8 + 8)

ORDER CODE : L9305
L9305C

DESCRIPTION

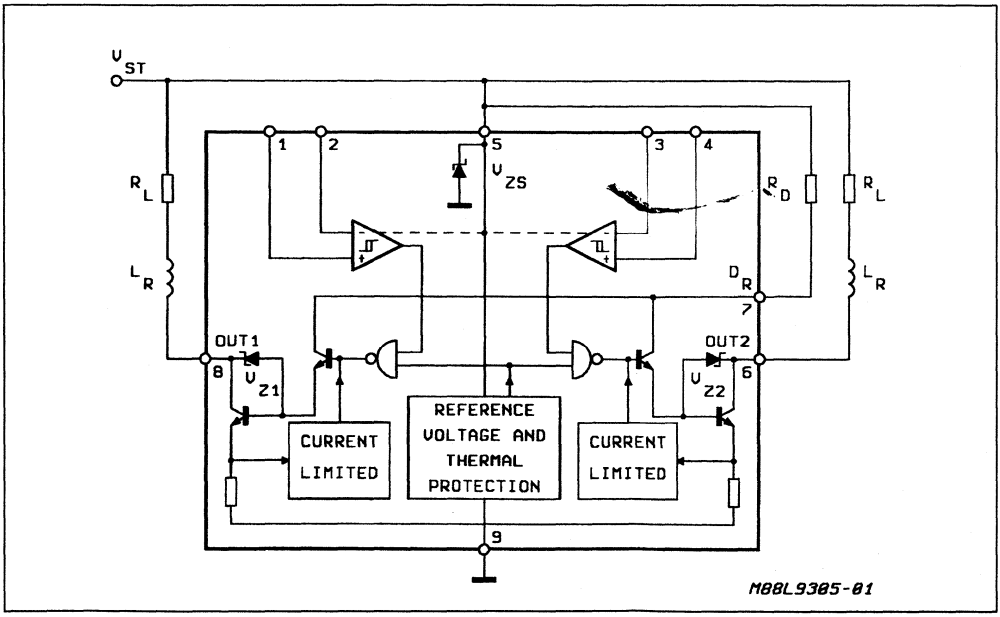
The L9305 and L9305C are a monolithic interface circuit with differential input comparator and open collector output able to sink high current specifically to drive relays, lamps, d.c. motors.

Particular care has been taken to protect the device against destructive failures - short circuit of outputs to Vs, output overvoltages, supply overvoltage.

A built in thermal shut-down switches off the device when the IC's internal dissipation becomes too high and the chip temperature exceeds the security threshold.

The input comparator hysteresis increases the interface's noise immunity, allowing the correct use in critical environments as automotive applications.

BLOCK DIAGRAM

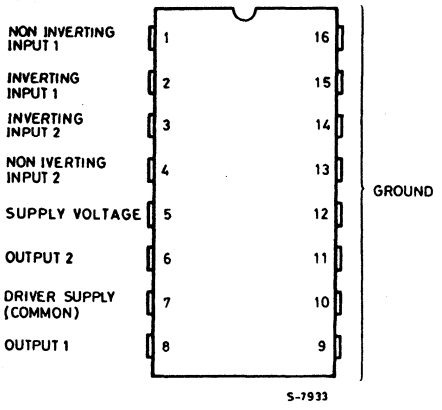


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_5	Supply Voltage	(*) 20	V
V_7	Driver Supply Voltage	26	V
I_{ZS}	Supply Zener Clamp Current (DC) (PULSED) (**)	30 80	mA mA
V_I	Comparator Input Voltage Range	– 0.2 to 24	V
V_I	Differential Input Voltage	24	V
T_j, T_{stg}	Junction and Storage Temperature	– 55 to 150	°C
V_{sc}	Max. Output Voltage in Short Circuit (L9305)	up to 16	V
V_{sc}	Max. Output Voltage in Output Short Circuit (L9305C)	up to 12	V
P_{tot}	Power Dissipation at T_{amb} = 85°C	928	mW
I_o	Output Current	Int. limited	

(*) The maximum allowed supply voltage without series resistors is limited by the built-in zener protection diodes.
(**) $T_{on} \leq 2.5$ ms ; repetition time ≥ 30 ms.

PIN CONNECTION (top view)



THERMAL DATA

$R_{thj\text{-}pins}$	Thermal Resistance Junction-pins	Max	15	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W

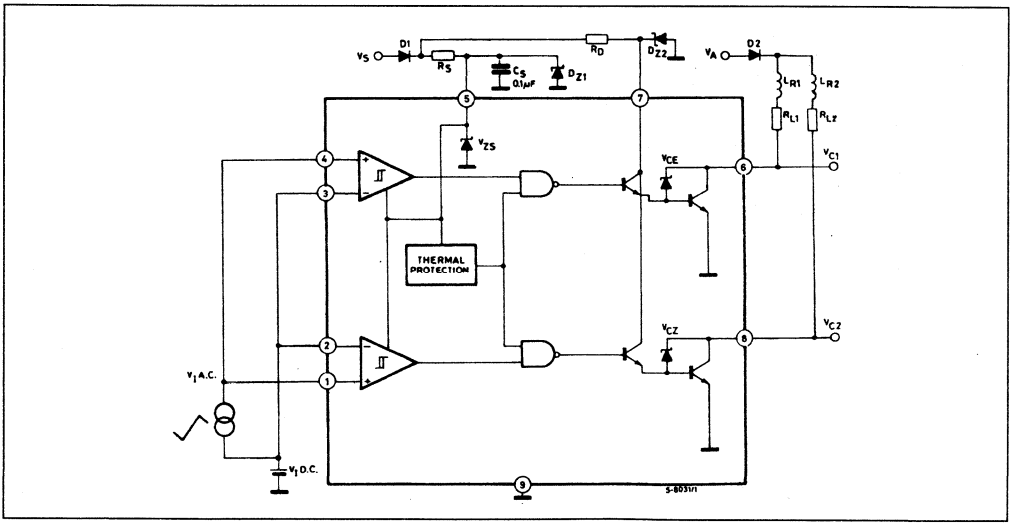
ELECTRICAL CHARACTERISTICS

(V_5 = 14.4V, T_{amb} = 25°C ; refer to block diagram unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_5	Supply Voltage		3.5		18*	V
I_S "st.by"	Supply Current	$V_I^+ - V_I^- \geq 70mV$ for **L9305**		5	8	mA
I_{SON}	Supply Current	$V_I^- - V_I^+ > 70mV$		18	30	
V_{CZ}	Output Clamping Voltage (for each channel)	I_{OUT} = 1A	20		27	V
V_{ZS}	Supply Voltage Clamp	I_{ZS} = 10mA	20		27	V
V_{IH}	Comparator Hysteresis	$V_I^+ - V_I^-$ = 200mVpp f = 1kHz	20		70	mV
I_B	Input Bias Current	$V^+ = V^-$ = 0V		0.2	1	µA
I_{OS}	Input Offset Current	$V^+ = V^-$ = 0V		± 20	± 200	nA
CMR	Input Common Mode Range	V_5 = 3.5V to 18V	0		V_5 – 1.6	V
I_{SC}	Output Short Circuit Current for Each Channel	$V_I^- - V_I^+ \geq 70mV$ for **L9305**	1.2	1.5	1.7	A
		for **L9305C**	1	1.5	2.3	
I_{CD}	Driver Transistor Current Capability	$V_I^- - V_I^+ \geq 70mV$ DC			300	mA
		Pulsed (**)			600	
V_{CSAT}	On Status Saturation Voltage	$V_I^- - V_I^+ \geq 70mV$ I_{CD} = 100mA			1	V
		I_{COUT} = 1.2A for **L9305**				
		I_{COUT} = 1A for **L9305C**				
I_{OL}	Output Leakage Current	$V_I^+ - V_I^- \geq 70mV$ for **L9305**			250	µA
		for **L9305C**			500	µA

* The maximum allowed supply voltage without limiting resistors is limited by the built-in protection zener diodes see V_{CZ}, V_{ZS} Spec. velues.
** $T_{ON} \leq 2.5$ ms ; repetition time ≥ 30 ms.

TEST AND APPLICATION CIRCUIT



APPLICATION INFORMATIONS (refer to application circuit)

D1 and D2 diodes are required only for reverse polarity protection.

If V_S is higher than V_{ZS} a resistor R_S is necessary to limit the zener current I_{ZS}. In order to determine R_S value the following equations can be used :

1) $$\frac{V_{SMAX} - V_{D1} - V_{ZSmin}}{R_S} < I_{ZS\ MAX}$$

2) $V_{S\ min} - V_{D1} - R_S \times I_{SON\ MAX}$ $V_{S\ min}$

where from $T_{amb} = 25°C$:

- $V_{S\ MAX}$ and $V_{S\ min}$ are the maximum and minimum values of power supply voltage
- V_{D1} is the forward diode D1 voltage drop
- $V_{ZS\ min} = 20V$
- $I_{ZS\ MAX} = 30mA$ for d.c. mode and $I_{ZS\ MAX} = 80mA$ for pulsed mode (see Absolute maximum ratings)
- $I_{SOM\ MAX} = 30mA$
- $V_{S\ min} = 3.5V$

If no R_S value can satisfy the system 1), 2) a more powerful external zener $D_{Z1} = 18V$ is required.

Then 1) becomes :

$$\frac{V_{S\ MAX} - V_{D1} - 18}{R_S} < I_{DZ\ MAX}$$

where $I_{DZ\ MAX}$ is the maximum allowed D_{Z1} current.

V_A voltage cannot be higher than 20V otherwise output overvoltage protection may be activated. Morever V_A must be less than 16V (for L9305) or 12V (for L9305C) if short circuit protection is required.

D_{Z2} = 22 to 24V is a mandatory for output 7 protection if V_S is higher than 26V.

MOUNTING INSTRUCTION

The L9305 and L9305C are assembled in the Powerdip package, in which 8 pins (from 9 to 16) are attached to the frame and remove the heat dissipated by the chip.

Figure 2 and 3 show two different heatsinking possibilities. In the first case, a PC board copper area is used as a heatsink (l = 65mm), while, in the second case, the device is soldered to an external heatsink. In both examples, the thermal resistance junction-ambient is 35°C/W.

Figure 2 : Example of Heatsink Using PC Board Copper (l = 65 mm).

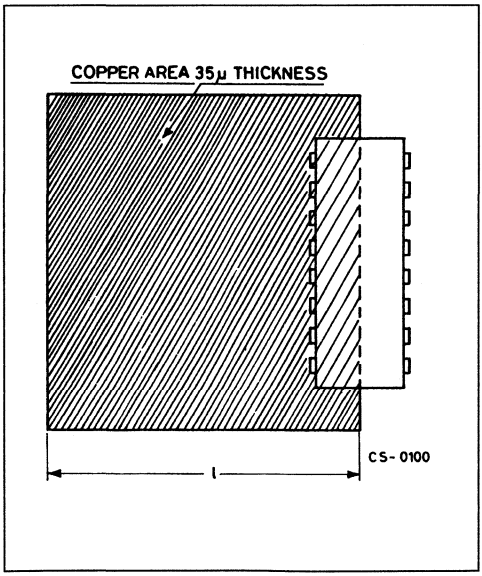
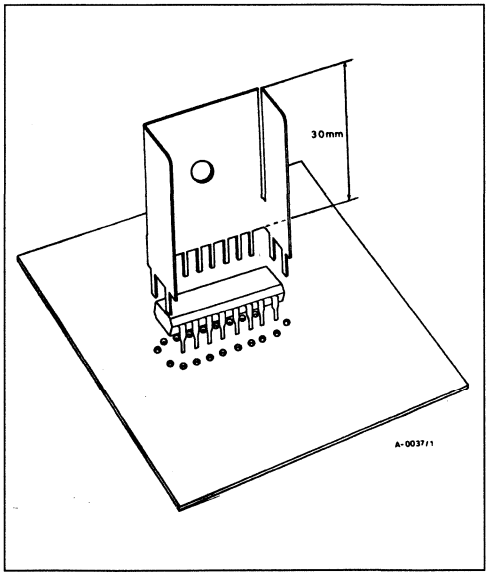


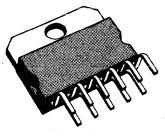
Figure 3 : Example of an External Heatsink.



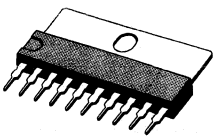
DUAL HIGH CURRENT LOW SIDE DRIVER

PRELIMINARY DATA

- HIGH OUTPUT CURRENT
- INPUT COMPARATOR WITH WIDE RANGE COMMON MODE OPERATION AND GROUND COMPATIBLE INPUTS
- INPUT COMPARATOR HYSTERESIS
- SHORT CIRCUIT PROTECTION WITH SOA PROTECTION OF OUTPUT
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS
- SINGLE SUPPLY VOLTAGE (3.5V to 28V)



MULTIWATT-11



SIP-10

ORDER CODES : L9307 (Multiwatt-11)
L9309 (SIP-10)

DESCRIPTION

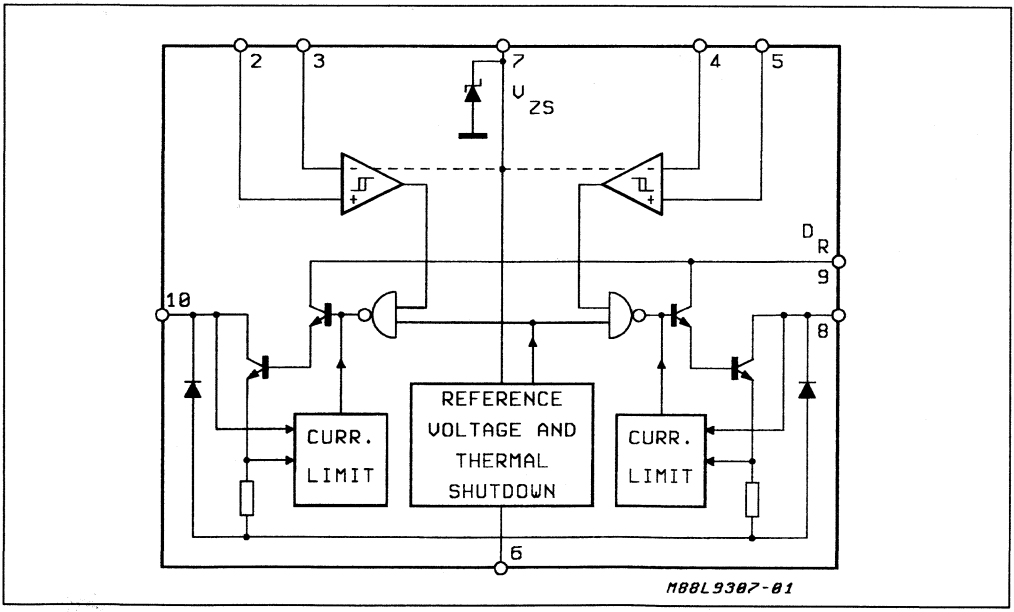
The L9307/9 is a monolithic integrated circuit with differential input comparator and open collector output able to sink high current specially to drive relays, lamps, d.c. motors.

Particular care has been taken to protect the device against destructive failures, i.e. short circuit of outputs to V_S, SOA protection, supply overvoltage.

A built in thermal shut-down switches off the device when the IC's internal dissipation becomes too high and the chip temperature exceeds security threshold.

The input comparator hysteresis increases the interface's noise immunity allowing the correct use in critical environments as automotive applications.

BLOCK DIAGRAM

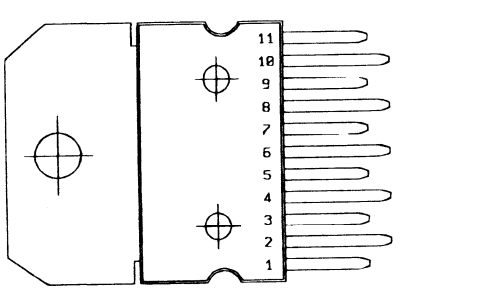


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
I_{ZS}	Current Into Supply Clamp Zener Diode	DC Conditions Pulsed : Ton < 2.5ms ; d < 8%	30 80	mA mA
V_S	Supply Voltage		28	V
I_O	Output Current		Internally Limited	°C
T_j, T_{stg}	Junction and Storage Temperature Range		– 55 to 150	°C
V_O 1, 2	Output Voltage		– 0.3 to 28	V
P_{tot}	Power Dissipation at T_{amb} = 85°C	for MULTIWATT-11	1.7	W
P_{tot}	Power Dissipation at T_{amb} = 85°C	for SIP-10	1.3	W

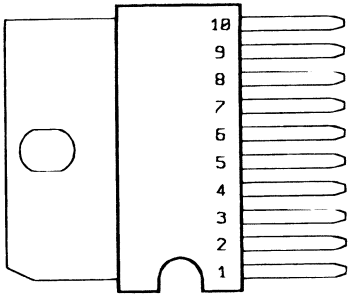
(*) TON 2.5ms ; repetition time ≤30ms
(**) The maximum allowed supply voltage without limiting resistor is limited by the built-in protection zener diode : see V_{ZS} spec. values.
If V_S is higher than V_{ZS} a resistor R_S is necessary to limit the zener current I_{ZS}.

PIN CONNECTIONS (top view)



M88L9307-02

N. C.
OUTPUT 1
COMMON DRIVER OUTPUT
OUTPUT 2
SUPPLY VOLTAGE
GND
NON INVERTING INPUT 2
INVERTING INPUT 2
INVERTING INPUT 1
NON INVERTING INPUT 1
N. C.



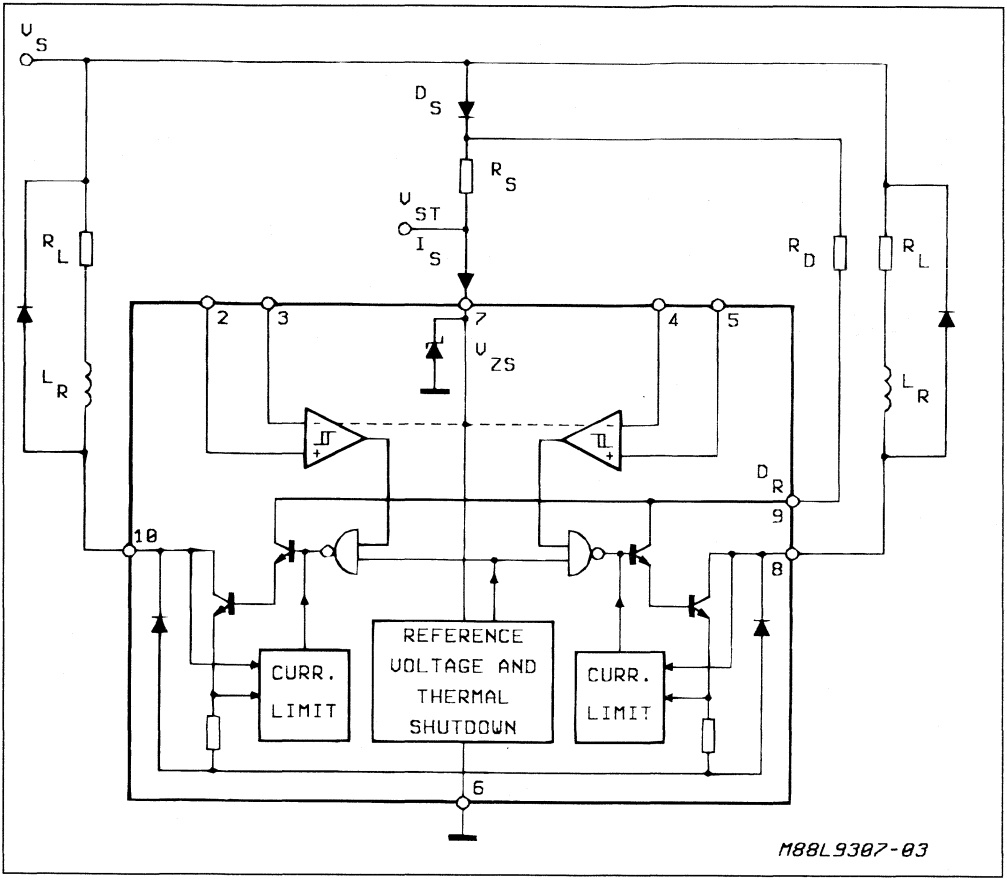
M88L9309-02

OUTPUT 1
COMMON DRIVER OUTPUT
OUTPUT 2
N. C.
SUUPLY VOLTAGE
GND
NON INVERTING INPUT 2
INVERTING INPUT 2
INVERTING INPUT 1
NON INVERTING INPUT 1

THERMAL DATA

			MULTIWATT	SIP-10	
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	38	50	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	10	°C/W

Figure 1 : Typical Applications.

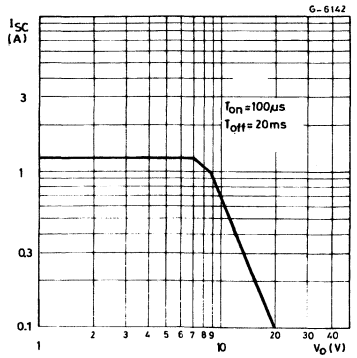


Note : a) R_S required only to limit I_{ZS} whenever V_S exceeds V_{ZS} voltage value.

ELECTRICAL CHARACTERISTICS (V_s = 14.4V ; T_{amb} = – 40°C to 85°C; R_S = 100Ω refer to block diagram unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Hysteresis of the Input Comparator	V_{in} = 200mV$_{PP}$; f = 1kHz	20		80	mV
I_B	Input Bias Current			0.2	1	µA
I_{OS}	Input Offset Current			± 50	± 400	nA
CMR	Input Common Mode Range	V_s = 6 to 18V	0		V_{ST} – 1.6	V
I_{SC}	Output Short Circuit Channel (typ SOA curve, see fig.2)	V_I^- – V_I^+ > 70mV V_{out} 1, 2 = 16V T_{amb} = 25 to 85°C T_{amb} = – 40 to 25°C V_{out} 1, 2 = 6V			 0.8 0.9 2.5	 A A A
I_D	Driver Transistor Curr. Capability	V_I^- – V_I^+ > 70mV V_S = 6 – 16V DC Conditions Pulsed : T_{on} = 2.5ms ; d < 8%			 300 600	 mA mA
I_o 1, 2	Output Current for Each Channel	(see fig.2) V_{out} 1, 2 < 2V ; V_I^- – V_I^+ > 70mV I_d = 100mA	1.5			A
V_{Csat}	On Status Saturation Voltage	V_I^- – V_I^+ > 70mV I_d = 100mA I_{out} 1, 2 = 1.2A			1.2	V
I_{OL}	Output Leakage Curr.	V_I^+ – V_I^- > 70mV V_S = 18V		10	250	µA
V_{st}	Supply voltage (pin 7)		3.5		18	V
I "st.by"	Supply Current	V_I^+ V_I^- > 70mV		5	8	mA
I"ON"	Supply Current	V_I^+ V_I^- > 70mV		18		mA
V_{ZS}	Voltage Clamp Supply Protection	I_{ZS} = 10mA	20		27	V

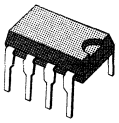
Figure 2 : SOA Protection.



DUAL LOW SIDE DRIVER

ADVANCE DATA

- DARLINGTON OUTPUT STAGE
- INPUT COMPARATOR WITH WIDE RANGE COMMON MODE OPERATION AND GROUND COMPATIBLE INPUTS
- INPUT COMPARATOR HYSTERESIS
- SHORT CIRCUIT PROTECTION OF OUTPUT WITH SOA PROTECTION
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS
- SINGLE SUPPLY VOLTAGE FROM 3.5V UP TO 28V



MINIDIP

ORDER CODE : L9308

DESCRIPTION

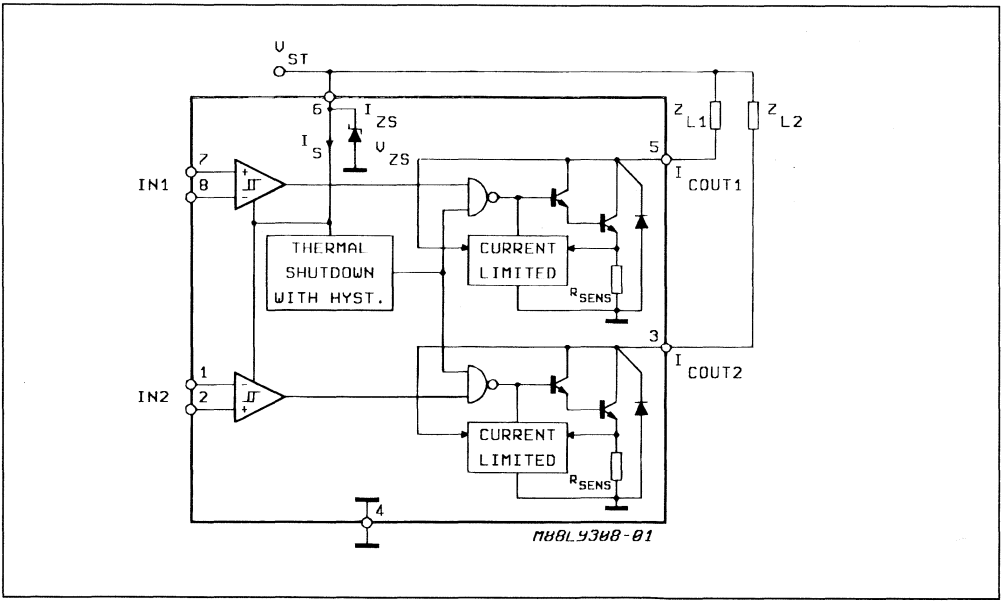
The L9308 is a monolithic interface circuit with differential input comparator and open collector output able to sink current specifically to drive lamps, relays, d.c. motors, electro valves etc.

Particular care has been taken to protect the device against destructive failures - short circuit of outputs to Vs, SOA protection, supply overvoltage.

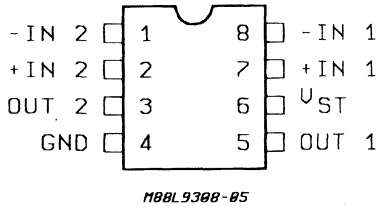
A built in thermal shut-down switches off the device when the IC's internal dissipation becomes too high and the chip temperature exceeds the security threshold.

The input comparator hysteresis increases the interface's noise immunity allowing the correct use in critical environments as automotive applications.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



M88L9308-05

1) -IN2 Inverting input2
2) +IN2 Non-inverting input2
3) OUT2 Output2
4) GND Ground
5) OUT1 Output1
6) V_{ST} Supply
7) +IN1 Non-inverting input1
8) -IN1 Inverting input1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
I_{SZ}	Current Into Supply Clamp Zener Diode	T_{amb} = 25°C, DC Pulsed (*)	30 80	mA mA
V_S	Supply Voltage		28	V(**)
I_O	Output Current		Internally Limited	
T_j, T_{stg}	Junction and Storage Temperature		– 55 to + 150	°C
P_{tot}	Power Dissipation at T_{amb} = 85°C		650	mW

(*) TON ≤ 2.5ms ; repetition time > 30ms.
(**) The maximum allowed supply voltage without limiting resistor is limited by the built-in protection zener diode : see V_{ZS} spec. values. If V_S is higher than V_{ZS} a resistor R_S is necessary to limit the zener current I_{ZS}.

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 14.4V ; – 40°C ≤ T_{amb} ≤ 85°C; R_S = 100Ω unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Hysteresis of the Input Comparater	V_{IN} = 200mVpp ; f = 1kHz	20		80	mV
I_B	Input Bias Current	$V_I^+ = V_I^- = 0$		0.2	1.0	µA
I_{OS}	Input Offset Current	$V_I^+ = V_I^- = 0$		± 50	± 400	nA
CMR	Input Common Mode Range	V_S = 6 – 18V T_{amb} = 25°C	0		V_{ST} – 1.6	V
I_{SC}	Output Short Circuit Current for Each Channel (see fig. ?)	$V_{IN} - V_{IN}$ > 70mV V_S = 16V T_{amb} = 25°C to 85°C T_{amb} = – 40°C to 25°C $V_{OUT\ 1,\ 2}$ = 6V			 0.5 0.6 1.2	 A A A
V_{CSAT}	On Status Saturation Voltage	T_{amb} = – 40°C to 25°C $V_I^- - V_I^+$ > 70mV $I_{OUT\ 1,\ 2}$ = 300mA T_{amb} = 25°C to 85°C		 1.0	1.5 1.4	V V
I_{OL}	Output Leakage Current	$V_I^- - V_I^-$ > 70mV V_S = 18V V_S = 5V		10	300 20	µA µA
V_{ST}	Supply voltage (pin 6)		3.5		18	V
$I_{-st.by-}$	Supply Current	$V_I^+ - V_I^-$ > 70mV		5	8	mA
I_{-ON-}	Supply Current	$V_I^- - V_I^+$ > 70mV		18		mA
V_{ZS}	Voltage Clamp Supply Protection	I_{ZS} = 10mA	20		27	V
I_{Omin}	Minimum Output Current with the Outputs connected Together	V_{CSAT} = 1.5V	400			mA
t_r t_f	Rise Time (see fig. 2) Fall Time	I_{OUT} = 50mA T_{amb} = 25°C			2 2	µs
t_{don} t_{doff}	Delay Time On Delay Time Off	I_{OUT} = 50mA T_{amb} = 25°C			10 10	µs

Figure 1 : Switching Time Test Circuit.

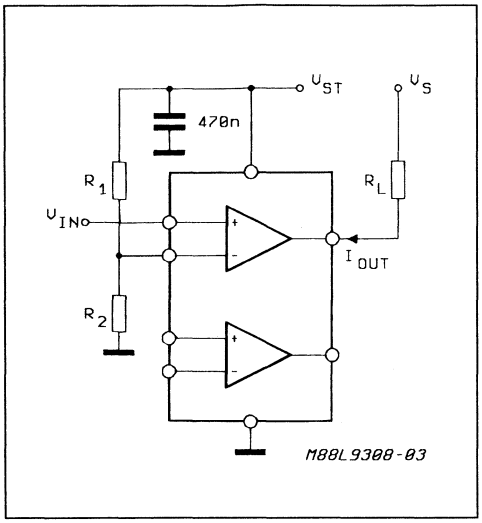


Figure 2 : Switching Time Waveforms for Resistive Loads.

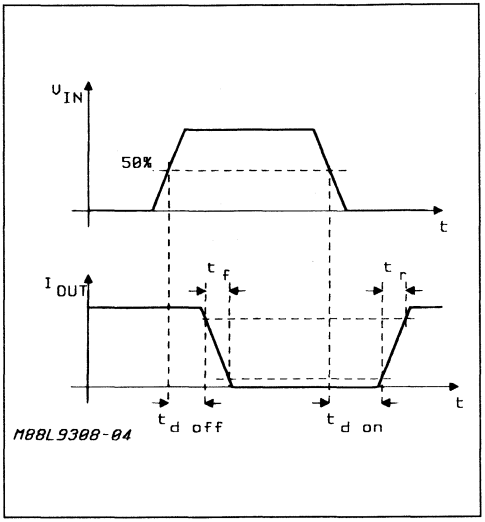
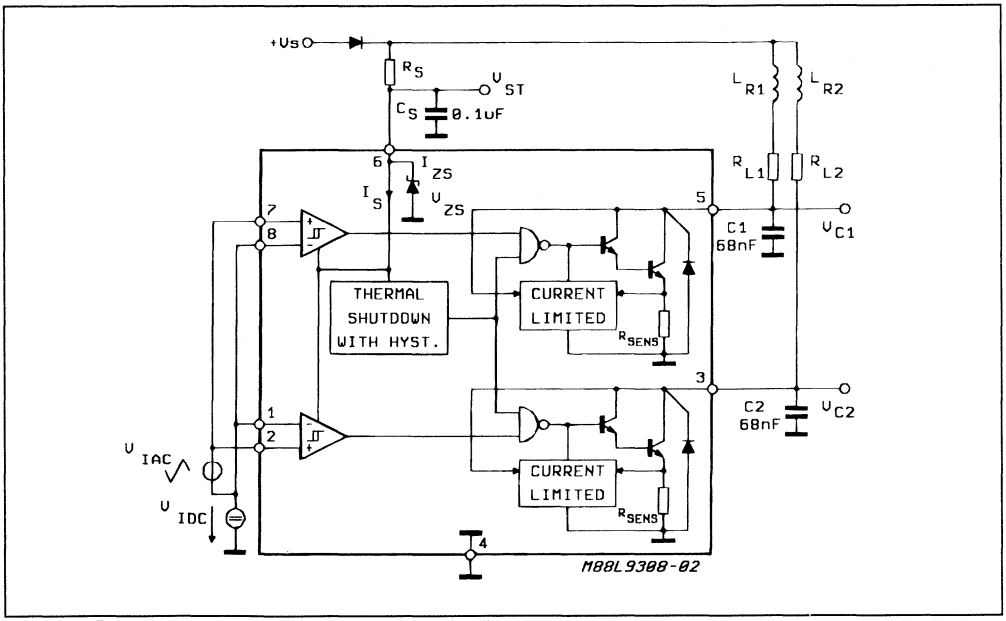
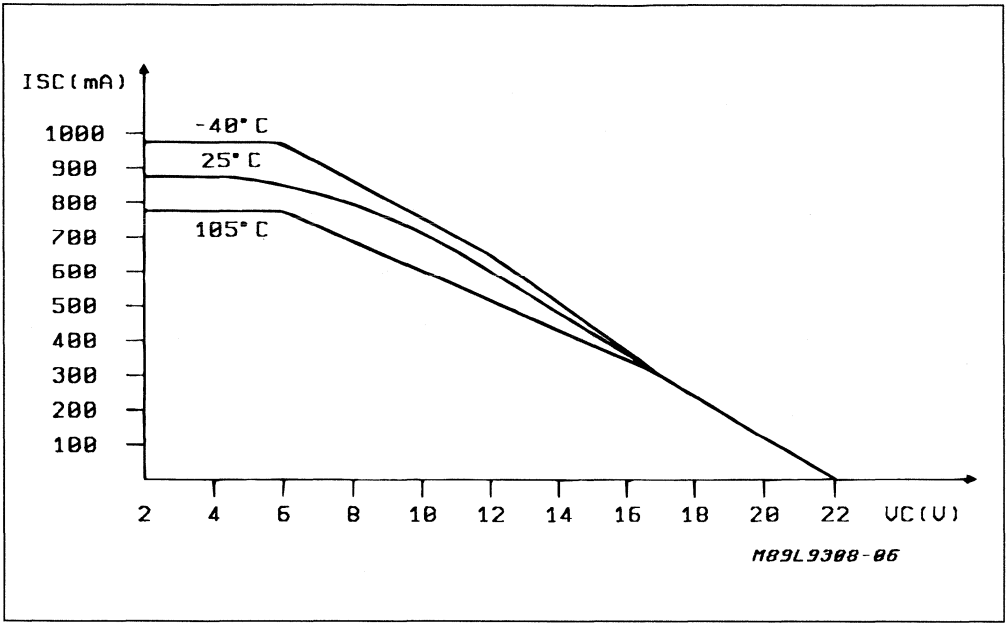


Figure 3 : Typical Application and Test Circuit.



Notes : a) R_S required only to limit I_{ZS} whenever V_S exceeds V_{ZS} voltage value.
b) C_1, C_2 cut high frequency gain during current limiting.

Figure 4 : Typical SOA Characteristic.



SGS-THOMSON MICROELECTRONICS

L9324

WINDOW LIFT CONTROLLER

ADVANCE DATA

- FOUR POWER OUTPUTS - UP TO 200 mA EACH ONE - FOR RELAIS DRIVING PROVIDED WITH INTERNAL RECIRCULATION
- TWO PROGRAMMING INPUTS FOR WINDOWS OPERATING MODE SELECTION
- ONLY TWO WIRES CONNECTING EACH KEYBOARD TO THE DEVICE
- WINDOW STATUS DETECTION BASED ON THE MOTOR CURRENT RIPPLE
- IGNITION KEY AND DOOR STATUS SENSING
- CLOCK FREQUENCY DEFINED BY AN EXTERNAL CAPACITOR
- ESD PROTECTION

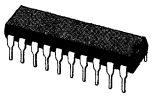
DESCRIPTION

The L9324 is a monolithic low side driver - realized with ST Multipower-BCD mixed technology - specially suited as window lift in automotive environment. The device drives four window motor control relais and it allows two possible window operating modes : the automatic (one touch) and the normal mode.

The window status (steady state, travel end) is checked by means of the ripple absence on the motor current.

The application circuit is able to withstand the load dump up to 80 V.

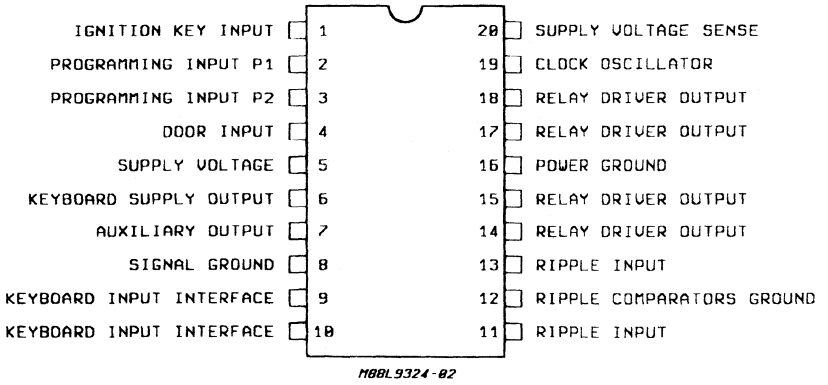
The device is assembled in 20 Lead Plastic DIP.



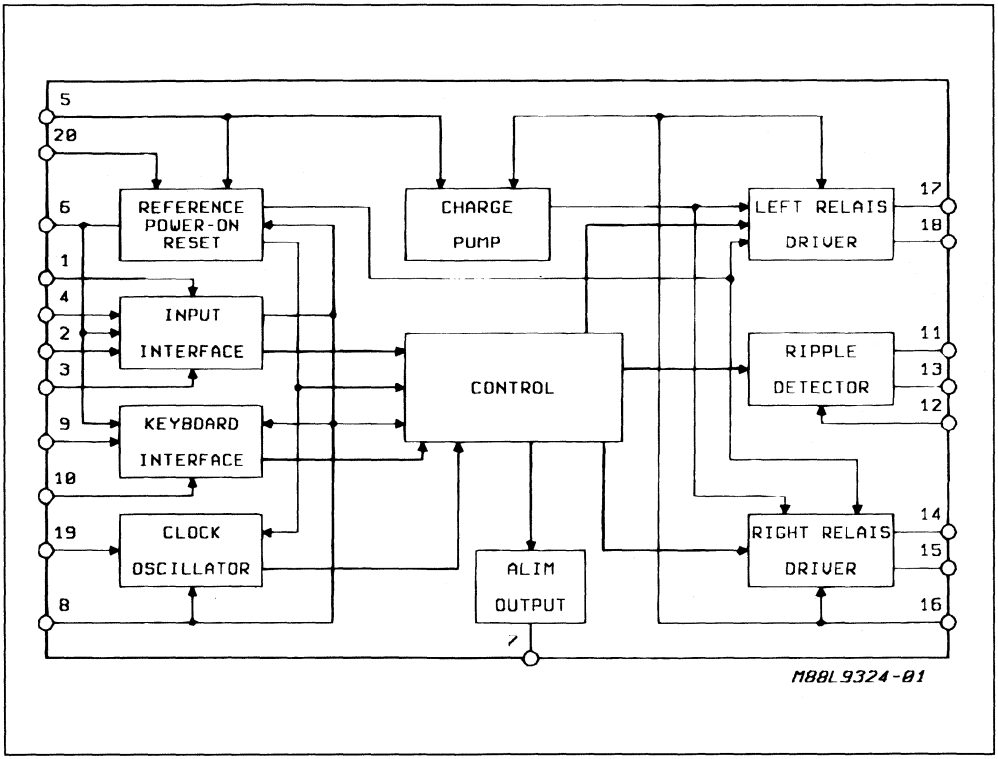
20 Lead Plastic Dip

ORDER CODE : L9324

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_5	D.C. Supply Voltage D.C. Reverse Supply Voltage	25 – 0.7	V V
$I_{14, 15, 17, 18}$	Max. Relais Driver Output Currents (in dump condition : V_{DUMP} = 80V 5ms ≤ t_{rise} ≤ 10ms) τ_f Fall Time Constant = 100ms $R_{SOURCE} \geq 0.5\Omega$	1	A
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

THERMAL DATA

$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	80	°C/W

ELECTRICAL CHARACTERISTICS (V_{BATT} = 14V, $-40°C \leq T_{amb} \leq 85°C$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_5	Operating Supply Voltage		8		16	V
I_{q5}	Quiescent Current (OFF condition)			1	2	mA
I_{q5ON}	Quiescent Current (ON condition)			30		mA
V_{OVth}	(pin 20) Overvoltage Protection Threshold (power output stage)		17	22	27	V
$V_{14,15,17,18}$	Relais Driver Output Saturation Voltage	$I_{14,15,17,18}$ = 200mA		0.7	1	V
V_{cz}	Internal Voltage Clamp at the Outputs (pin 14, 15, 17, 18)			26		V
$V_{11,13th}$	Ripple Detection Threshold			20	40	mV
I_{AUX7}	Auxiliary Output Source Current			20		mA
V_6	Keyboard Reference Voltage	$0 < I_6 < 100mA$	5.5	6.5	7.5	V
I_6	Keyboard Reference Output Current			100	120	mA
	Keyboard Input Comparator Threshold for					
	Pin 9 and Pin 10 S_1	V_6 = 6.5V	4.65	4.90	5.15	V
	S_2	V_6 = 6.5V	2.42	2.55	2.68	V
	S_3	V_6 = 6.5V	1.18	1.25	1.32	V
	S_4	V_6 = 6.5V	0.33	0.35	0.37	V
R_9, R_{10}	Comparator Input Resistances		50			KΩ
V_{2th}, V_{3th}	Programming Input Threshold Voltage			1.5		V
V_{1th}	Ignition KeyThreshold Voltage			1.5		V
V_{4th}	Door Input Threshold Voltage			0.5		V
T	Clock Period	C_{EXT} = 2.2nF	1	1.5	2	ms
t_{fd1}	Keyboard Filter Delay Time		16T		32T	ms
t_{fd2}	Door and Key Filter Delay Time		32T		64T	ms
t_{dabs}	Delay Time between the Ripple Absence and the Motor Stop		30T		36T	ms
t_{fd3}	Ripple Filter Delay Time at Motor Start-up		32T		48T	ms
t_{stup}	Start-up Delay Time		150T		182T	ms

FUNCTIONAL DESCRIPTION

PIN FUNCTIONS

1 - Ignition key input. This pin must be connected, through a resistor, to the ignition key ; in this way, at ignition key turn on (high level at pin 1), the full operating mode of the device is enabled. The a.m. resistor, together an internal zener, provides to protect this input in load dump condition ; recommended value for this resistor is 47 K.

2 and 3 - Programming inputs P_1 and P_2. These two pins allow to programme the device operation mode, according to the following truthtable :

P1	P2	Operating Mode
0	X	The device is programmed to work in a rear module. The automatic mode is disabled for both the windows. The high to low transition of a signal applied to pin 4 changes, in this operating mode, the status of the auxiliary output ; the device is enabled only at ignition key turn-on. The input P2 has no effect when P1 is low.
1	1	The device is programmed to work in a front module. The automatic mode is enabled for both the windows if the ign. key is on ; if the key is in off condition, the device works in traditional mode if one of the front doors is open, or it is disabled if both the front doors are closed.
1	0	In this case too the device is programmed to work in a front module. The operating mode is as for the last case but the automatic mode, when enabled, is possible only for the left window.

Note : a logic level 0 in the above table means the pin connected to ground ; a logic level 1 means the pin open ; X = don't care.

4 - Door input. This input senses the doors status (open or close) when the device is programmed to work in a front module. This pin must be connected, via an external resistor, to the door switch normally present on all the cars for the inside lamp. A low voltage level on this input means that the door is open (inside lamp on), an high voltage level means that the door is closed (inside lamp off). In the rear module this pin is connected to a push button which allows to enable and disable the module. The external resistor, together an internal zener, provides to protect the input against overvoltages ; recommended value for the external resistor is 4.7 K ohms.

5 - Supply voltage. This pin must be connected to the battery through a voltage limiter not to damage the device in load dump conditions (see the application circuit).

6 - Keyboard supply output. The voltage on this pin is about 4 V and the output current capability is 100 mA. An internal divider connected to this same voltage source generates the 4 thresholds for the keyboards interface input. This pin is connected to the two keyboards through two resistors (recommended value 220 ohms).

7 - Auxiliary output. This output, by an external transistor, drives the relay necessary to enable the rear keyboard when the device works in a rear module. The output current capability of this output is 20 mA.

8 - Signal ground.

9 and 10 - Keyboards input interfaces. This two pins are respectively connected to the left and to the right keyboard ; pushing one of the 4 pushbuttons of each keyboard a voltage is established on this pins. The device "understands", by this voltage level, which pushbutton has been pressed and execute the command. This concept allows to have many functions with a limited number of wires between the module and the keyboards. The voltage levels of the keyboards are then function of the pressed pushbutton as follow :

- traditional up.....3/4 * V_{pin6}
- automatic up.....1/2 * V_{pin6}
- traditional down.....1/4 * V_{pin6}
- automatic down.....0

The recommended values of the keyboards resistor necessary to have the a.m. values are respectively 470, 150 and 68 ohms (see schematic diagram).

11 and 13 - Ripple inputs. These inputs sense respectively the ripple of the right and the left motor through 2 decoupling capacitors connected to the sense resistors.

12 - Ripple comparators ground. This pin must be connected directly to the sense resistor ground, so to avoid bad operations of the ripple comparators.

14, 15, 17 and 18 - Relay driver outputs. These outputs control the relais to drive the window motors in the correct way. The 4 power devices are also switched on during the relais current recirculation and in overvoltage condition to protect themselves. In this way the device can withstand overvoltages up to 80 V (t = 300 msec), because the current flowing in the output power devices is limited by the relais resistance.

16 - Power ground. This pin is internally connected to the common power ground of the relay driver outputs.

19 - Clock oscillator. A capacitor connected bet-

ween this pin and ground set the clock frequency necessary for the correct operation of the internal logic. Recommended value for this capacitor is 2.2 nF.

20 - Supply voltage sense. This pin, connected by an external resistor to the battery supply voltage, allows the device to sense overvoltages ; in this condition, as said above, all the relay drivers are switched on to protect themselves.

APPLICATION INFORMATION

The L9324 can perform two possible window operating modes : the normal and the automatic mode. In the normal operating mode the window goes up or down until the keyboard push-button is pushed and the window is not stopped by obstacles. In the automatic mode, even after releasing the keyboard push-button, the window continues its movement that is interrupted if another push-button is pushed or by an obstacle. The window status (steady state, travel end) is detected by the absence of the ripple on the motor current. The delay time between the ripple absence and the motor switch off is about 50 ms. During the starting phase the motor is driven up to 250 ms even if the ripple is not present.

The complete window lift system using L9324 is based on two modules, one for the front windows and the other for the rear ones.

The possible operating modes, set by the programming inputs P_1 and P_2, are shown in the following diagram.

Figure 1 : Operating Modes.

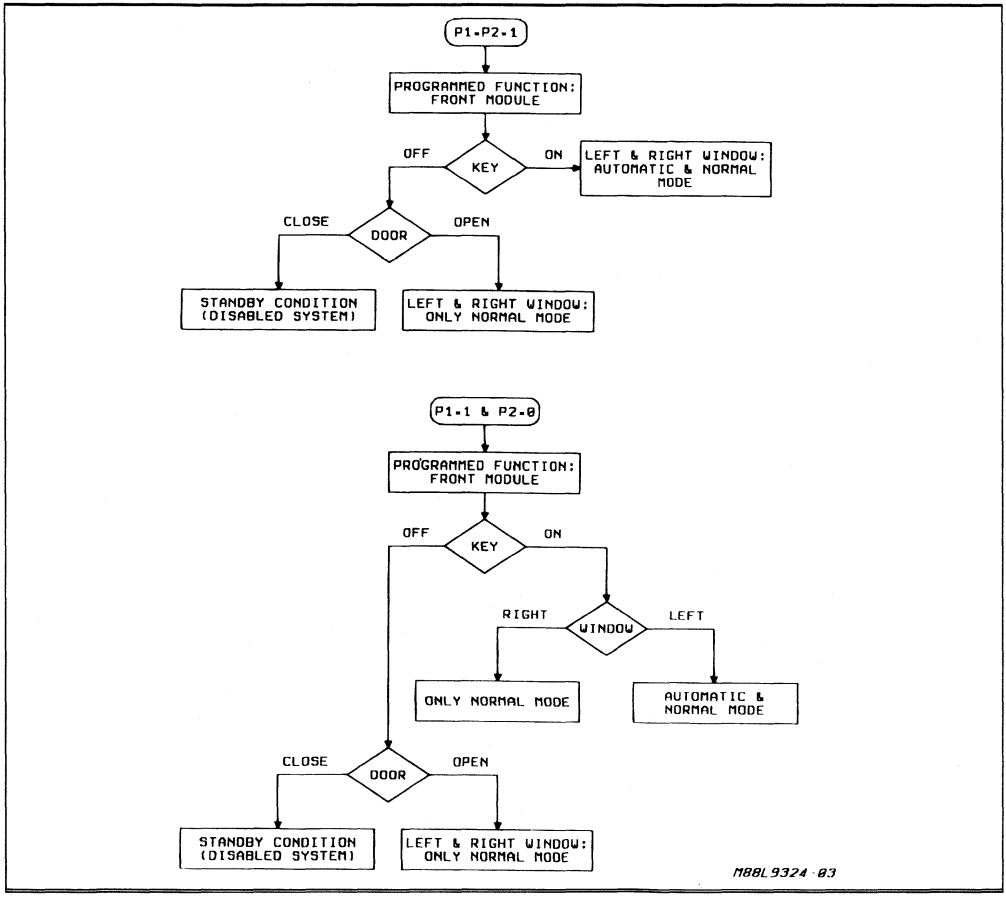


Figure 2 : Operating Modes.

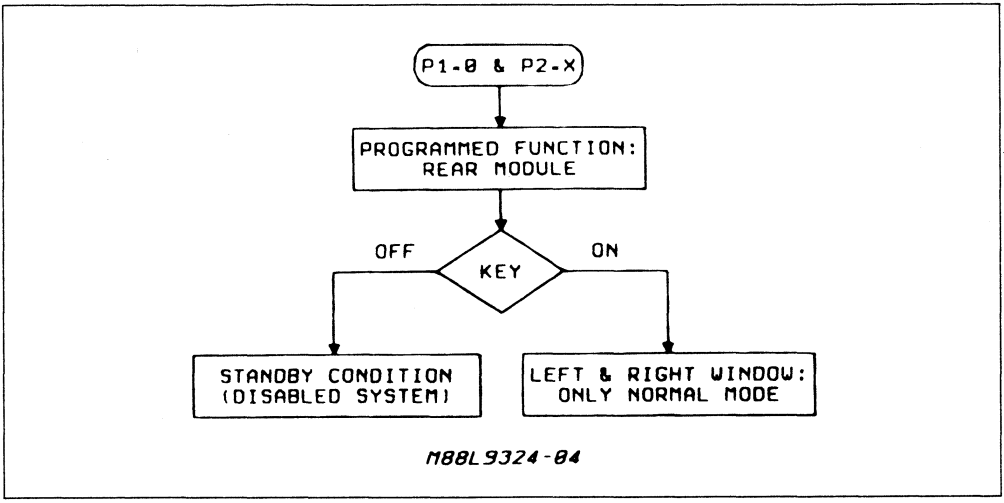


Figure 3 : Application Circuit.

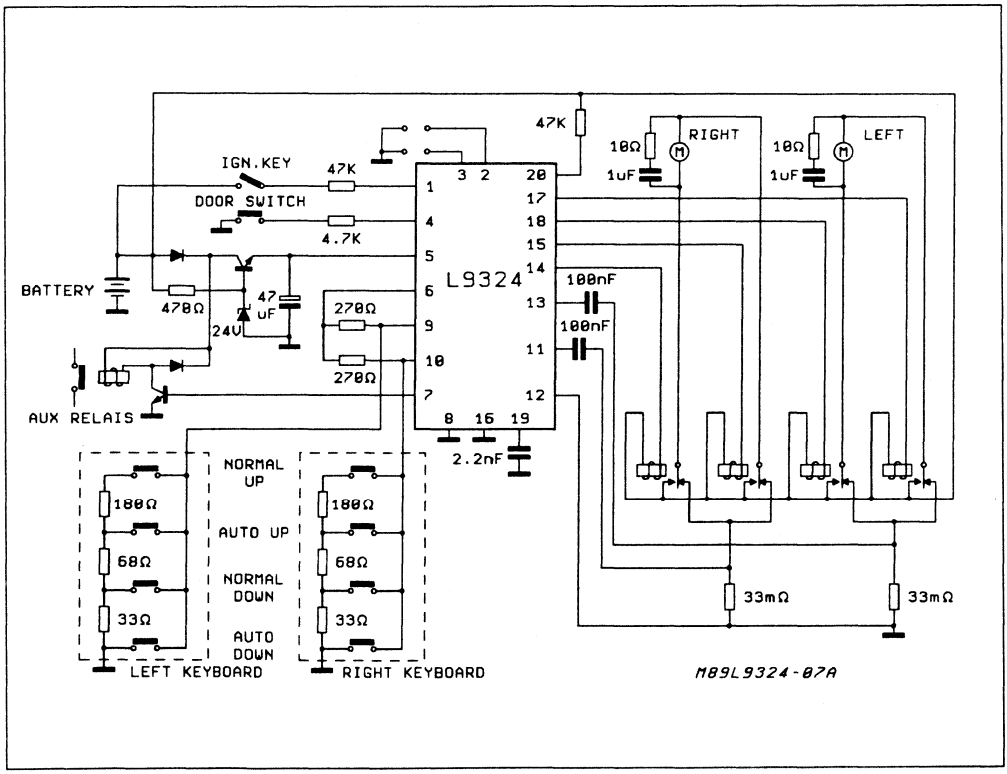
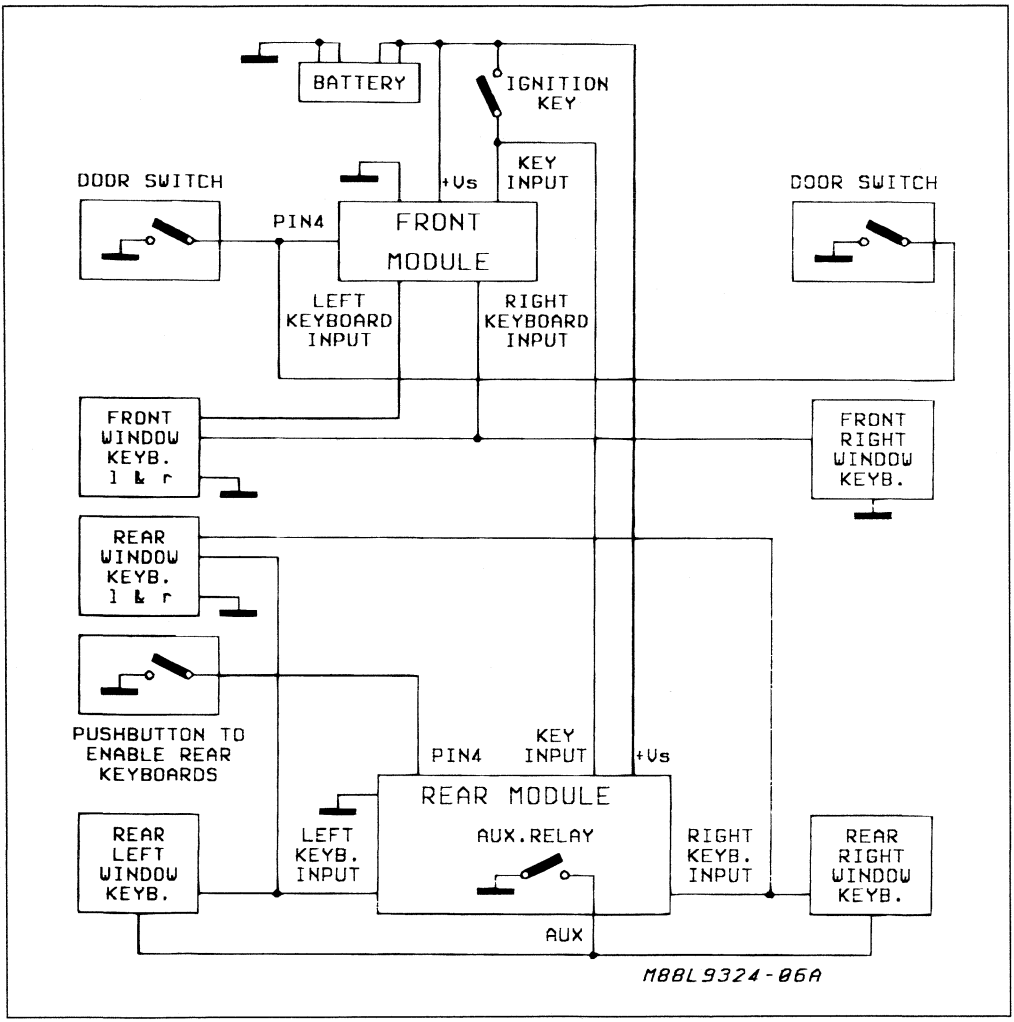


Figure 4 : Complete Window Lift System.



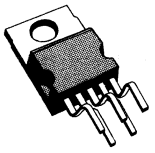
SGS-THOMSON MICROELECTRONICS

L9350

HIGH SIDE DRIVER

ADVANCE DATA

- LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUT
- WIDE SUPPLY VOLTAGE
- NO EXTERNAL COMPONENTS
- INTERNAL RECIRCULATION PATH FOR FAST DECAY OF INDUCTIVE LOAD CURRENT
- SHORT CIRCUIT PROTECTION
- FAILSAFE OPERATION : OUTPUT IS OFF IF THE LOGIC INPUT IS LEFT OPEN



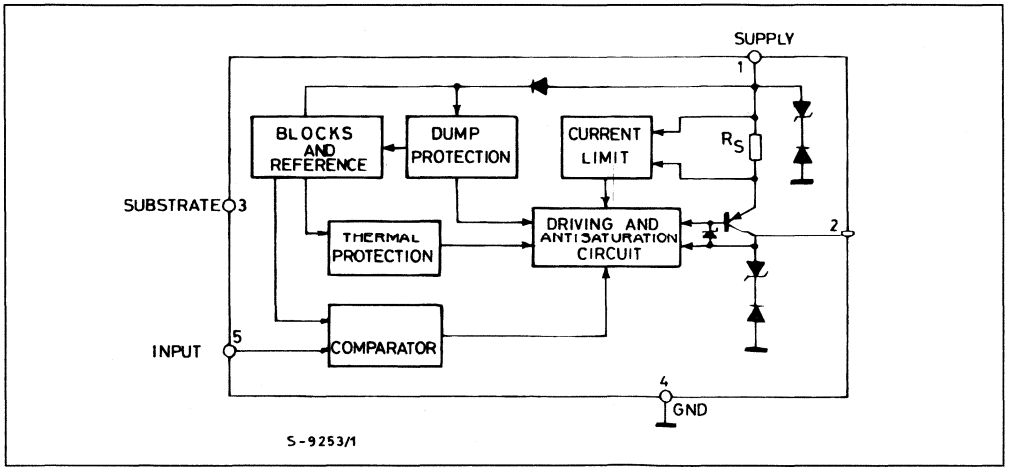
Pentawatt
ORDER CODE: L9350

DESCRIPTION

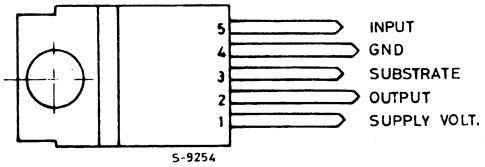
The L9350 is a monolithic integrated circuit designed to drive grounded resistive, inductive or mixed loads from the power supply positive side. Very low standby current (100/A typ.) and internally implemented protections against load dump and reverse voltages make the device very useful in automotive applications. No external components are required because the output recirculation clamping zener is included in the chip. This zener can withstand a recirculation peak current of 550mA on a 80mH/25 load.

The device is self-protected against overtemperature, overvoltage and overcurrent conditions. The L9350 operates over the full battery voltage range, from 4.5V (cold cranking) up to 24V (jump starting). The L9350 withstands revers battery conditions (- 13V) and supply voltage transients up to 100V limiting the maximum output transistor V_{EC} to 70V by an internal zener. ON and OFF delay times of 25/s max in any output status, including recirculating situation, allow PWM use of L9350.

BLOCK DIAGRAM



PIN CONNECTIONS (top view)



Note : Pin 3 must be left open or connected to ground.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	D.C. Supply Voltage	24	V
	D.C. Reverse Supply Voltage	– 13	V
	Load Dump : 5ms ≤ t_{rise} ≤ 10ms τ_f Fall Time Constant = 100ms, R_{source} ≥ 0.5Ω	60	V
	Low Energy Spikes : R_{source} ≥ 10Ω, t_{rise} = 1µs, tf = 2ms, fr Repetition Frequency = 0.2Hz	± 100	V
V_I	Input Voltage	– 0.3 to 7	V
I_O	Output Current	Internally Limited	
P_{tot}	Total Power Dissipation at T_{case} = 90°C	17.1	W
T_{JI} T_{stg}	Junction and Storage Temperature	– 55 to 150	°C

THERMAL DATA

$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	3.5	°C/W

ELECTRICAL CHARACTERISTICS

(V_S = 14.4V, – 40°C ≤ Tj ≤ + 125°C unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage		4.5		24	V
V_{IH}	Input Voltage High	4.5 < V_S < 24	2.0			V
V_{IL}	Input Voltage Low			1	0.8	
I_I	Input Current	0.8 < V_I < 5.5V		80	300	µA
I_{PL}	Output Leakage Current	V_O = 0V V_S = 24V V_I < 0.8V			1	mA
V_{sat}	Output Saturation Voltage	I_O = 125mA V_S = 4.5V		0.3	0.7	V
		I_O = 225mA V_S = 14.4V		0.5	0.8	V
		I_O = 550mA V_S = 14.4V		0.7	1.1	V
I_{SC}	Output Short Circuit Current		0.6	1.5		A
I_Q	Quiescent Current	V_I > 2V		50	100	mA
		V_I < 0.8V Stand-by Condition		100	200	µA
V_{ZO}	Negative Output Zener Voltage	R_L = 25Ω L = 80mH on V_I Transition from "1" to "0"	– 36	– 30	– 24	V
T_{on}	Turn ON Delay	Resistive Load R_L = 25Ω, T_j = 25°C (fig.2)			20	µs
T_{off}	Turn OFF Delay				25	µs
T_{dc}	Turn On Delay While Output is Clamped	R_L = 25Ω L = 80mH Any Time During Internal Clamping (fig.3)			20	µs

Figure 1 : Typical Automotive Application Circuit.

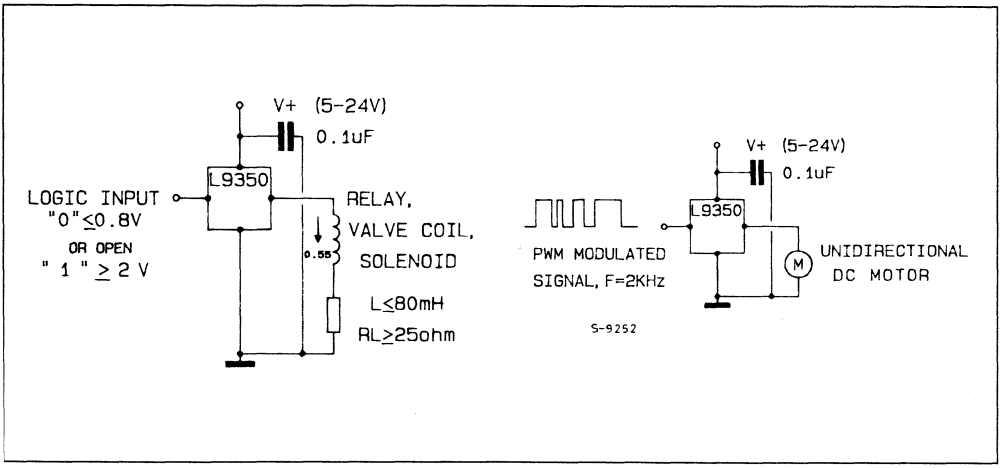


Figure 2 : Resistive Load.

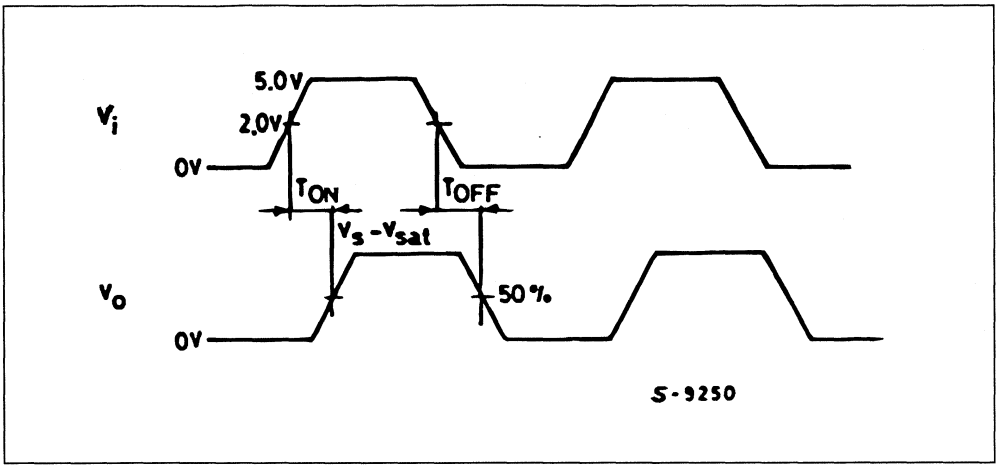
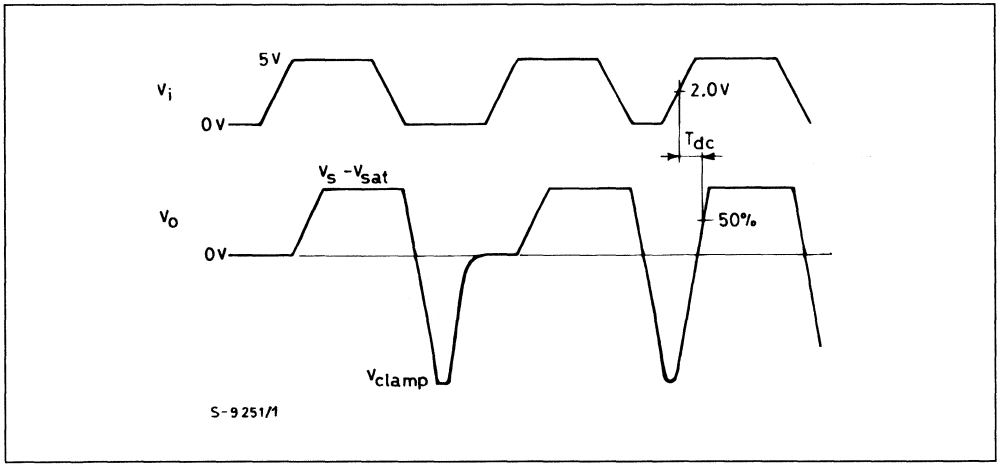


Figure 3 : Inductive Load.



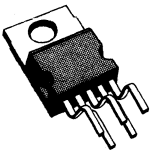
SGS-THOMSON MICROELECTRONICS

L9355

6A SWITCHMODE HIGH SIDE DRIVER

ADVANCE DATA

- HIGH SIDE ACTUATION FOR GROUNDED LOADS
- PWM LOAD CURRENT REGULATION FOR LOW POWER DISSIPATION
- TWO LEVEL CURRENT CONTROL FOR FAST LOAD CURRENT RISE
- SUPPLY COMPENSATED PEAK CURRENT DURATION
- INTERNAL RECIRCULATION ZENER FOR FAST LOAD CURRENT DECAY
- INTERNAL CURRENT SENSE CIRCUIT
- DUMP, SHORT CIRCUIT AND THERMAL PROTECTION
- DIAGNOSTIC OUTPUT



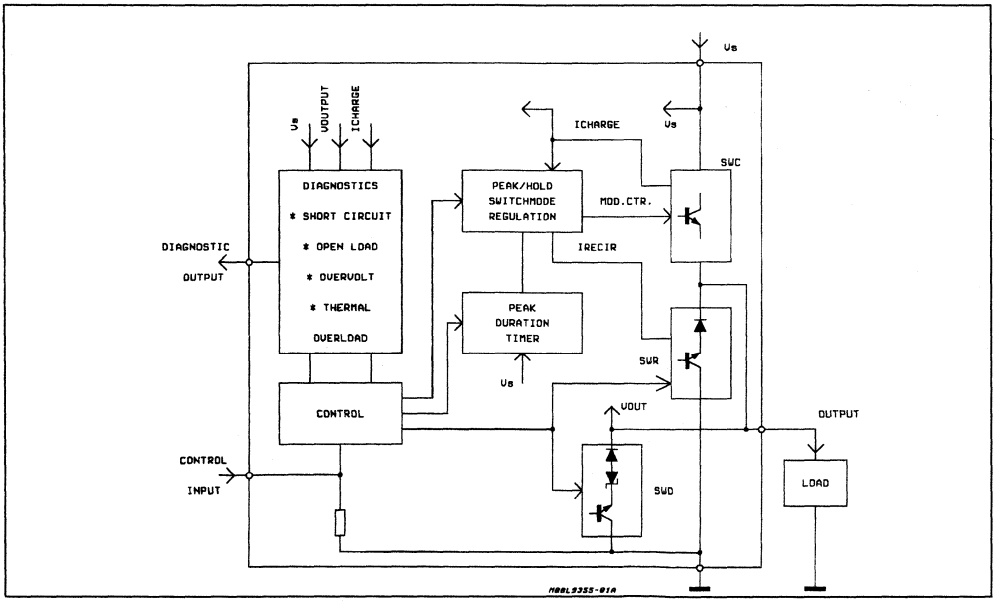
Pentawatt

ORDER CODE : L9355

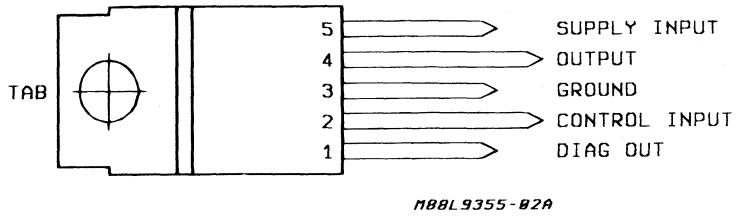
DESCRIPTION

The L9355 is a monolithic power integrated circuit designed to drive inductive grounded loads in the automotive environment. All control, power, protection and diagnostic circuits are provided on chip.

BLOCK DIAGRAM



PIN CONNECTION (top view)



Note : Tab is connected to GND.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
V_S	Supply Voltage (D.C.) Transient Voltage (load dump : 5ms ≤ t_{rise} ≤ 10ms τ_f Fall Time Constant ≤ 100ms, R_{source} ≥ 0.5Ω)	− 0.3	+ 26 + 60	V V
I_O	Output Current	Internally Limited		
V_i	Input Voltage	− 0.3	+ 7	V
I_i	Input Current	− 20	+ 20	mA
I_1	Diag. Output Current	− 20	+ 20	mA
V_1	Diag. Output Voltage	− 0.3	+ 7	V
T_j, T_{stg}	Junction and Storage Temperature Range	− 55	+ 150	°C

THERMAL DATA

R_{Tjc}	Thermal Resistance Junction to Case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS

(refer to application circuit and waveform diagram @ V_S = 14.4V and – 40°C ≤ Tj ≤ + 125°C unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{sop}	Operating Supply Voltage		10		24	V
V_{shd}	Overvoltage Shutdown Treshold		26		32	V
I_q	Quiescent Current	$V_{in} > V_{ih}$ $V_{in} < V_{ih}$, $I_o = O$			30 5	mA mA
I_{Hmin}	Minimum Holding Current		1.9		2.1	A
I_{HMAX}	Maximum Holding Current		$1.4*I_{Hmin}$		$1.6*I_{Hmin}$	A
I_{Pmin}	Minimum Peak Current		$1.9*I_{Hmin}$		$2.1*I_{Hmin}$	A
I_{PMAX}	Maximum Peak Current		$2.9*I_{Hmin}$		$3.1*I_{Hmin}$	A
t_P	Peak Current Duration see fig.3	15V ≤ Vs ≤ 24V Vs = 10V	9.5 14.5		12.5 19.5	ms ms
f_{sh}	Short Circuit Prot. Intervention Frequency			10		kHz
I_{od}	Open Load Current Detection	$V_{in} \geq V_{ih}$			40	$\%I_{Hmin}$
V_{sat}	Output Saturation Voltage	$V_s - V_o$ @ I_o = 5A			2	V
V_{osd}	Output Slow Delay Turn-off Voltage	V_o @ I_o = 5A ; Slow Recirculation Mode	– 3			V
V_{ofd}	Output Fast Decay Turn-off Voltage	$V_s \leq 24V$	– 28		– 22	V
I_{lk}	Output Leakage Current	$V_s \leq 24V$			5	mA
V_{iH}	Input Voltage HIGH		2.4			V
V_{iL}	Input Voltage LOW				.8	V
V_{ihy}	Input Hysteresis		.9			V
I_i	Input Current	Input High or Low	– 10		+ 10	µA
V_{1sat}	Diagnostic Output LOW Voltage	$I_1 \leq 1.2mA$			.4	V
I_{1l}	Diagnostic Output HIGH Leakage Curr.	$V_1 \leq 5.5V$			10	µA

FUNCTIONAL DESCRIPTION

This integrated solenoid driver provides in PWM two driving output current levels, the peak and the holding current : the internal peak/hold switch mode regulation (see block diagram) sets I_{Pmax}, I_{Pmin} and I_{Hmax}, I_{Hmin} values.

The device is enabled by the control input voltage (see fig. 2). If this TTL compatible input is High, the SWC circuit is turned on, the output current increases and the peak duration timer is activated. When the output current reaches I_{Pmax} value, SWC is turned off and the internal slow recirculation circuit SWR is switched on causing the current decrease to I_{Pmin} : the output recirculation voltage is max. 3V below the ground voltage.

When the recirculating current has decayed to I_{Pmin}, SWC turns on again until the charging current reaches the maximum value and the process is repeated for a tp time set by the peak duration timer. t_p Vs. V_S variation is shown in fig. 3. Exceeded tp duration, the peak current decays to I_{Hmin} value and the switchmode operation between I_{Hmin} and I_{Hmax}, internally regulated, is repeated until the control input level is High. If the control input goes Low, SWC and SWR are turned off while the fast recirculation circuit SWD is activated : in this way the inductive load stored energy is quickly discharged and the output fast decay voltage is max. 28V below ground voltage.

The L9355 features thermal, overvoltage and output short circuit protection. The diagnostic feedback is able to send to an external processor the following fault information :

1) Thermal overload
2) Overvoltage condition
3) Open load condition
4) Ground short circuit to output : both hard (R_{short} = 0Ω) and soft (R_{short} = 15 to 35Ω) short circuit.
5) Battery short circuit to output : both hard (R_{short} = 0Ω) and soft (R_{short} = 15 to 35Ω) short circuit.

Figure 1 : Test and Application Circuit.

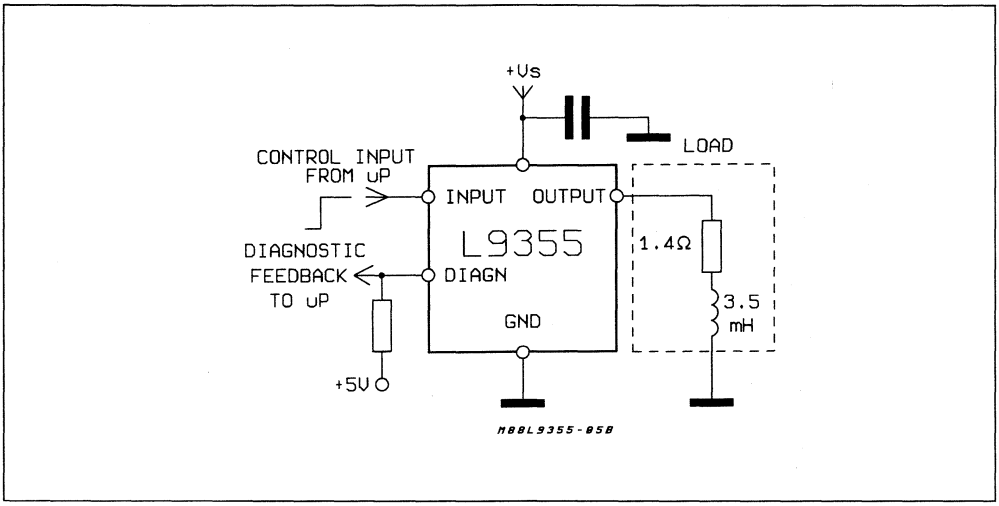


Figure 2 : Output Waveform.

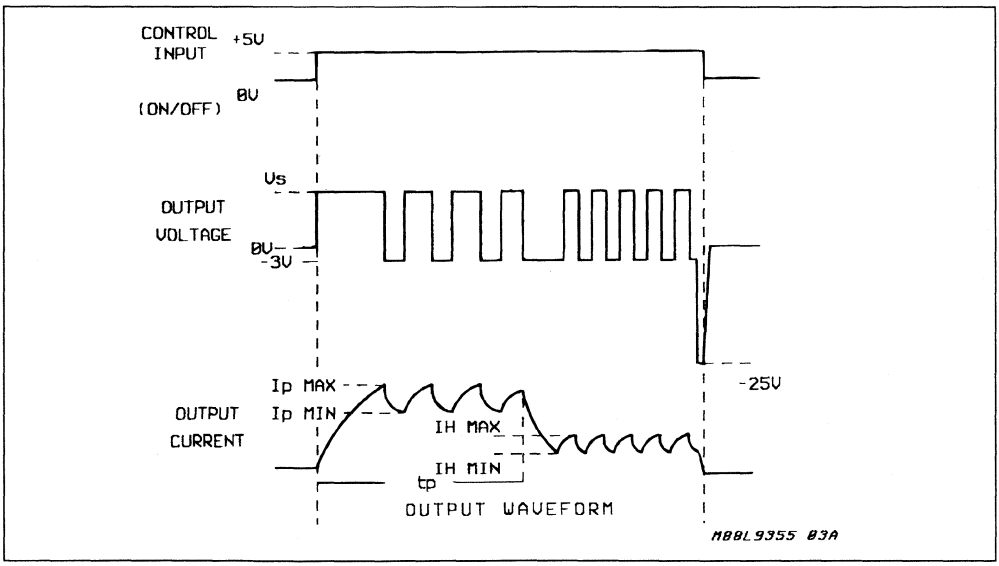
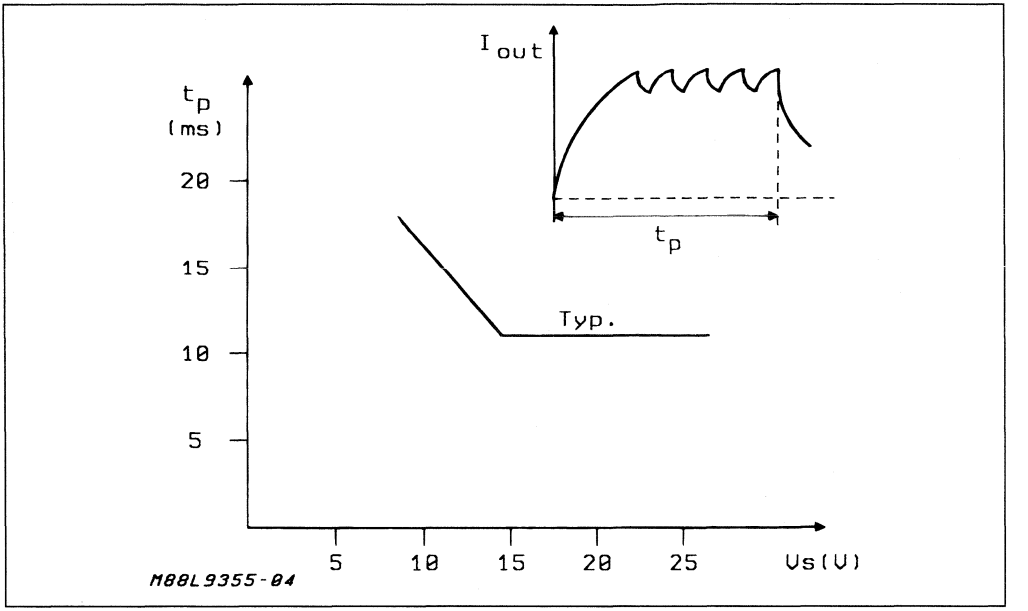


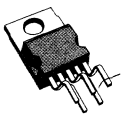
Figure 3 : Peak Duration Time vs. Supply Voltage.



HIGH SIDE DRIVER

ADVANCE DATA

- 25A PEAK OUTPUT CURRENT
- R_{ON} = 100mΩ
- DIAGNOSTIC AND PROTECTION FUNCTIONS
- INRUSH CURRENT LIMITER
- µP COMPATIBLE
- GROUNDED CASE



PENTAWATT

ORDER CODE: L9801A

DESCRIPTION

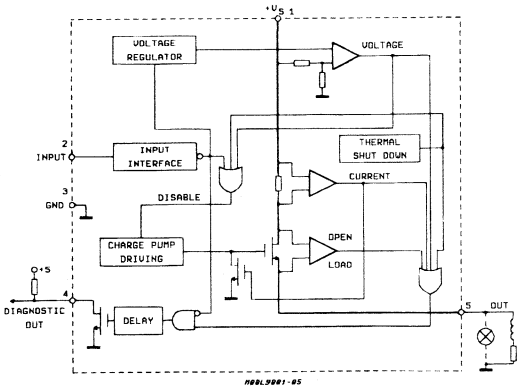
The L9801 High Side Driver realized with ST Multipower - BCD mixed technology, drives resistive or inductive loads with one side connected to ground.

The input control is TTL compatible and a diagnostic output provides an indication of load (open and short) and device status (thermal and overvoltage shutdown). On chip thermal protection and short circuit protection are provided.

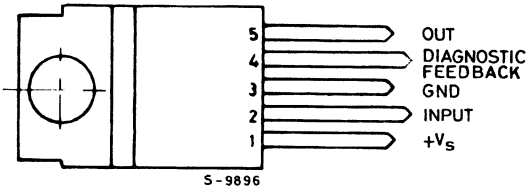
Inrush current limiting makes the L9801 particularly suited for driving lamps.

The device is assembled in the Pentawatt package with the tab connected to the ground terminal.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value
V_S	Max Forward Voltage Positive Transient Peak Voltage (dump : τ_f fall time constant = 100 ms, 5 ms ≤ t_{rise} ≤ 10 ms, R_{source} ≥ 0.5 Ω) – Resistive Load – Inductive Load	50 Vdc 60 V 50 V (*)
	Reverse Input Voltage	– 0.3 Vdc
V_I V_4 V_5	Input Voltage Pin 2 (to GND) Pin 4 Voltage (to GND) Pin 5 Voltage (to GND)	– 0.3 V / + V_s (V_s < 20 V) – 0.3 V / + V_s (V_s < 20 V) – 3 V / + V_s (V_s < 20 V)
I_1 I_2 I_4 I_5	Pin 1 Current Pin 2 Current (forced) Pin 4 Current (sink) Pin 5 Current	Internally Limited 0.5 mA 10 mA Internally Limited
P_{TOT} T_J, T_{STG}	Power Dissipation Junction and Storage Temperature Range	Internally Limited – 55 °C to + 150 °C

* due to the negative voltage at the output during the switching off.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.5	°C/W

PIN FUNCTIONS

1. POWER SUPPLY

Supply voltage input. When the supply reaches the maximum operating voltage (16 V) the device is turned off, protecting itself and the load.

2. INPUT

TTL compatible input. High level on this pin means output current ON. The low level voltage switches off the charge pump, the power stage and the diagnostic output reducing to the minimum value the quiescent current.

3. GROUND

This pin must be connected to ground.

4. DIAGNOSTIC FEEDBACK.

The diagnostic circuit is active in input high level condition. This output detects with 25 msec delay the following faults :

- Overvoltage condition.
- Thermal shutdown.
- Short circuit. The power stage current is internally limited at 25 A.
- Open load. The open load condition is detected with load current < 1.1 A.

The diagnostic output is active low. The diagnostic delay time allows to avoid spurious diagnosys (i.e : turn ON overcurrent, overvoltage spikes etc.).

5. POWER OUTPUT.

The device is provided with short circuit protection.

ELECTRICAL CHARACTERISTICS : (V_s = 14.4 V ; – 40 °C ≤ T_j ≤ 125 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{op}	Operat. Voltage		9		16	V
R_{on}	On Resistance	Input > 2 V ; T_j = 25 °C Input > 2 V ; Full T Range		0.1	 0.2	Ω Ω
I_{sc}	Short Circuit Curr.			25		A
I_{DL}	Over Current Detection Level		20			A
I_{OPD}	Open Load Detection Level	Device ON		1.1		A
V_{clamp}	Output Under Voltage Clamping	I_{load} < 6 A inductive	– 9		– 4	V
I_{off}	Off State Supply Current	T_j < 35 °C T_j = 85 °C			100 300	µA µA
I_{on}	On State Supply Current			4		mA
V_{IL}	Input Low Level				0.8	V
V_{IH}	Input High Level		2.0			V
I_j	Input Current	0 < V_i < 5 V			100	µA
I_{LEAKD}	Diagnostic Output Leakage Current	V_{cc} = 5 V, Diagnostic Output High			10	µA
V_{SATD}	Diagnostic Output Saturat. Volt.	I_{sink} < 3.5 mA			0.4	V
t_{Dd}	Diagnostic Delay Time	t_j = 25 °C		25		ms
t_{dON}	Output ON Delay Time	t_j = 25 °C		4		µs
t_r	Output ON Rise Time	t_j = 25 °C		50		µs
t_{dOFF}	Output OFF Delay Time	t_j = 25 °C		6.5		µs
t_f	Output OFF Fall Time	t_j = 25 °C		2.5		µs

FUNCTIONAL DESCRIPTION

The L9801 is a high side drive monolithic switch, driven by TTL, CMOS input logic, able to supply resistive or inductive loads up to 6 A DC allowing a current peak of 25 A with a $R_{DS\ (ON)}$ = 0.1 Ω. The electronic switch, in addition to its main function, protects itself, the power network and the load against load dump (up to 60V) and overload and it detects short circuit, open load and overtemperature conditions. All these functions (logic control and power actuation) are possible on a single chip thanks to the new mixed ST Multipower BCD technology that allows to integrate isolated DMOS power transistors in combination with Bipolar and CMOS signal structures on the same chip.

The high side drive connection (series switch between the load and the positive power source) is particularly suited in automotive environment where the electrochemical corrosion withstanding has primary importance. For this connection the best solution is a Power MOS N-channel which requires for driving only a capacitive charge pump completely integrated on the switch chip.

The L9801 is based on a power DMOS series element, a driving circuit with a charge pump, an input logic interface and on some protection and fault detection circuits.

The power DMOS transistor has a $R_{DS\ (ON)}$ = 0.1 Ω (typ. value @ T_J = 25 °C, V_{GS} = 10 V). The low value of $R_{DS\ (ON)}$ is important both to increase the power transferred to the load and to minimize the power dissipated in the device.

The charge pump is a capacitive voltage doubler starting from power supply (car battery), driven by a 500 kHz oscillator.

The input interface is based on a circuitry solution able to guarantee the stability over temperature of the TTL logic levels and very low quiescent current in OFF condition.

When the supply reaches the maximum operating voltage (16 V) the device is turned OFF, protecting itself and the load ; moreover local zener clamps are provided in some critical points to avoid that V_{GS} of any MOS transistor could reach dangerous values even during 60 V load dump transient.

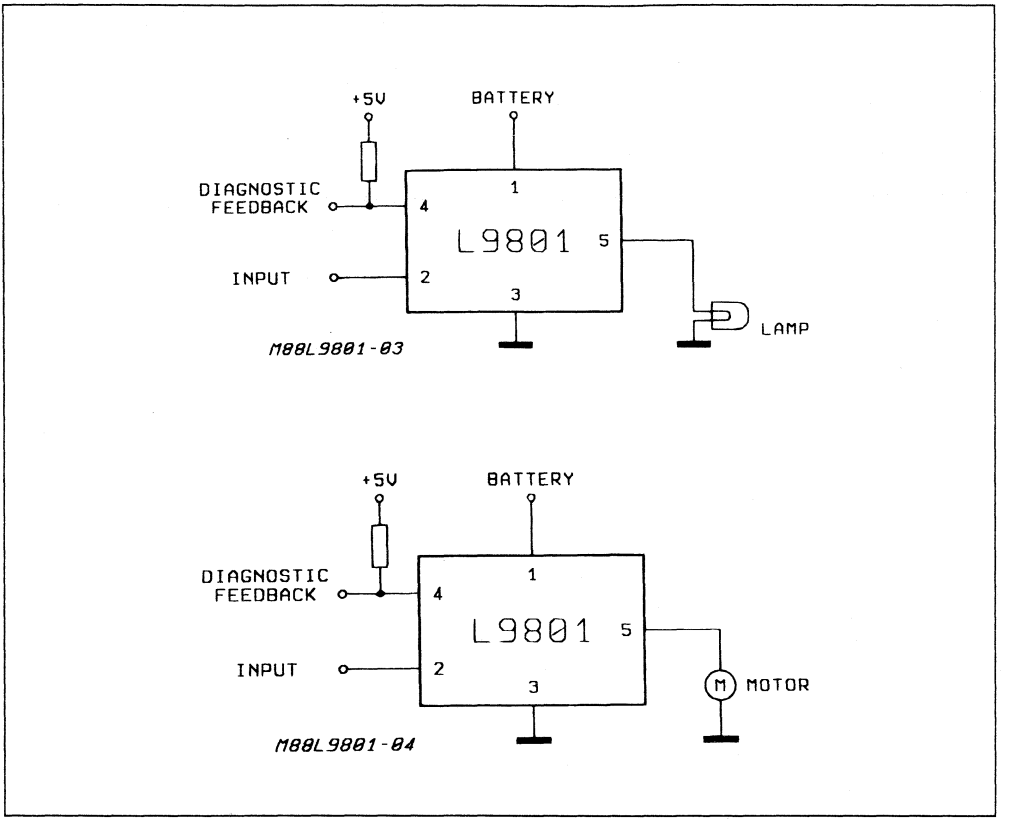
The inrush current limiting is a significant feature of the L9801. This function allows to protect the power supply network and may extend the life of the loads. For example, in the case of the lamps, the tungsten wire resistance value in cold condition is about one tenth of the nominal steady state and then the inrush current during the turn on is statistically one of the main causes of lamps failures. If the high current condition persists (e.g. load short circuit) and the junction temperature rises above 150 °C, the thermal protection circuit turns off the device preventing any damage. The current limiting and the thermal shutdown are sufficient to protect the device against any overload because the power DMOS has not the second breakdown.

When the L9801 is driven and one of the protections (overtemperature, overvoltage, overload) is present, a fault detection open drain output turns on. This output is active also when I_{load} is lower than 1.1 A detecting the open load (disconnected or burned out). The diagnostic output detects fault conditions with 25 ms delay in order to avoid spurious diagnosys (i.e. : turn on overcurrent, overvoltage spikes etc.). In OFF conditions the fault detection circuits are not active to allow a minimum quiescent current.

The device can drive unipolar DC motors and solenoids as well because it can recirculate an inductive current when the output voltage goes lower than V_{clamp} value (typically - 6.5 V in respect to ground). The possibility to have a start up current is useful also for DC motors allowing the maximum starting torque.

TYPICAL APPLICATIONS OF THE L9801

The L9801 integrated high side driver can be used to replace an electromechanical relay. In the following typical application two different driving configurations are shown : resistive load (i.e. lamps) and inductive load (i.e. solenoids, motors). In this last case no external components are required for the coil current recirculation, because the device provides this function internally.



MAKE A FULL BRIDGE USING L9801

To make a bidirectional DC motor driver for the very hostile automotive environment, two L9801 high side drivers and two power MOS devices can be used.

This solution for a DC motor full bridge is self-protected against load dump transients up to 60 V, thermal runaway and short circuit on the motor and to ground.

Thanks to the L9801 features, a motor with nominal current up to 10 A and a stall current up to 25 A can be driven by such a system : the 10A limit for the nominal current depends on the R_{DSON} = 0.1 Ω of the L9801's internal power MOS device. If 1 V is the maximum allowed voltage drop for each power switch at the nominal current this last one must be no higher than 10 A ; the 25 A limit for the motor stall current is due to the internal short circuit protection.

Moreover the described system features a diagnostic output that signals short circuit and open load conditions, main supply overvoltages and thermal shutdown.

CIRCUIT DESCRIPTION

Two solutions are possible to drive the 4 power devices in the full bridge configuration.Fig. 1 shows the first possibility : the system provides 4 µP-compatible inputs and 1 diagnostic output. The L9222 device is a quad inverting transistor switches (open collector outputs) which operates as interface between the µP and the power stage. Depending on the status of this 4 control inputs, the 4 power devices are in ON or in OFF conditions as shown in the truth table A.

The other status of the control inputs have no effect on the operation of the bridge or they are dangerous (i.e. short circuit between the power devices on the same side).

Due to the very short switching times of the discrete PowerMos compared with the L9801 ones - two problems could arise :

1) a simultaneous conduction of I_1 and T_1 (or I_2 and T_2) at the switching on of T_1 (or T_2)

2) an overvoltage on the drain of T_1 (or T_2) at the switching off of T_1 (or T_2).

To avoid these two problems C_1 and C_2 capacitors and the fast switching diodes D_1 and D_2 must be used.

C_3 and C_4 are necessary to prevent overvoltages on the main supply at the switching off phase due to the recirculation current and to the main supply wires inductance. Note that, thanks to the centralized clamp feature of the L9222 device, only one 16 V zener is requested to protect both the power MOS gate and the input of the L9801.

The operating voltage range is 9 V to 16 V ; at supply voltage higher than 16 V the two upper switches, if in ON conditions, are turned-OFF.

The diagnostic output is common for both the L9801 ; this output may be used by the µP to detect bad operating condition of the system.

The second solution for the control of the bridge is that shown in fig. 2 ; in this case we have only two control inputs, plus an enable input. The truth table of such a system is table B.

In this case the control of the bridge is very simple and no 5 V supply voltage is required ; in addition it is not possible the contemporary switch-on of two power devices on the same side of the bridge as in the previous configuration. All the other features of this circuit are identical ones. The L603 device (eight darlingtons array) provides to interface the power stage and the control stage (µP or other) ; in this case too only one centralized clamp zener allows to protect the system inputs against supply overvoltages.

TRUTH TABLE A

I1	I2	I3	I4	Function	Device ON	
H	L	L	H	Turn Left	UL	LR
L	H	H	L	Turn Right	UR	LL
L	H	L	H	Fast Stop	LL	LR
H	L	H	L	Fast Stop	UL	UR
H	H	H	H	Disabled	None	

Note : UL, UR, LL and LR mean respectively upper left, upper right, lower left and lower right device.

TRUTH TABLE B

EN	I1	I2	Function	Device ON	
L	H	L	Turn Left	UL	LR
L	L	H	Turn Right	UR	LL
L	L	L	Fast Stop	LL	LR
L	H	H	Fast Stop	UL	UR
H	X	X	Disabled	None	

Note : X = don't care.

Figure 1 : Full Bridge Configuration with 4 Control Inputs.

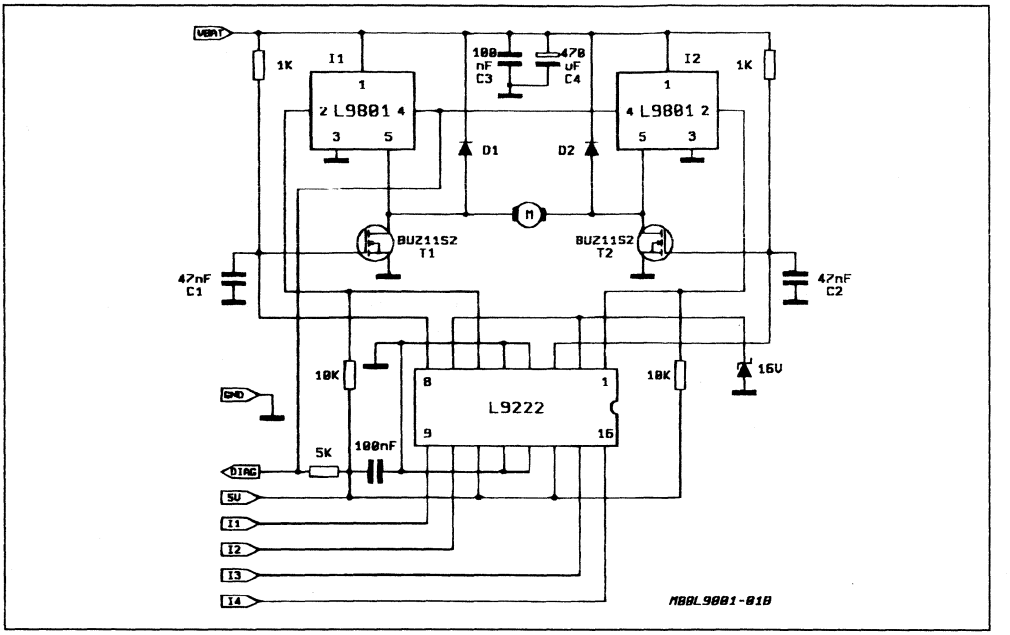
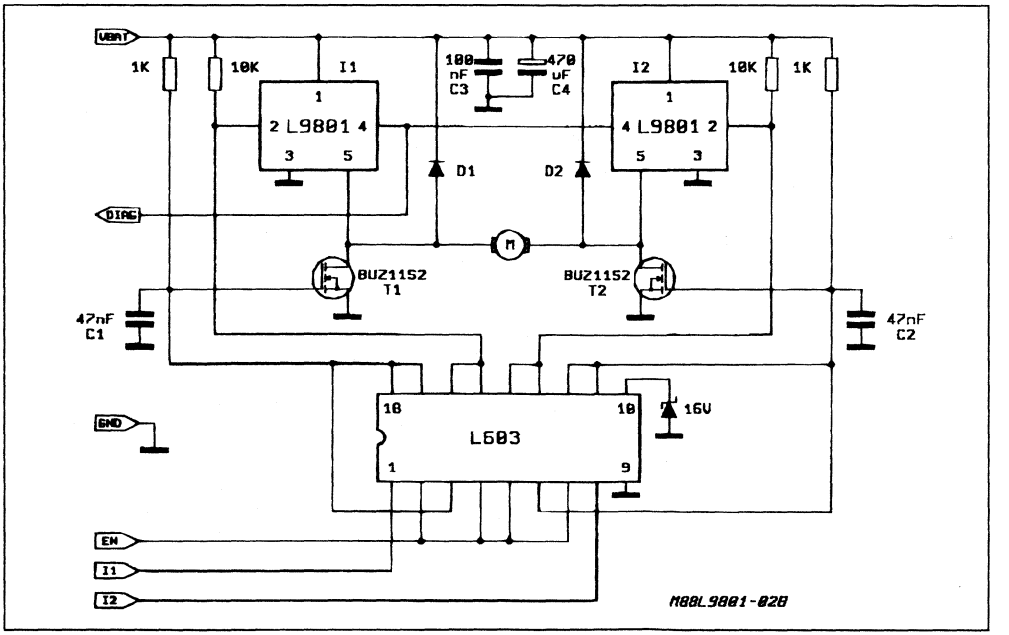


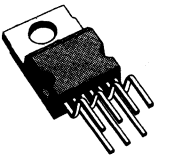
Figure 2 : Full Bridge Configuration with 2 Control Inputs Plus Enable.



DC AND PWM HIGH SIDE DRIVER

ADVANCE DATA

- OPERATING SUPPLY VOLTAGE RANGE 6V TO 45V
- R_{ON} LESS THAN 400mΩ
- µP COMPATIBLE INPUT WITH THRESHOLD HYSTERESIS
- DC AND PWM OPERATION
- HIGH PERFORMANCE DIAGNOSTIC FUNCTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTIONS
- GROUNDED CASE
- ENABLE INPUT FOR STANDBY MODE



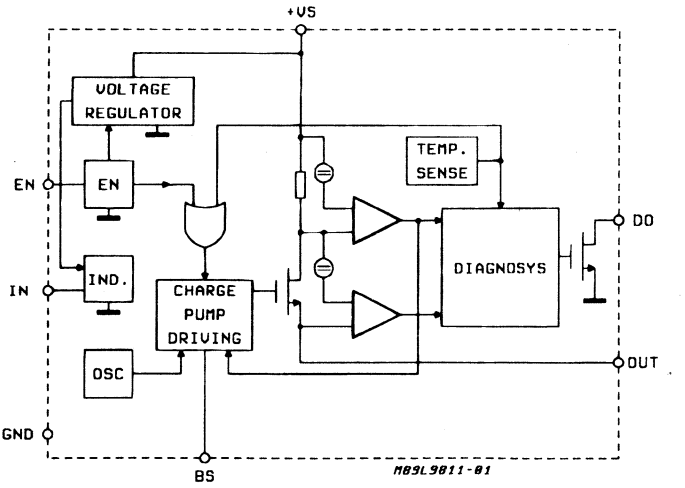
Heptawatt

ORDER CODE : L9811

DESCRIPTION

The L9811 is a monolithic integrated circuit realized in Multipower BCD technology. It is an intelligent high side driver designed especially for inductive or resistive loads. It features all functions necessary for automotive environment including high performance diagnostics.

BLOCK DIAGRAM



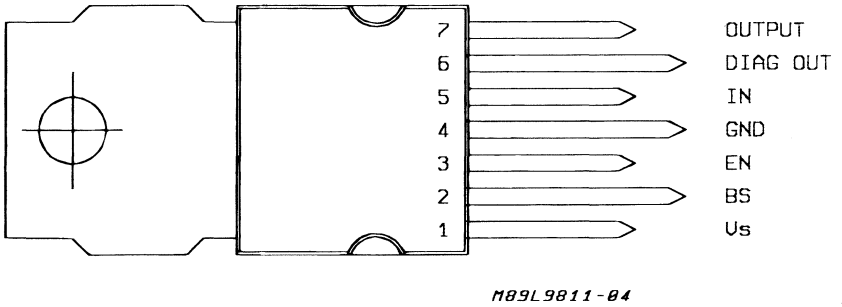
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{SDC}	DC Supply Voltage	+ 45 –0.3	V
V_S- V_{OUT}	Supply to Output Voltage	60	V
V_{IN}, V_{EN}	Input and Enable Input Voltage	+ 7 – 0.2	V
V_{BS}	Bootstrap Voltage	+ 60	V
V_{OUT}	Output Voltage	+ 45 – 18	V
I_{OUT}	Output Current	Internally Limited	
V_{DO}	Diagnostic Output Voltage	+ 32 – 0.2	V
I_{DO}	Diagnostic Output Current	+ 10	mA

THERMAL DATA

$R_{th\ j\text{-}c}$		3.5	°C/W

PIN CONNECTION (top view)



ELECTRICAL CHARACTERISTICS $6V \leq V_S \leq 45V$ (1) ; $-40°C \leq T_j \leq 125°C$; V_{EN} = HIGH unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{ON}	On Resistance	$V_{IN} < 0.8V$; $T_j < 125°C$		200	400	mΩ
I_{SC}	Short Circuit Current		2.5	5	7.5	A
I_{OL}	Open Load Detection Level	Device On $T_j < 125°C$	30	90	140	mA
I_{OC} (2)	Output Current	$V_O = -18V$			100	mA
I_Q	Off State Quiescent Current	$V_{IN} > 2V$		5	10	mA
I_Q	On State Quiescent Current	$V_{IN} < 0.8V$		10	12	mA
V_{IL}	Input Low Level				0.8	V
V_{IH}	Input High Level		2			V
V_{ITH}	Input Thres. Hysteresis		50	100	TBD	mV
I_{IN}	Input Current	$0 < V_{IN} < 5.5V$			10	µA
I_{DL}	Diagnostic Output Leak. Current	Diagnostic Output = HIGH			10	µA
V_{DL}	Diagnotic Output LOW	$I_{DF} < 3.5mA$			0.4	V
V_{OEXD}	Excessive Dropout Voltage Detection Level		1	1.5	2	V
V_{ODTH}	Output Diagn. Threshold	$V_{IN} \geq 2$ V	4		6	V
t_{RD}	Diagnostic Delay Time				10	µs
I_{QSB}	Standby Mode Quiesc. Current	$V_{EN} < 0.8V$ $T_j \leq 125°C$; $V_S = 27V$		200	350	µA
		$V_S = 13V$; $T_j = 25°C$		30		µA
V_{ENL}	Enable Level (3) LOW				0.8	V
V_{ENH}	Enable Level HIGH		2			V
V_{ENTH}	Enable Thresh. Hysteresis		50	100		mV
I_{ENH}	Enable Input Current HIGH	$2V \leq V_{EN} \leq 5.5V$ $V_{EN} \leq V_S - 2V$			10	µA
I_{ENL}	Enable Input Current LOW	$0V < V_{EN} \leq 0.8V$	−1		1	µA
t_{rON}	ON Rise Time	with C_B ; $8V < V_S$	TBD		2	µs
t_{fOFF}	OFF Fall Time	$8V < V_S$			2	µs
t_{dON} t_{dOFF}	ON Delay Time OFF Delay Time	$8V < V_S$ $8V < V_S$		1 1	3 3	µs µs
t_d	DIFF Delay time t_{dON}-t_{dOFF}	$8V < V_S$			2	µs

Notes : 1. for $V_S < 6V$ the device can switch off.
2. an external recirculation path must be assured in PWM operation to avoid exessive power dissipation.
3. standby mode.

DIAGNOSTIC DECISION TABLE

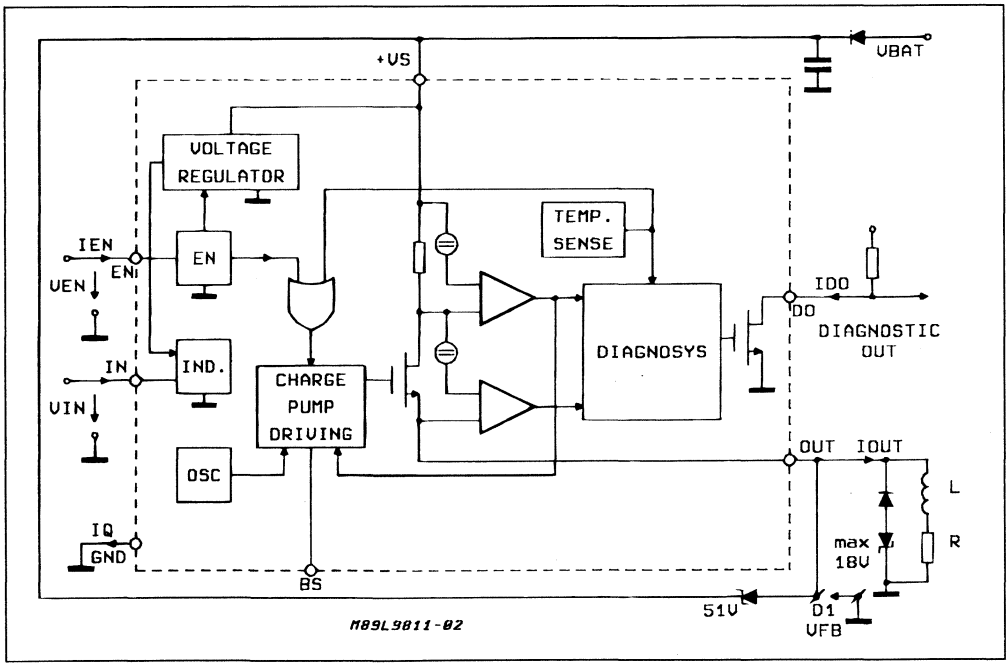
State	Enable	Input	Output VO	Output IO	T_J	Function	Diagnostic
Off	H	H	L	X	< T_{JSD}	Normal "Off"	H
	H	H	L	X	T_{JSD}	Thermal Overload "On"	L
	H	H	> V_{ODth}	X	< T_{JSD}	Output Fail / "Off"	L
On	H	L	H	> I_{OL}	< T_{JSD}	Normal "On"	H
	H	L	X	X	T_{JSD}	Thermal Overload "On"	L
	H	L	X	> I_{SC}	X	Overcurrent "On"	L
	H	L	X	< I_{OL}	X	Open Load "On"	L
	H	L	< V_S-V_{OEXD}	X	< T_{JSD}	Excessive Drop "On"	L
Standby	L	X	X	X	X	Standy Mode	H

= Parameter causing Diagnostic = LOW.

* Minimum thermal shutdown threshold 150°C ; max. hysteresis 35°C.

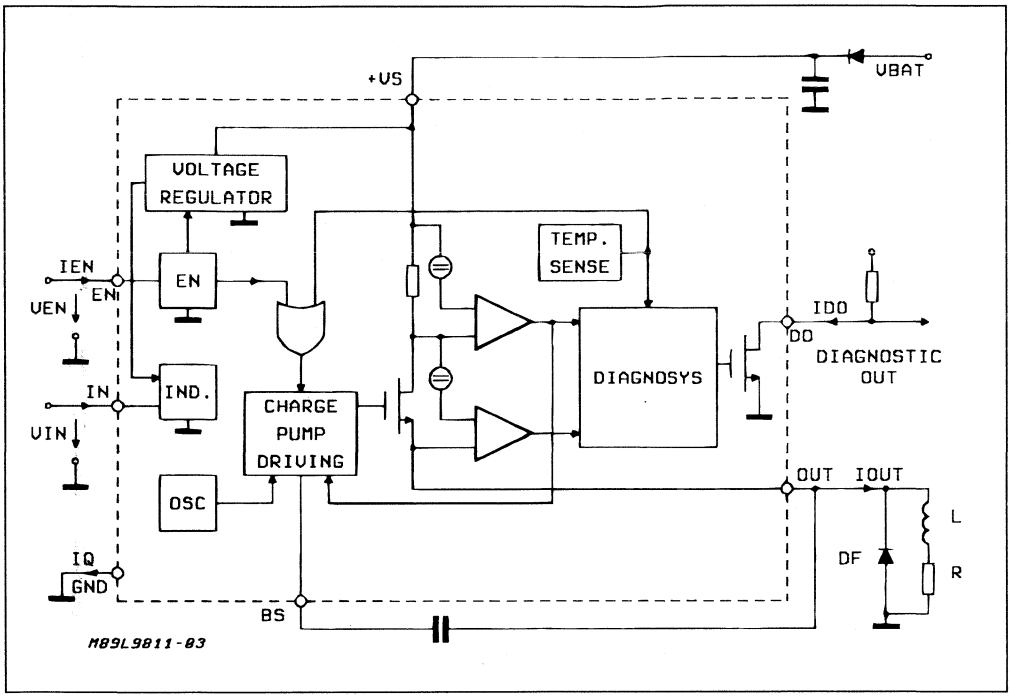
APPLICATION DIAGRAM

Figure 1 : DC – Operation



Note : D1 can be omitted if (V_S + V_{FB}) max ≤ 60V.

Figure 2 : PWM–Operation.

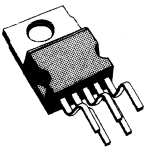


Notes : 1. C_B recommended value.
typ. C_B = 10nF.
2. C_B only with flyback diode D_F.

HIGH SIDE DRIVER

ADVANCE DATA

- 25A PEAK OUTPUT CURRENT
- R_{ON} = 100mΩ
- DIAGNOSTIC AND PROTECTION FUNCTIONS
- INRUSH CURRENT LIMITER
- µP COMPATIBLE
- GROUNDED CASE



Pentawatt

ORDER CODE : L9821

DESCRIPTION

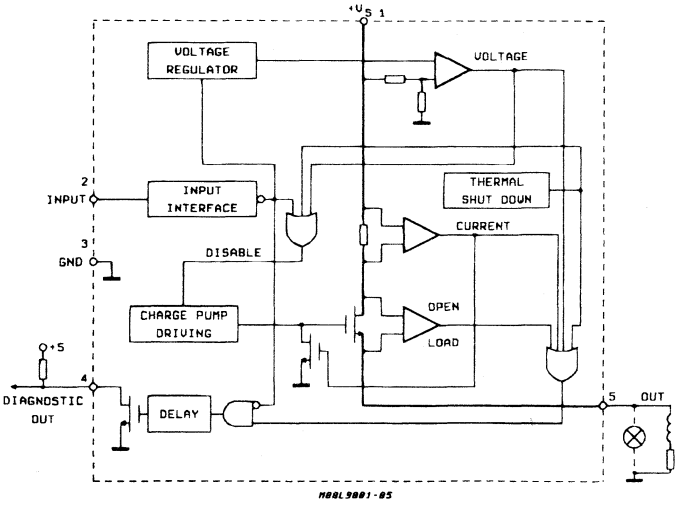
The L9821 High Side Driver realized with Multipower - BCD mixed technology, drives resistive or inductive loads with one side connected to ground.

The input control is TTL compatible and a diagnostic output provides an indication of load (open and short) and device status (thermal and overvoltage shutdown). On chip thermal protection and short circuit protection are provided.

Inrush current limiting makes the L9821 particularly suited for driving lamps.

The device is assembled in the Pentawatt package with the tab connected to the ground terminal.

BLOCK DIAGRAM



M88L9801-05

ABSOLUTE MAXIMUM RATINGS

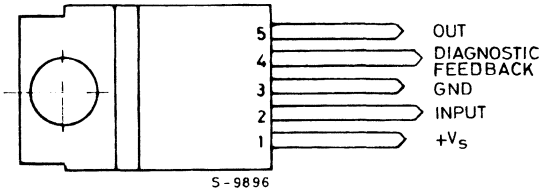
Symbol	Parameter	Value
V_S	Max Forward Voltage Positive Transient Peak Voltage (dump : τ_f fall time constant = 100ms, 5ms ≤ t_{rise} ≤ 10ms, R_{source} ≥ 0.5Ω) – Resistive Load – Inductive Load	50Vdc 60V 50V (*)
	Reverse Input Voltage	– 0.3Vdc
V_I V_4 V_5	Input Voltage Pin 2 (to GND) Pin 4 Voltage (to GND) Pin 5 Voltage (to GND)	– 0.3V / + V_S (V_S < 20V) – 0.3V / + V_S (V_S < 20V) – 3V / + V_S (V_S < 20V)
I_1 I_2 I_4 I_5	Pin 1 Current Pin 2 Current (forced) Pin 4 Current (sink) Pin 5 Current	Internally Limited 0.5mA 10mA Internally Limited
P_{TOT} T_J, T_{STG}	Power Dissipation Junction and Storage Temperature Range	Internally Limited – 55°C to + 150°C

* due to the negative voltage at the output during the switching off.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.5	°C/W

PIN CONNECTION (top view)



PIN FUNCTIONS

1. POWER SUPPLY

Supply voltage input. When the supply reaches the maximum operating voltage (32V) the device is turned off, protecting itself and the load.

2. INPUT

TTL compatible input. High level on this pin means output current ON. The low level voltage switches off the charge pump, the power stage and the diagnostic output reducing to the minimum value the quiescent current.

3. GROUND

This pin must be connected to ground.

4. DIAGNOSTIC FEEDBACK

The diagnostic circuit is active in input high level condition. This output detects with 25msec delay the following faults :

- Overvoltage condition.
- Thermal shutdown.
- Short circuit. The power stage current is internally limited at 25A.
- Open load. The open load condition is detected with load current < 0.6A.

The diagnostic output is active low. The diagnostic delay time allows to avoid spurious diagnosys (i.e : turn ON overcurrent, overvoltage spikes etc.).

5. POWER OUTPUT

The device is provided with short circuit protection.

ELECTRICAL CHARACTERISTICS : (V_s = 14.4V ; – 40°C ≤ T_J ≤ 125°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{op}	Operat. Voltage		6		32	V
R_{on}	On Resistance	Input > 2V : T_j = 25°C Input > 2V : Full T Range		0.1	 0.2	Ω Ω
I_{sc}	Short Circuit Curr.					A
I_{DL}	Over Current Detection Level		20			A
I_{OPD}	Open Load Detection Level	Device ON		0.6		A
V_{clamp}	Output Under Voltage Clamping	I_{load} < 6A Inductive	– 9		– 4	V
I_{off}	Off State Supply Current	T_j < 35°C T_j = 85°C			100 300	µA µA
I_{ON}	On State Supply Current			4		mA
V_{IL}	Input Low Level				0.8	V
V_{IH}	Input High Level		2.0			V
I_I	Input Current	0 < V_i < 5V			10	µA
I_{LEAKD}	Diagnostic Output Leakage Current	V_{cc} = 5V, Diagnostic Output High			10	µA
V_{SATD}	Diagnostic Output Saturation Voltage	I_{sink} < 3.5mA			0.4	V
t_{Dd}	Diagnostic Delay Time	T_J = 25°C		25		ms
t_{dON}	Output ON Delay Time	T_J = 25°C		30		µs
t_r	Output ON Rise Time	T_J = 25°C		100		µs
t_{dOFF}	Output OFF Delay Time	T_J = 25°C		80		µs
t_f	Output OFF Fall Time	T_J = 25°C		100		µs

FUNCTIONAL DESCRIPTION

The L9821 is a high side drive monolithic switch, driven by TTL, CMOS input logic, able to supply resistive or inductive loads up to 6A DC allowing a current peak of 25A with a $R_{DS(ON)}$ = 0.1. The electronic switch, in addition to its main function, protects itself, the power network and the load against load dump (up to 60V) and overload and it detects short circuit, open load and overtemperature conditions. All these functions (logic control and power actuation) are possible on a single chip thanks to the new mixed ST Multipower BCD technology that allows to integrate isolated DMOS power transistors in combination with Bipolar and CMOS signal structures on the same chip.

The high side drive connection (series switch between the load and the positive power source) is particularly suited in automotive environment where the electrochemical corrosion withstanding has primary importance. For this connection the best solution is a Power MOS N-channel which requires for driving only a capacitive charge pump completely integrated on the switch chip.

The L9821 is based on a power DMOS series element, a driving circuit with a charge pump, an input logic interface and on some protection and fault detection circuits.

The power DMOS transistor has a $R_{DS(ON)}$ = 0.1Ω (typ. value @ T_J = 25°C, V_{GS} = 10V). The low value of $R_{DS(ON)}$ is important both to increase the power transferred to the load and to minimize the power dissipated in the device.

The charge pump is a capacitive voltage tripler starting from power supply (car battery), driven by a 500kHz oscillator.

The input interface is based on a circuitry solution able to guarantee the stability over temperature of the TTL logic levels and very low quiescent current in OFF condition.

When the supply reaches the maximum operating voltage (32V) the device is turned OFF, protecting itself and the load ; moreover local zener clamps are provided in some critical points to avoid that V_{GS} of any MOS transistor could reach dangerous values even during 60V load dump transient.

The inrush current limiting is a significant feature of the L9821. This function allows to protect the power supply network and may extend the life of the loads. For example, in the case of the lamps, the tungsten wire resistance value in cold condition is about one tenth of the nominal steady state and then the inrush current during the turn on is statistically one of the main causes of lamps failures. If the high current condition persists (e.g. load short circuit) and the junction temperature rises above 150°C, the thermal protection circuit turns off the device preventing any damage. The current limiting and the thermal shutdown are sufficient to protect the device against any overload because the power DMOS has not the second breakdown.

When the L9821 is driven and one of the protections (overtemperature, overvoltage, overload) is present, a fault detection open drain output turns on. This output is active also when I_{load} is lower than 0.6A detecting the open load (disconnected or burned out). The diagnostic output detects fault conditions with 25ms delay in order to avoid spurious diagnosys (i.e. : turn on overcurrent, overvoltage spikes etc.). In OFF conditions the fault detection circuits are not active to allow a minimum quiescent current.

The device can drive unipolar DC motors and solenoids as well because it can recirculate an inductive current when the output voltage goes lower than V_{clamp} value (typically - 6.5V in respect to ground). The possibility to have a start up current is useful also for DC motors allowing the maximum starting torque.

TYPICAL APPLICATION OF THE L9821

The L9821 integrated high side driver can be used to replace an electromechanical relay. The following typical application is used to drive lamps in automotive environment.

Inductive load also (i.e. solenoids, motors) can be driven by the L9821. In this last case no external components are required for the coil current recirculation, because the device provides this function internally.

Figure 1.

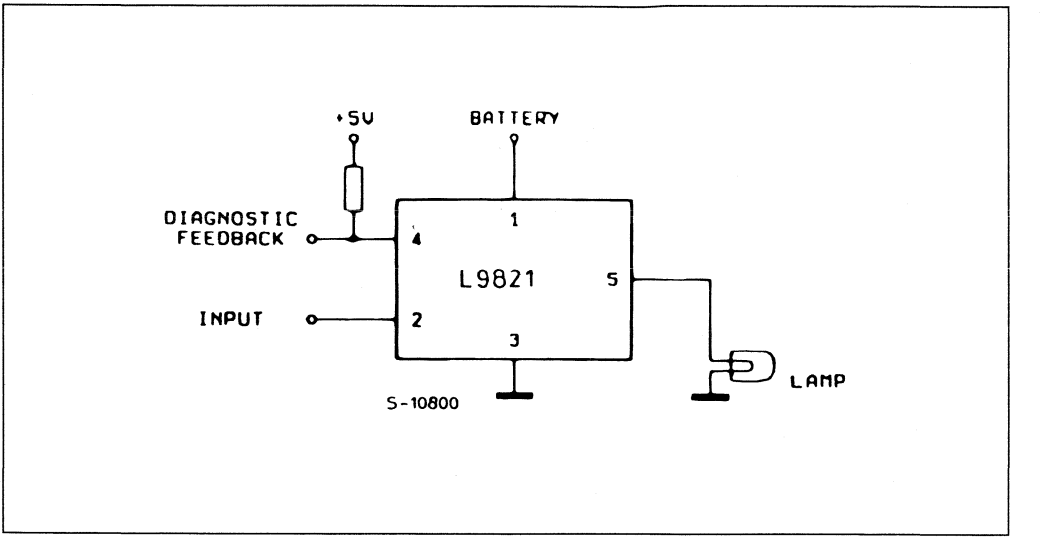
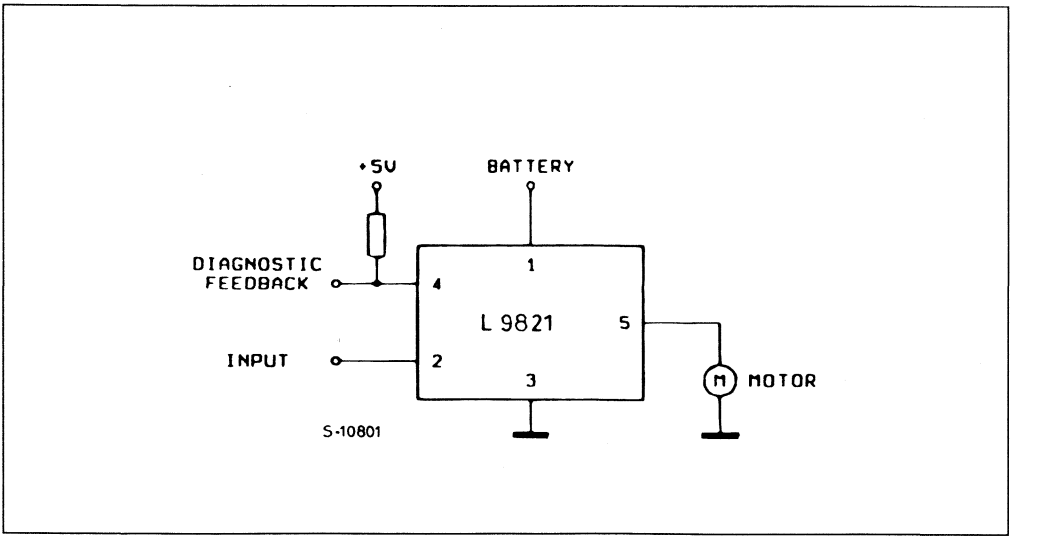


Figure 2.



OCTAL SERIAL SOLENOID DRIVER

ADVANCE DATA

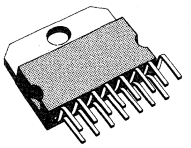
- EIGHT HIGH CURRENT OUTPUTS CAPABLE OF DRIVING UP TO 0.75A PER OUTPUT
- 8 BIT SERIAL INPUT DATA
- 8 BIT SERIAL DIAGNOSTIC OUTPUT FOR OVERLOAD AND OPEN CIRCUIT CONDITIONS
- OUTPUT SHORT CIRCUIT PROTECTION
- CHIP ENABLE SELECT FUNCTION (active low)
- INTERNAL 34V CLAMPING FOR EACH OUTPUT
- CASCADABLE WITH ANOTHER OCTAL DRIVER

DESCRIPTION

TheL9822 is an octal low side solenoid drive rea lized in Multipower-BCD technology particularly suited for driving lamps, relays and solenoids in automotive environment.

Data is transmitted serially to the device using the Serial Peripheral Interface (SPI) protocol.

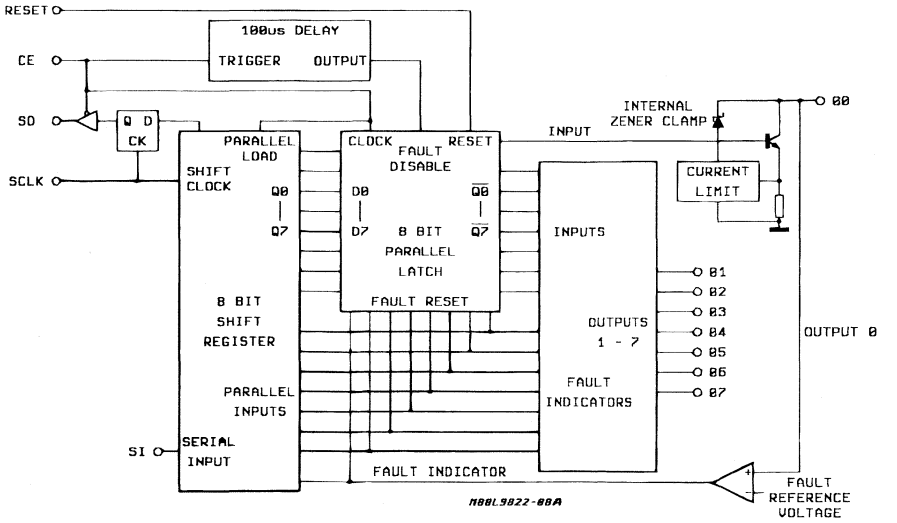
The L9822 features the outputs status monitoring function.



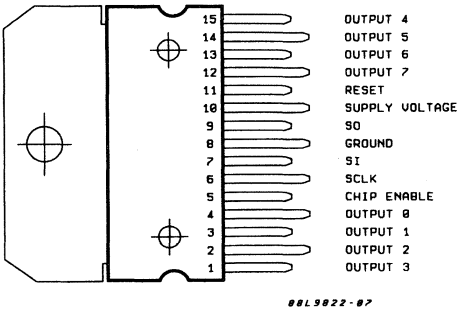
ORDER CODE : L9822

MULTIWATT–15

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
V_{CC}	DC Logic Supply	– 0.7	7	V
V_O	Output Voltage	– 0.7	32	V
I_I	Input Transient Current (CE, SI, SCLK, RESET, SO) : Duration Time t = 1s, $V_I < 0$ $V_I > V_{CC}$	 – 25	 + 25	 mA mA
I_{Odc}	Continous Output Current (for each output)	Int. Limited		A
T_j, T_{stg}	Junction and Storage Temperature Range	– 55	150	C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

PIN DESCRIPTION

V_{CC}

Logic supply voltage - nominally 5V

GROUND

Device Ground. This ground applies for the logic circuits as well as the power output stages.

RESET

Asynchronous reset for the output stages, the parallel latch and the shift register inside the L9822. This pin is active low and it must not be left floating. A power on clear function may be implemented connecting this pin to V_{CC} with an external resistor and to ground with an external capacitor.

CE

Chip Enable. Data is transferred from the shift registers to the outputs on the rising edge of this signal. The falling edge of this signal sets the shift register with the output voltage sense bits coming from the output stages. The output driver for the SO pin is enabled when this pin is low.

SO

Serial Output. This pin is the serial output from the shift register and it is tri-stated when CE is high. A high for a data bit on this pin indicates that the particular output is high. A low on this pin for a data bit indicates that the output is low.

Comparing the serial output bits with the previous serial input bits the external microcontroller implements the diagnostic data supplied by the L9822.

SI

Serial Input. This pin is the serial data input. A high on this pin will program a particular output to be OFF, while a low will turn it ON.

SCLK

Serial Clock. This pin clocks the shift register. New SO data will appear on every rising edge of this pin and new SI data will be latched on every SCLK's falling edge into the shift register.

OUTPUTS 00-07

Power output pins. The input and output bits corresponding to 07 are sent and received first via the SPI bus and 00 is the last. The outputs are provided with current limiting and voltage sense functions for fault indication and protection. The nominal load current for these outputs is 500mA, but the current limiting is set to a minimum of 1.2A. The outputs also have on board clamps set at about 32V for recirculation of inductive load current.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%. T_j = – 40 to 125°C ; unless otherwise speciifed)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OC}	Output Clamping Volt.	I_O = 0.5A, Output Programmed OFF	32		35	V
E_{OC}	Out. Clamping Energy	I_O = 0.5A, When ON	20			mJ
I_{Oleak}	Out. Leakage Current	V_O = 24V, Output Progr. OFF			750	µA
V_{sat}	Output Sat. Voltage	Output Progr. ON I_O = 0.5A I_O = 0.8A I_O = 0.95A With Fault Reset Disabled			 0.5 1.25 2.0	 V V V
I_{OL}	Out. Current Limit	Output Progr. ON	1.2			A
t_{PHL}	Turn-on Delay	I_O = 500mA No Reactive Load			10	µs
t_{PLH}	Turn-off Delay	I_O = 500mA No Reactive Load			10	µs
V_{OREF}	Fault Refer. Voltage	Output Progr. ON Fault detected if $V_O > V_{OREF}$	1.35		1.65	V
t_{UD}	Fault Reset Delay (after CE L to H transition)	See fig. 3	75		125	µs
V_{OFF}	Output OFF Voltage	Output Progr. OFF, Output Pin Floating.			1.0	V

ELECTRICAL CHARACTERISTICS (continued)

INPUT BUFFER (SI, CE, SCLK and RESET pins)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{T-}	Threshold Voltage at Falling Edge	V_{CC} = 5V ± 10%	$0.2V_{CC}$			V
V_{T+}	Threshold Voltage at Rising Edge	V_{CC} = 5V ± 10%			$0.7V_{CC}$	V
V_H	Hysteresis Voltage	$V_{T+} - V_{T-}$	0.85		2.25	V
I_I	Input Current	V_{CC} = 5.50V, 0 < V_I < V_{CC}	− 10		+ 10	µA
C_I	Input Capacitance	0 < V_I < V_{CC}			20	nF

OUTPUT BUFFER (SO pin)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SOL}	Output LOW Voltage	I_O = 1.6mA			0.4	V
V_{SOH}	Output HIGH Voltage	I_O = 0.8mA	V_{CC} − 1.2V			V
I_{SOtl}	Output Tristate Leakage Current	0 < V_O < V_{CC}, CE Pin Held High, V_{CC} = 5.25V	− 10		10	µA
C_{SO}	Output Capacitance	0 < V_O < V_{CC} CE Pin Held High			20	pF
I_{CC}	Quiescent Supply Current at V_{CC} Pin	T_j = 125°C T_j = 25°C T_j = − 40°C All Outputs Progr. ON. I_O = 0.5A per Output Simultaneously			120 200 250	mA mA mA

SERIAL PERIPHERAL INTERFACE (see fig. 2, timing diagram)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{op}	Operating Frequency		D.C.		500	KHz
t_{lead}	Enable Lead Time				1000	ns
t_{lag}	Enable Lag Time				1000	ns
t_{wSCKH}	Clock HIGH Time		840			ns
t_{wSCKL}	Clock LOW Time		840			ns
t_{su}	Data Setup Time		500			ns
t_H	Data Hold Time		500			ns
t_{EN}	Enable Time				1000	ns
t_{DIS}	Disable Time				1000	ns
t_V	Data Valid Time				740	ns
t_{rSO}	Rise Time (SO output)	V_{CC} = 20 to 70% C_L = 200pF			100	ns
t_{fSO}	Fall Time (SO output)	V_{CC} = 70 to 20% C_L = 200pF			100	ns
t_{rSI}	Rise Time SPI Inputs (SCK, SI, CE)	V_{CC} = 20 to 70% C_L = 200pF			2.0	µs
t_{fSI}	Fall Time SPI Inputs (SCLK, SI, CE)	V_{CC} = 70 to 20% C_L = 200pF			2.0	µs
t_{ho}	Output Data Hold Time		0			µs

FUNCTIONAL DESCRIPTION

The L9822 is a low operating power device featuring, eight 0.75A open collector drivers with transient protection circuits in output stages. Each channel is independently controlled by an output latch and a common RESET line which disables all eight outputs. The driver has low saturation and short circuit protection and can drive inductive and resistive loads such as solenoids, lamps and relais. Data is transmitted to the device serially using the Serial Peripheral Interface (SPI) protocol. The circuit receives 8 bit serial data by means of the serial input (SI) which is stored in an internal register to control the output drivers. The serial output (SO) provides 8 bit of diagnostic data representing the voltage level at the driver output. This allows the microprocessor to diagnose the condition of the output drivers.

The output saturation voltage is monitored by a comparator for an out of saturation condition and is able to unlatch the particular driver through the fault reset line. This circuit is also cascadable with another octal driver in order to jam 8 bit multiple data. The device is selected when the chip enable (CE) line is low.

Additionally the (SO) is placed in a tri-state mode when the device is deselected. The negative edge of the (CE) transfers the voltage level of the drivers to the shift register and the positive edge of the (CE) latches the new data from the shift register to the drivers. When CE is Low, data bit contained into the shift register is transferred to SO output at every SCLK positive transition while data bit present at SI input is latched into the shift register on every SCLK negative transition.

INTERNAL BLOCKS DESCRIPTION

The internal architecture of the device is based on the three internal major blocks : the octal shift register for talking to the SPI bus, the octal latch for holding control bits written into the device and the octal load driver array.

SHIFT REGISTER

The shift register has both serial and parallel inputs and serial and parallel outputs. The serial input accepts data from the SPI bus and the serial output simultaneously sends data into the SPI bus. The parallel outputs are latched into the parallel latch inside the L9822 at the end of a data transfer. The parallel inputs jam diagnostic data into the shift register at the beginning of a data transfer cycle.

PARALLEL LATCH

The parallel latch holds the input data from the shift register. This data then actuates the output stages. Individual registers in the latch may be cleared by fault conditions in order to protect the overloaded output stages. The entire latch may also be cleared by the RESET signal.

OUTPUT STAGES

The output stages provide an active low drive signal suitable for 0.75A continuous loads. Each output has a current limit circuit which limits the maximum output current to at least 1.2A to allow for high inrush currents. Additionally, the outputs have internal zeners set to 34 volts to clamp inductive transients at turn-off. Each output also has a voltage comparator observing the output node. If the voltage exceeds 1.5V on an ON output pin, a fault condition is assumed and the latch driving this particular stage is reset, turning the output OFF to protect it. The timing of this action is described below. These comparators also provide diagnostic feedback data to the shift register. Additionally, the comparators contain an internal pulldown current which will cause the cell to indicate a low output voltage if the output is programmed OFF and the output pin is open circuited.

TIMING DATA TRANSFER

Figure #2 shows the overall timing diagram from a byte transfer to and from the L9822 using the SPI bus.

CE High to Low Transition

The action begins when the Chip Enable (CE) pin is pulled low. The tri-state Serial Output (SO) pin driver will be enabled entire time that CE is low. At the falling edge of the CE pin, the diagnostic data from the voltage comparators in the output stages will be latched into the shift register. If a particular output is high, a logic one will be jammed into that bit in the shift register. If the output is low, a logic zero will be loaded there. The most significant bit (07) should be presented at the Serial Input (SI) pin. A zero at this pin will program an output ON, while a one will program the output OFF.

SCLK Transitions

The Serial Clock (SCLK) pin should then be pulled high. At this point the diagnostic bit from the most significant output (07) will appear at the SO pin. A high here indicates that the 07 pin is higher than 1.5V. The SCLK pin should then be toggled low then high. New SO data will appear following every rising edge of SCLK and new SI data will be latched into the L9822 shift register on the falling edges. An unlimited amount of data may be shifted through the

device shift register (into the SI pin and out the SO pin), allowing the other SPI devices to be cascaded in a daisy chain with the L9822.

CE Low to High Transition

Once the last data bit has been shifted into the L9822, the CE pin should be pulled high.

At the rising edge of CE the shift register data is latched into the parallel latch and the output stages will be actuated by the new data. An internal 100 usec delay timer will also be started at this rising edge. During the 100 usec period, the outputs will be protected only by the analog current limiting circuits since the resetting of the parallel latches by faults conditions will be inhibited during this period. This allows the part to overcome any high inrush currents that may flow immediately after turn on. Once the delay period has elapsed, the output voltages are sensed by the comparators and any output with voltages higher than 1.5V are latched OFF. It should be noted that the SCLK pin should be low at both transitions of the CE pin to avoid any false clocking of the shift register. The SCLK input is gated by the CE pin, so that the SCLK pin is ignored whenever the CE pin is high.

FAULT CONDITIONS CHECK

Checking for fault conditions may be done in the following way. Clock in a new control byte. Wait 150 microseconds or so to allow the outputs to settle. Clock in the same control byte and observe the diagnostic data that comes out of the device. The diagnostic bits should be identical to the bits that were first clocked in. Any differences would point to a fault on that output. If the output was programmed ON by clocking in a zero, and a one came back as the diagnostic bit for that output, the output pin was still high and a short circuit or overload condition exists. If the output was programmed OFF by clocking in a one, and a zero came back as the diagnostic bit for that output, nothing had pulled the output pin high and it must be floating, so an open circuit condition exists for that output.

Figure 1 : Byte Timing with Asynchronous Reset.

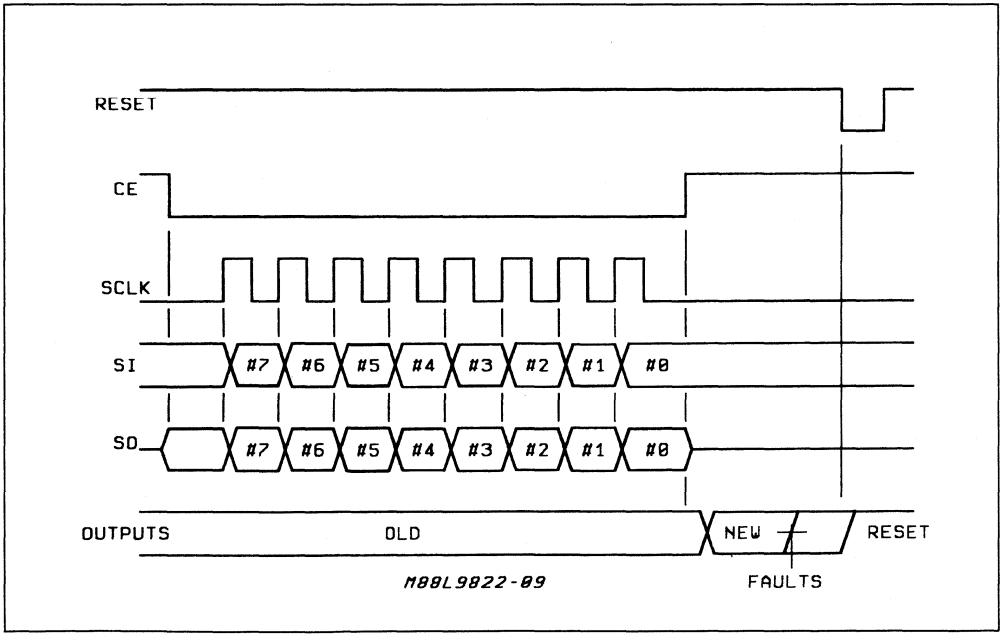


Figure 2 : Timing Diagram.

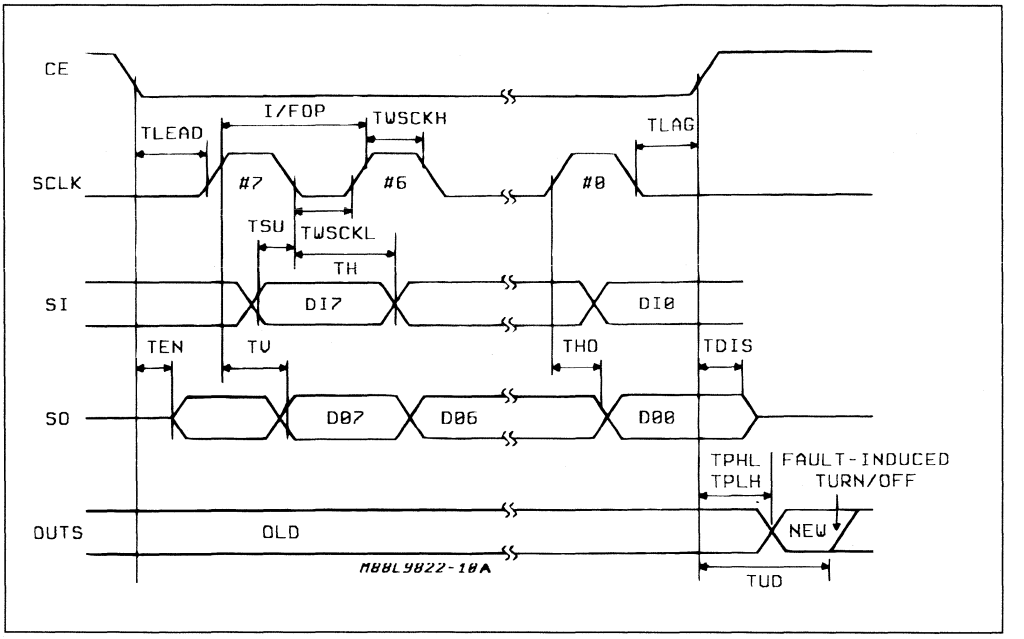
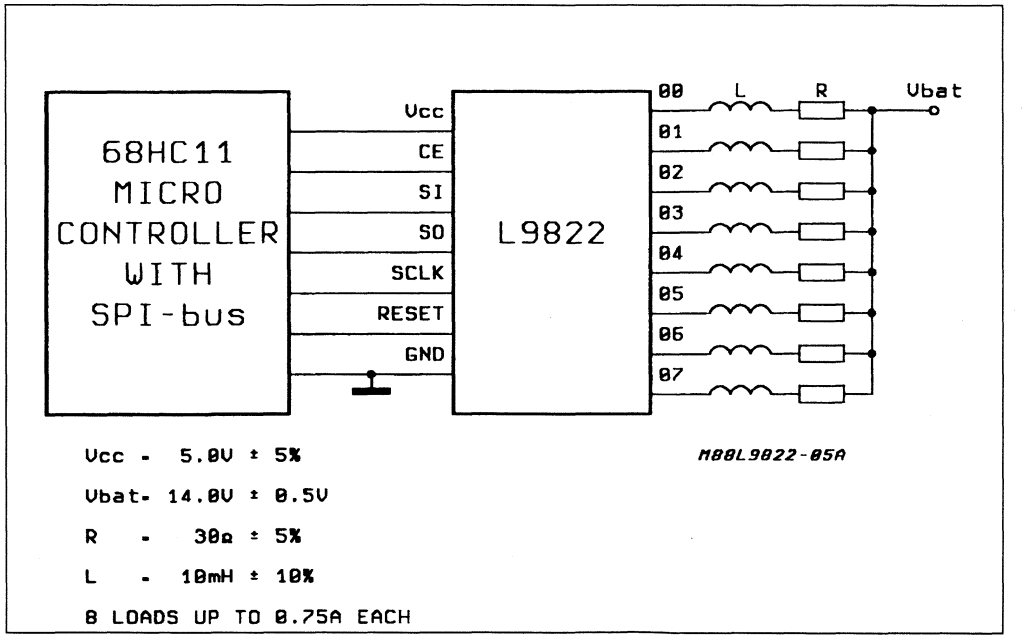


Figure 3 : Typical Application Circuit.



Vcc - 5.0V ± 5%

Vbat- 14.0V ± 0.5V

R - 30Ω ± 5%

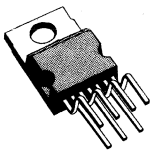
L - 10mH ± 10%

8 LOADS UP TO 0.75A EACH

MONOLITHIC LAMP DIMMER

ADVANCE DATA

- HIGH EFFICIENCY DUE TO PWM CONTROL AND POWER DMOS DRIVER
- CURRENT LIMITATION
- OVER AND UNDERVOLTAGE PROTECTION
- THERMAL PROTECTION
- LIMITED AND PROGRAMMABLE OUTPUT VOLTAGE SLEW RATE
- OPEN GROUND PROTECTION
- VERY LOW STANDBY POWER CONSUMPTION
- LOAD DUMP PROTECTION
- MINIMIZED ELECTROMAGNETIC INTERFERENCE
- WIDE CHOICE IN PWM FREQUENCY RANGE
- LOAD POWER LIMITATION



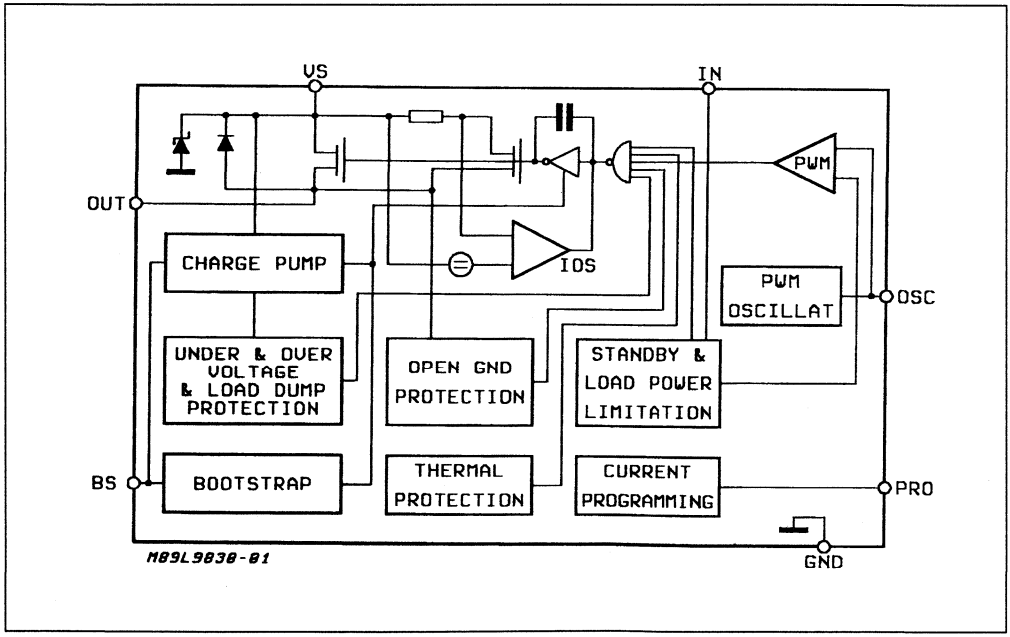
HEPTAWATT

ORDER CODE : L9830

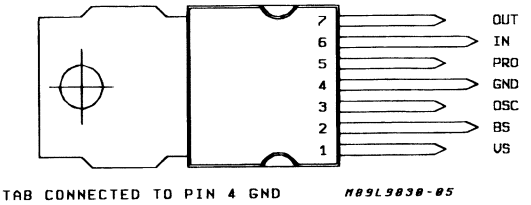
DESCRIPTION

The L9830 high side driver is a monolithic integrated circuit realized with Multipower BCD mixed technology to drive resistive or inductive loads in PWM mode. The device is particularly suited as dashboard dimmer in automotive applications.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Transient Supply Overvoltages : Load Dump : $5ms \leq t_{rise} \leq 10ms$ τ_f Fall Time Constant = 100ms $R_{SOURCE} \geq 0{,}5\Omega$	60	V
I_q	Supply Current	± 0.2	A
I_{OR}	Output Reverse Current	– 2.0	A
V_{DS}	Drain Source-voltage	60	V
V_{IN}	Input Voltage	– 0.3, VS + 0.3	V
T_J , T_{STG}	Junction and Storage Temperature	– 55 to 150	°C

THERMAL DATA

$R_{th\ J\text{-}C}$	Thermal Resistance Junction-case	2	°C/W

PIN FUNCTION (7 Pin Heptawatt)

Name	Function
GND	Common Ground Connection
VS	Power Supply Connection
BS	A capacitor connected between this pin and the Source of the power DMOS pin Out allows to bootstrap the gate driving voltage of the power DMOS.
OSC	A capacitance C_T connected between GND and this pin sets the PWM switching frequency.
IN	Analog input controlling the PWM ratio, related to VS.
Out	Source Connection of the Internal Power DMOS
PRO	A resistor connected between this pin and GND allows to program the output voltage slew rate, the PWM oscillator frequency and the short circuit current value.

ELECTRICAL CHARACTERISTICS (unless otherwise noted)

$6V \leq VS \leq 16V$, $-40°C \leq T_J \leq 125°C$

Parameter		Conditions	min	typ	max	Unit
I_{qo}	Operating Quiescent Current *1	$V_{IN} \geq 0.2*VS$ $R_P \rightarrow \infty$ $R_P = 30K\Omega$		1.7 4.9	3 10.0	mA
I_{qs}	Standby Current	$V_{IN} \leq V_{INSB}$ $T_j n \leq 100°C$	80	200	400	µA
V_{INSB}	Input Standby High Threshold V_{IN}/VS		0.1	0.15	0.2	
$V_{INSBhys}$	Input Standby Hysteresis		– 350	– 190	– 50	mV
V_{INH}	Input High Threshold	$f_o \times t_{on} = 1$ $VS \leq VS_{LPL}$	0.95VS			
I_{IN}	Input Current	$-0,3 \leq V_{IN} \leq V_S + 0,3V$		1	5	µA
VS_L	Low Supply Voltage High Threshold		5.0	5.5	6	V
VS_{Lhys}	Low Supply Voltage Hysteresis		– 300	– 100	– 50	mV
VS_{LPL}	Load Power Limitation Start Supply Voltage		12.0	13.2	14.5	V
VS_H	High Supply Voltage High Threshold		16.4	18.2	20	V
VS_{Hhys}	High Supply Voltage Hysteresis		– 350	– 190	– 50	mV
VS_{LD}	Load Dump Supply Voltage Threshold		46	52	55	V
R_{LD}	Load Dump Device Serial Resistance	$VS \geq VS_{LD}$		50	110	Ω
K_{T1}	Internal PWM Frequency Constant	$f_o = K_{T/CT}$ $R_P \rightarrow \infty$	250	500	750	Hznf
K_{T0}	External PWM Frequency Constant	$f_o = \frac{1}{C_T R_P} K_{TO}$ $30K\Omega \leq R_P \leq 500K\Omega$	0.225	0.250	0.275	
I_{OS}	Short Current Limitation	$VS = 12V$	3.0	6.0	9.0	A

Notes : 1.

$$I_{qo} = 11.3 \frac{V_S - 0.7V}{R_p} + 0.67mA, \; R_p \leq 30K\Omega$$

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Conditions	min	typ	max	Unit
I_{OS0}	External Programmable Short Current Limit. *4	VS = 12V R_P = 125KΩ	5.1	6.0	6.9	A
R_{DS}	Static Drain Source on Resistance			160	350	mΩ
S_1	Internal Fixed Output Voltage Slew Rate *2	VS = 12V 5Ω ≤ R_L ≤ 7Ω	50	120	190	V/ms
S_0	External Programmable Output Voltage Slew Rate *3	VS=12V, R_P=125KΩ 5Ω ≤ R_L ≤ 7Ω	95	120	145	V/ms

Notes : 2.

$$S_1 = VS * 10.55 \frac{1}{ms} - 6.85 V/ms$$

3.

$$S_0 = \frac{10^3}{R_P} (VS * 1320\ V/\mu C - 860\ V2/\mu C) \frac{V\Omega}{ms}$$

$$S_0 = \frac{R_L}{R_P} \frac{VS - 0.65V}{R_L + 0.32\Omega} 1.38 * 10 \frac{V}{msA}$$

4.

$$I^{OS} = (VS - 0.6V) * 0.514 \frac{A}{V}$$

$$I_{OS0} = (VS - 0.6V) * \frac{64620}{R_P}$$

FUNCTIONAL DESCRIPTION

To control the power of the load with a Power-MOS transistor in the switched mode, its gate must be driven with a PWM signal. The amplitude of the gate driving pulse must guarantee that the Power DMOS transistor will be completely saturated during the ON phase. To generate the necessary gate driving voltage a charge pump circuit is required. With this circuit a gate voltage value approximatively given by $2(V_S - 1.5V)$ is obtained.

The slope of the leading and trailing edge of the gate driving signal is defined with an internal capacitor. The important criteria for the dimensioning of the output voltage slope are the electromagnetic radiation and the power dissipation of the Power DMOS. The typical slope value is about 120V/ms to fulfill automotive EMI requirements.

The output signal slope is directly related to V_S value and is in a wide range programmable through the programming resistance R_P.

$$S = \frac{dV_{out}}{dt} = RL \frac{d_{load}}{dt} = \frac{R_L}{R_P} \frac{VS - 0.65V}{R_L + 0.32\Omega} \frac{10^6 V}{Ams}$$

For fast gate voltage variation the bootstrap option can be used. The bootstrap capacitance should have a relation 50 times greater than DMOS parasitic capacitances and should be about

$$C_{BS} \geq 100nF$$

The switching frequency f_o is defined with a triangle oscillator and is programmed with the capacitor C_T or with C_T and R_P if a greater precision is required.

$$f_o = K_T/C_T \text{ (without } R_P)$$

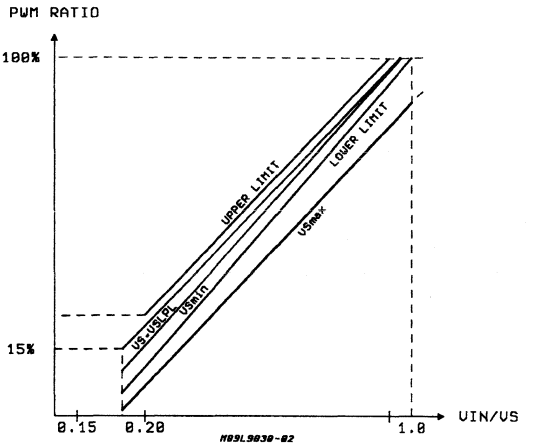
$$fo = \frac{1}{4CTRP} \text{ (with RP)}$$

The modulation factor of the PWM driving signal of the internal Power DMOS transistor is defined by the voltage level at the analog input. The typical trannsfer curve giving the PWM factor as a function of the input voltage is shown in fig. 1.

For V_S values higher than the load power limitation threshold voltage, the PWM ratio is reduced linearly to transfer a constant power to the load.

The input voltage is referred to the supply voltage. The PWM factor regulation can be realized using a potentiometer connected to the supply voltage and the analog input (see the typical application circuit diagram).

TRANSFER CHARACTERISTIC



The maximum load current in the short circuit condition is limited internally with a sense DMOS cell.

The short circuit current value depends on the supply voltage value : this allows to achieve in any condition the lamp required warm up current which will be normally two or three times higher than the nominal current value. The typical short circuit current value can be programmed by the external resistor R_P according to the following formula :

$$I_{OSe} = \frac{VS - 0.6V}{R_P} \; 64620$$

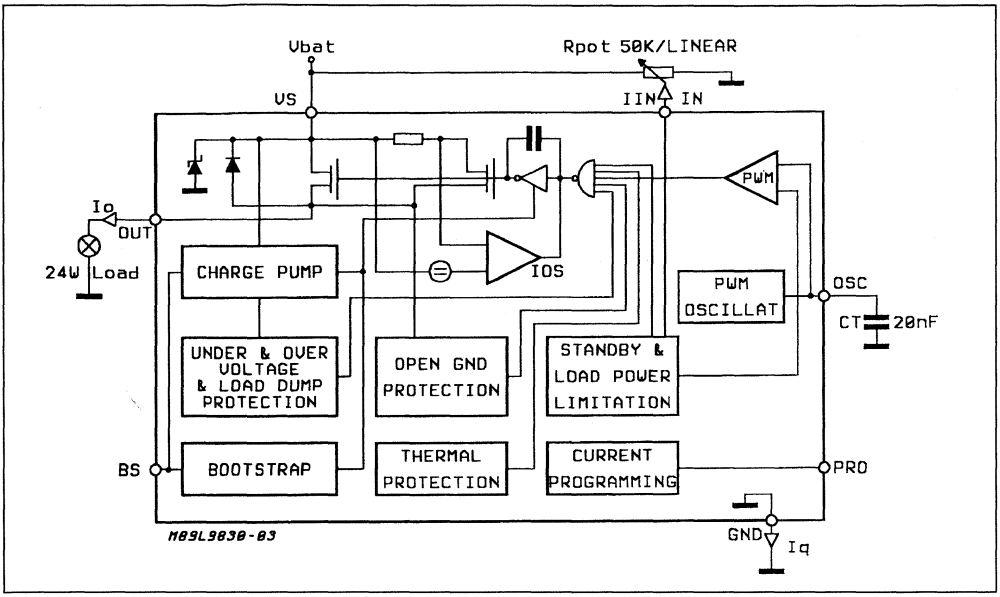
If the short current condition is detected the gate will be driven with a DC voltage regulated to maintain the specified current. With this function the switch on phase for a lamp as a load will be speeded up.

The circuit features also a protection function which allows to withstand high overvoltage for a limited time (load dump in automotive application). Above the VS_H threshold the gate driving of the Power MOS transistor is switched off. When the V_{BAT} rises above the internal supply clamp voltage VS_{LD} the Power DMOS gate voltage arises up to VS. In this condition the current limitation works too the voltage is limited to V_{SLD} with a serial resistance of R_{LD} and the load voltage can be calculated.

$$V_L = VS - V_{GS} \geq I_{SO} R_L$$

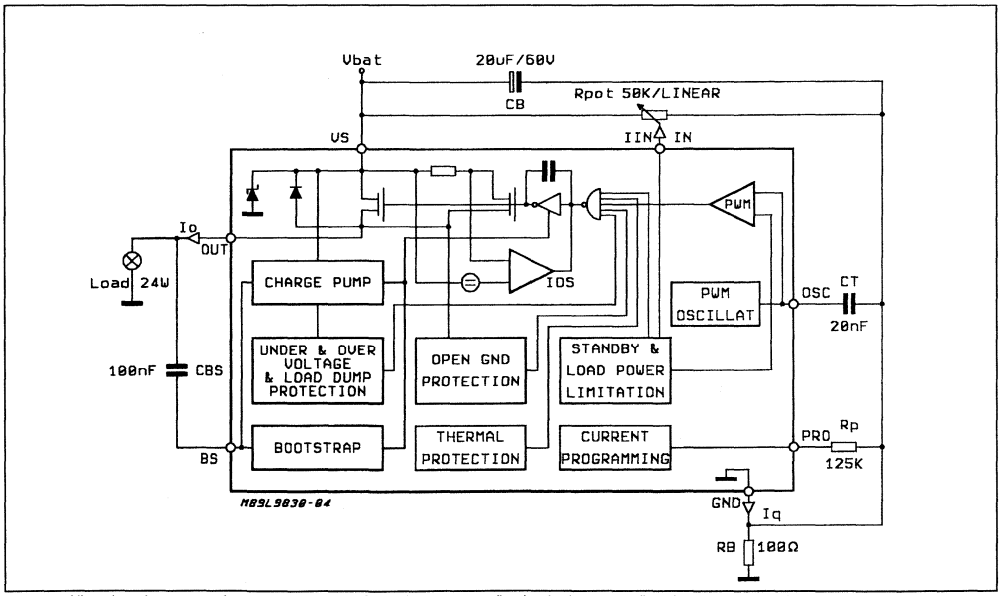
The device is provided with an internal thermal protection.

APPLICATION CIRCUIT DIAGRAM FOR DASHBOARD DIMMING



Note : All node voltage are referred to ground pin GND. The currents flowing in the arrow direction are assumed positive.

APPLICATION CIRCUIT DIAGRAM FOR DASHBOARD DIMMING WITH OPTIMIZED DEVICE POWER DISSIPATION



Note : All node voltage are referred to ground pin GND. The currents flowing in the arrow direction are assumed positive.

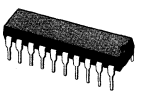
SGS-THOMSON MICROELECTRONICS

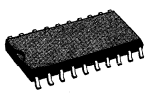
L9842

OCTAL PARALLEL LOW SIDE DRIVER

ADVANCE DATA

- OPERATING DC SUPPLY VOLTAGE RANGE 5V TO 25V
- SUPPLY OVERVOLTAGE PULSE UP TO 40V
- VERY LOW STANDBY QUIESCENT CURRENT 100µA
- EIGHT BIT PARALLEL STRUCTURE WITH MEMORY FEATURE
- BIDIRECTIONAL INPUTS-OUTPUTS
- µC COMPATIBLE INPUT LEVELS WITH THRESHOLD HYSTERESIS
- INTERNAL 4.5V REFERENCE DEFINING THE OUTPUT HIGH LEVELS
- EIGHT HIGH CURRENT OUTPUTS FOR DC CURRENTS UP TO 350mA WITH ON RESISTANCE LESS THAN 3Ω (typ. 1,5Ω)
- OUTPUT SHORT CIRCUIT PROTECTION WITH TIME DELAY CHARACTERISTICS FOR DRIVING LAMPS
- THERMAL OVERLOAD PROTECTION





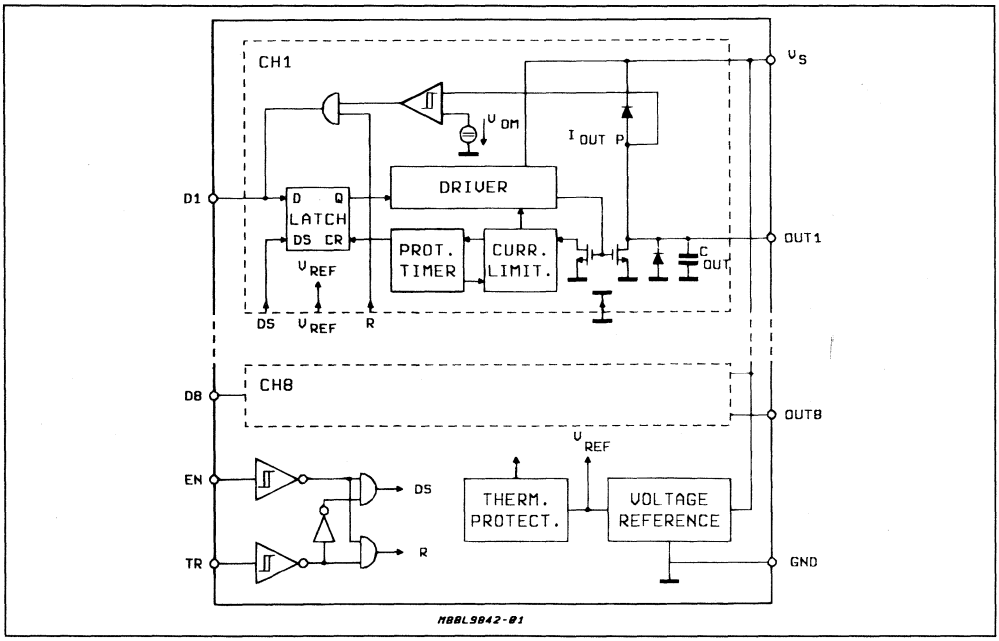
DIP-20 Plastic **SO-20L**

ORDER CODES : L9842 (DIP-20)
L9842D (SO-20L)

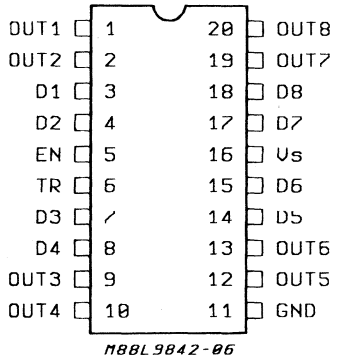
DESCRIPTION

The L9842 is an octal parallel input power interface circuit in the Multipower BCD technology with bidirectional inputs and outputs and output status monitoring.

BLOCK DIAGRAM



PIN CONNECTIONS (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Transient Supply Voltage : Load Dump : 5ms ≤ t_{rise} ≤ 10ms; τ_f Fall Time Constant = 100ms; R_{SOURCE} ≥ 0.5Ω	40	V
V_{OUT}	Output Voltage	Int. Clamped to Vs	V
dV_{OUT}/dt	Output Voltage Transient	100	V/µs
$I_{OUT\ DC}$	DC Output Current	350	mA
$I_{OUT\ P}$ (*)	Peak Output Current of Clamping Diode (T = 0.2s, tp = 2ms)	1	A
$V_{D\ IN}$	Input Voltage	– 0.3 to 7	V
V_E	Enable Input Voltage	– 0.3 to 7	V
V_R	Transfer Input Voltage	– 0.3 to 7	V
T_j-T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C
P_{max}	Power Dissipation (T_{amb} = 80°C) DIP-20 SO-20L	875 420	mW mW

(*) Schaffner pulses type 1 and 2

THERMAL DATA

			DIP-20	SO-20L
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (unless otherwise noted)
$5V \leq V_S \leq 25V$, $-40°C \leq T_j \leq 125°C$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DINL}	Input Voltage LOW	V_E = L, V_{TR} = L (input-mode) [1]	0		1.0	V
V_{DINH}	Input Voltage HIGH		2.0		7.0	V
		V_E = L, V_{TR} = H (output-mode) [1]				
V_{DOUTL}	Output Voltage LOW	I_{DOUT} = 1mA	4.0		0.4	V
V_{DOUTH}	Output Voltage HIGH	I_{DOUT} = – 0.1mA			5.0	V
I_{DIN}	Input Current	V_E = L, V_{TR} = L (input-mode) [1]	– 10		10	µA
V_{EL}	Enable Voltage LOW		0		1.0	V
V_{EH}	Enable Voltage HIGH		2.0		7.0	V
V_{TRL}	Transfer Voltage LOW		0		1.0	V
V_{TRH}	Transfer Voltage HIGH		2.0		7.0	V
$I_{E.TR}$	Enable, Transfer Input Current	$0 < V_{E.TR} < 5V$	– 1		1	µA
V_{EH}	Enable Threshold Hysteresis		50	150	300	mV
$V_{TR.H}$	Transfer Threshold Hysteresis		50	150	300	mV
R_{OUT}	Output Resistance R_{OUT}-characteristic See fig. 2	Out = L $0 < I_{OUT} \leq 200mA$ $8V \leq V_S \leq 25V$ V_{S1} = 6.5V V_{S2} = 5.0V		1.5	3.0 25 1000	Ω Ω Ω
I_{SC}	Output Short Current I_{OUTSC}-characteristic See fig. 3	Out = L : $V_{OUT} = V_S$ T_{SCH} = 2.5mS T_{SCL} = 40mS	1 0.4	1.5 0.65	2 0.9	A A
V_{OUT}	Output Voltage	Out = H I_{OUT} = 0.35A (DC) I_{OUT} = 1A (pulsed)	V_S + 0.5 V_S + 1.5		V_S + 1.5 V_S + 4	V V
ΣI_{OUTL}	Output Leakage Current	Out = H, T_j = 85°C V_{OUT} = 16V	0	10	100	µA
dV_{OUT}/dt	Output Voltage Transient	Out = H	0		100	V/µS
C_{OUT}	Output Capacitance	Out = H, V_{OUT} = 5V V_{OUT} = 15V	60 30	90 60	120 90	pF pF
I_Q	Quiescent Current STANDBY MODE TRANSFER-, HOLD MODE READ MODE	$5V \leq V_S \leq 16V$ T_j = 100°C V_E = H, V_{TR} = H V_{TR} = L V_E = L, V_{TR} = H I_{DOUT} = 0			 100 200 400	 µA µA µA
I_Q	Quiescent Current	V_S = 25V			1	mA
I_{SCOP}	Short Circuit Operating Current Per Channel	V_E = L, V_{DIN} = L V_{TR} = L $I_{OUT} \geq 1A$	300	400	500	µA
V_{OM}	Output Monitor Threshold		2.5		3.5	V

Note : 1. $V_{D...}$ are bidirectional data inputs or outputs depending on the V_E, V_{TR} status.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{SCH} (2)	Duration of High Short Current Limiting	$I_{OUT} > I_{SCH}$	1.25	2.5	3.75	mS
T_{SCL} (2)	Duration of Low Short Current Limiting	$I_{OUT} > I_{SCL}$	20	40	60	mS
t_n ON	ON-delay Time (5)	See fig. 1			10	µS
t_n OFF (3)	OFF-delay Time (5)	R_L = 1KΩ			10	µS
t_s ON	ON-delay Time (5)	See fig. 1		20	40	µS
t_s OFF (3)	OFF-delay Time (5)	R_L = 1KΩ		20	40	µS
/t_{ON}-t_{OFF}/	Delay Time Difference	Except STANDBY MODE			4	µS

Notes : 2. If the output current exceeds the high short current threshold I_{SCH} an internal timer is started and if after the time period of T_{SCH} + T_{SCL} the current limiting is still active the overload condition is recognized and this output is switched off. To restart the output the corresponding input voltage V_{DIN} must become HIGH to reset the internal overload latch.

3. Because the output capacitance is the drain-source capacitance of the power switch the risetime of the outputs depends of the used supply voltage V_S, the load resistor R_L and the output capacitance C_{OUT} and can be calculated with the following equation :
$T_d = T \ln 10$ (reaching 90% of V_S) $T = R_L \times C_{OUT} \times K$ (4) $K = 1.5$
This additional delay time T_d must be added to t_{OFF}.

4. Because the drain source capacitance of the output transistor is voltage dependent, it is necessary to multiply C_{OUT} (specified at the maximum V_{OUT}) with a correction factor K to obtain the average output capacitance C_{OUT}.

5. Delay time between alla modes except STANDBY MODE.

6. Delay time between STANDBY MODE and any other mode and vice versa.

TRUTH TABLE FOR THE CONTROL INPUTS

Enable V_E	Transfer V_{TR}	Mode Symbol	Function Mode
L	H	RM	READ MODE (output monitoring)
L	L	TM	TRANSFER MODE (input data transferred to output)
H	L	HM	HOLD MODE (output corresponds to the data latch)
H	H	SM	STANDBY MODE (all outputs open)

Figure 1 : Timing Diagram with Function Modes.

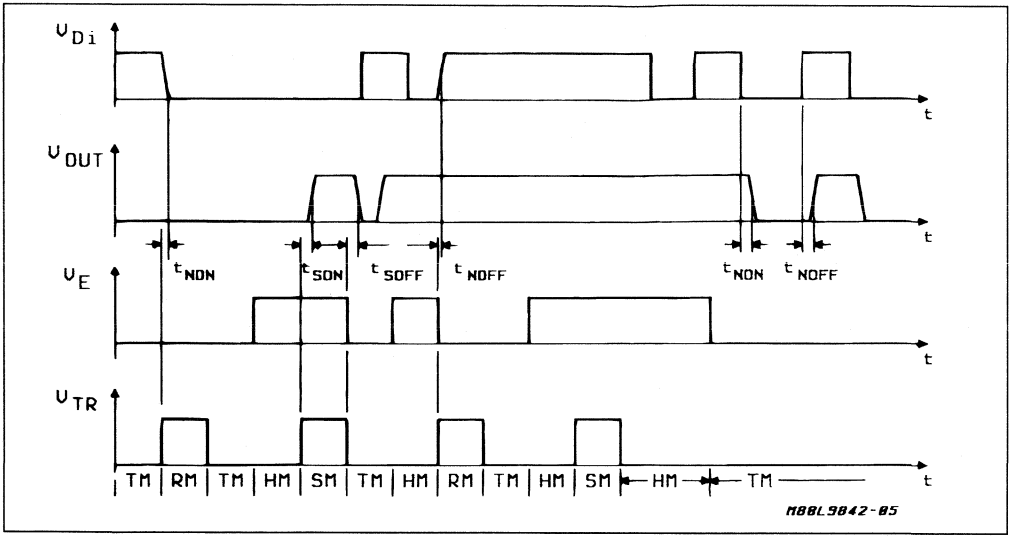


Figure 2 : Maximum R_{OUT} - Characteristics.

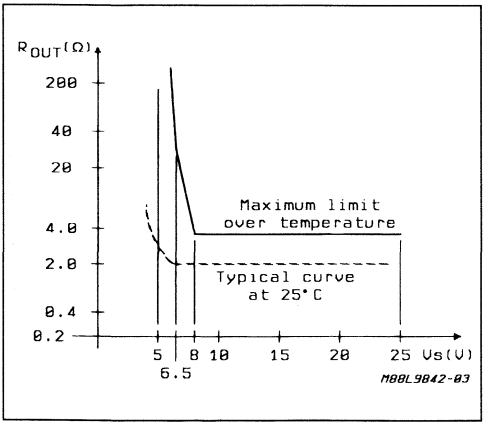


Figure 3 : Typical Output Short Current Characteristics.

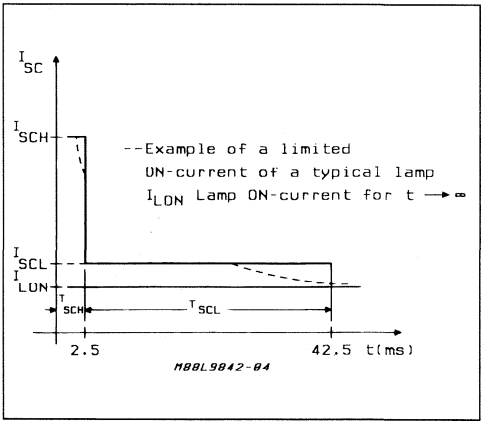
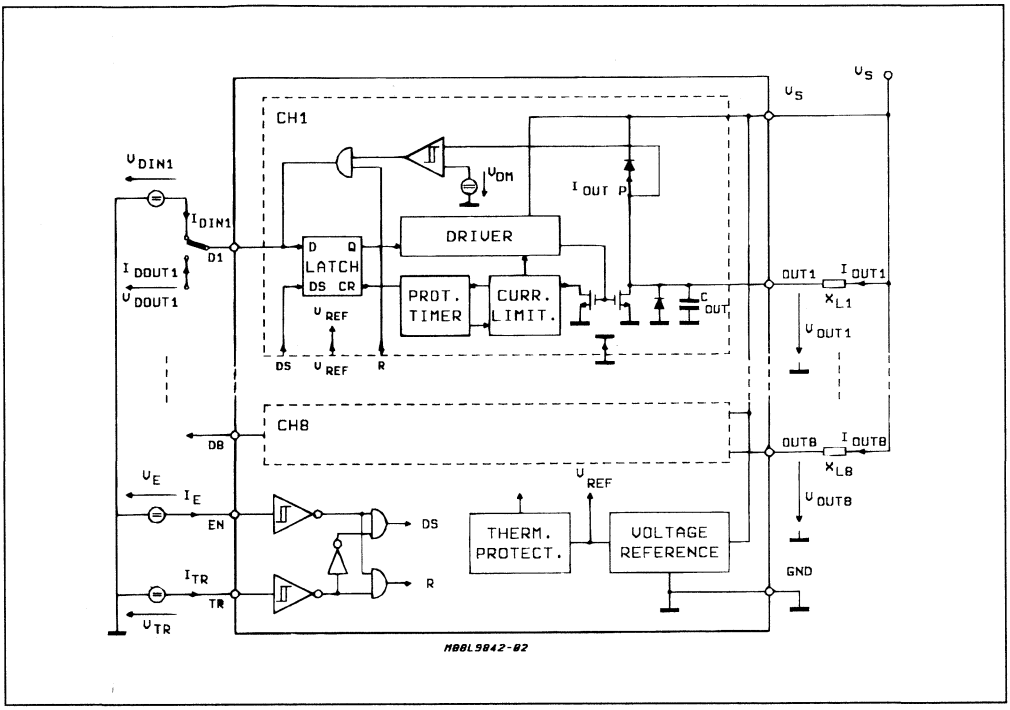


Figure 4 : Test Circuit.



FUNCTIONAL DESCRIPTIONS

This device is developed specially for automotive applications to drive different loads like relais, lamps, data buses or actuators with very low current consumption.

The L9842 contains eight identical channels each with a separate DATA input/output and the power output. In each channel the memory function, the output short circuit function and the diagnostic function is realized.

The common part determines the function modes through ENABLE and TRANSFER inputs whereas the reference part biases all current sources and generates the threshold voltages and the stabilized supply voltage for the whole CMOS-logic.

A special thermal protection, ESD-protected inputs/DATA pins and a particular output short circuit characteristic prevent a damage or the destruction of the device.

Referring to the clock diagram it can be seen that each channel works independent and contains all necessary functions described in the following points.

OUTPUT BLOCK

TRANSFER FROM DATA INPUT TO POWER OUTPUT. The DATA pins are used bidirectional. The main path is the transfer of a digital signal from the DATA pin to the power output (transfer mode). The data pass the input latch that works also as a memory in the HOLD MODE. They remain stored until the TRANSFER MODE is selected to write in new data.

This means that in all other modes the memory content will not be changed except the output short circuit protection was active more than the check time of 42.5ms. In this case the storage flip-flop will be reset to set the output for protection into the Off-state. By activating the READ MODE in this position it is possible to detect short-circuit load.

To switch on the output again the external control processor has to select the TRANSFER MODE and to change the input signal at the corresponding data terminal to "HIGH" to set the storage flip-flop and then to write in "LOW". An additional reading of this channel output (selecting the READ MODE after the mentioned check time) shows whether the short-circuit is still present.

TRANSFER FROM POWER OUTPUT TO DATA OUTPUT.The opposite signal path (READING MODE) from the output to the DATA terminals is used for the diagnostic function to monitor the output status. Output voltages greater than 3.5V lead to "HIGH" state at the DATA terminals. The HIGH level is typical 4.5V and internally stabilized. For LOW level the saturation voltage of an NPN-transistor is relevant.

SHORT-CIRCUIT PROTECTION. For the use of lamps a particular short-current characteristic is implemented that is drawn in fig. 3. Because of the low resistance of lamps during the ON-phase the current limit is for typical 2.5ms about the double as for the second current limiting phase. This prevents a switching off of this channel after the check time of 42.5ms (dotted line in fig. 3).

These time periods are generated from two frequencies 400Hz/6.4kHz coming from the common oscillator part. If the current limiting is active after the check period an overload is recognized and the regarding channel is switched off and the DATA flip-flop is also reset as explained earlier.

In order to save supply current a special short-circuit protection is used that needs no quiescent current during the ON-state as long as no overload is present at the output. Because of this special circuit configuration the output current must exceed a given threshold to activate the current regulation loop.

This current threshold I_{TH} is determined by the ON-resistance R_{DSON} of the output DMOS and the minimum operating supply voltage V_{Smin} of the limiting circuit and can be easily calculated in the following way :

$I_{TH} = V_{Smin}/R_{DSON} = 4V/1.5\Omega = \underline{2.7A}$ (typical value at $T_j = 25°C$)

When the output is shorted for instance to V = a maximum peak current will occur for a short duration up to the limiting circuit is switched on and the settling time is over. Under worst case conditions (T_j = 40°C), V_S = 16V, where R_{DSON} is lowest) the peak current can reach 7A with a duration of 1µs at V_{out} = 15V and 4A with a duration of 20µs at V_{out} = 5V.

COMMON PARTS

MODE CONTROL. By the TRANSFER and ENABLE input the working modes can be selected as shown in the truthtable in the upper part of fig. 1. The control signals coming from both input comparators which determine the logic threshold and hysteresis drive the mode logic that distributes the right data to all output blocks.

TRANSFER, HOLD and READ MODE are explained before. The remaining STANDBY MODE switches the clock oscillator and all outputs off and reduces the quiescent current below 100µA. This means that only the both mode comparators and the bandgap regulator are active. The input data stored before will be not changed.

OSCILLATOR PART. The clock oscillator contains an on-chip capacitor and requires therefore no external components. The oscillation frequency is approximately in the range of 50kHz. This oscillator signal is devided by a 7 bit-counter which creates the two frequencies for the timing of all short current control circuits in each output block.

VOLTAGE REFERENCE. The main reference cell is a bandgap controlled very low drop voltage regulator. All threshold voltages for the input comparators, the diagnostic comparators and the thermal overload comparators as well as the reference voltage for the CMOS supply buffers are derived from one resistor devider.

Because of the low current capability of the regulator two buffers are used to supply the CMOS logic for every four channels. These voltage followers work like a current multiplier at a very low quiescent current. A clamping circuit prevents that the CMOS breakdown voltage will be reached.

CURRENT REFERENCE + POWER–ON RESET. The two temperature compensated current lines are generated directly from the bandgap voltage and are switched off by the mode logic to save supply current. A third unswitched current line biases the input comparators and CMOS buffers.

During the supply voltage rise the power-on reset circuit provides a defined status of all latches in the CMOS logic. From a supply voltage of about 4V on it enables the whole logic and the device can work.

PROTECTION CIRCUITS

ESD–PROTECTION. Both input comparators (ENABLE, TRANSFER) are ESD protected and include zener diodes that clamp the gates of the internal MOSFETs to minimal 15V. Second diodes clamp these inputs to V = if the supply voltage is lower than 0.6V below the zener voltage.

The eight DATA terminals has the same ESD protection structure as the comparator inputs only with the difference that the zener diode has a clamping voltage of minimal 7V.

SHORT CURRENT LIMITING. The detailed function explanation is given in a former section where the output block is described. This kind of protection

determines the limits within the safe operating area of the used DMOS structure.

The big chip area and the heat capacity of silicon allow for short durations peak currents up to five times the maximum DC current that occur under certain conditions as expounded above.

THERMAL SHUTDOWN. Because of the symmetry and the big size of the chip two thermal overload protection circuits were placed on each side of the chip where the output structures are concentrated to ensure minimum thermal gradients to the thermal sensors.

At a chip temperature of about 160°C the device is switched off. This state is similar to the STANDBY MODE. After the temperature remains under approximately 135°C the element is switched on. The thermal shut-down does not influence any logic because it switches only the gates of all output DMOS-transistors directly to ground.

SGS-THOMSON MICROELECTRONICS

BUZ11
BUZ11FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

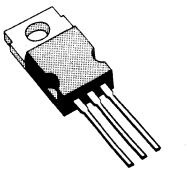
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
BUZ11	50 V	0.04 Ω	30 A
BUZ11FI	50 V	0.04 Ω	20 A

- HIGH SPEED SWITCHING
- VERY LOW ON-LOSSES
- LOW DRIVE ENERGY FOR EASY DRIVE
- HIGH TRANSCONDUCTANCE/C_{rss} RATIO

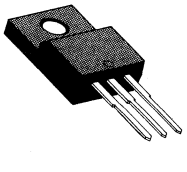
INDUSTRIAL APPLICATIONS:

- AUTOMATIVE POWER ACTUATORS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits in applications such as power actuator driving, motor drive including brushless motors, hydraulic actuators and many other uses in automotive applications. They also find use in DC/DC converters and uninterruptible power supplies.

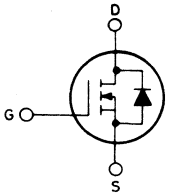


TO-220



ISOWATT 220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50		V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	50		V
V_{GS}	Gate-source voltage	±20		V
I_{DM}	Drain current (pulsed) $T_c=25°C$	120		A
		BUZ 11	**BUZ11FI**	
I_D ■	Drain current (continuous) $T_c=30°C$	30	20	A
P_{tot} ■	Total dissipation at $T_c<25°C$	75	35	W
T_{stg}	Storage temperature	−55 to 150		°C
T_j	Max. operating junction temperature	150		°C
	DIN humidity category (DIN 40040)	E		
	IEC climatic category (DIN IEC 68-1)	55/150/56		

■ See note on ISOWATT 220 in this datasheet

THERMAL DATA ▪

			TO-220	ISOWATT 220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.67	3.57	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	75		°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

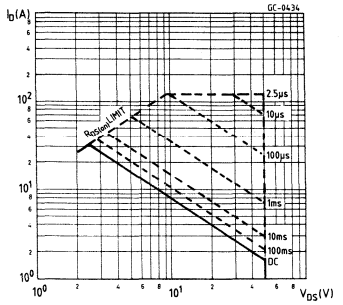
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 15 A			0.04	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 15 A	4			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 1100 400	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3 A V_{GS} = 10 V			45 110 230 170	ns ns ns ns

▪ See note on ISOWATT 220 in this datasheet

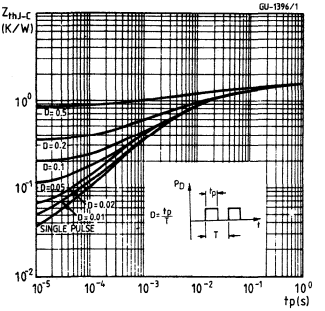
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				30 120	A A
V_{SD}	Forward on voltage	I_{SD} = 60 A	V_{GS} = 0			2.6	V
t_{rr}	Reverse recovery time				200		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 30 A	di/dt = 100A/µs		0.25		µC

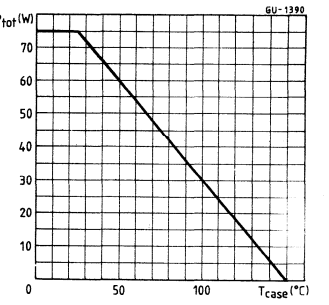
Safe operating areas (standard package)



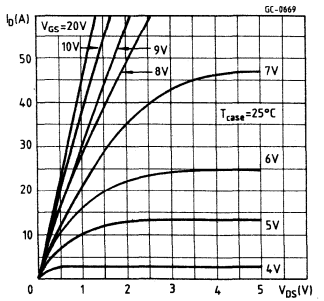
Thermal impedance (standard package)



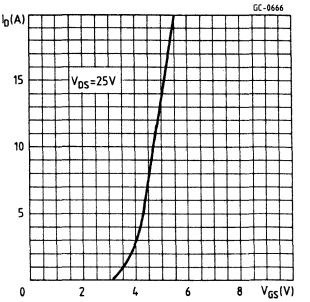
Derating curve (standard package)



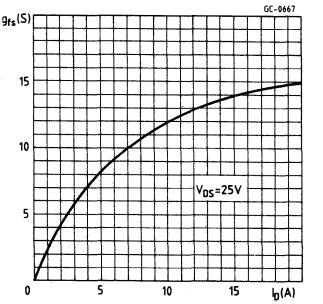
Output characteristics



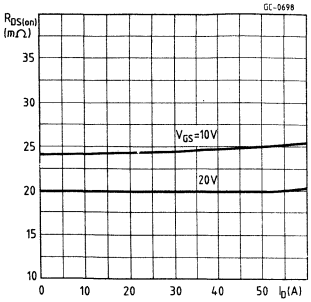
Transfer characteristics



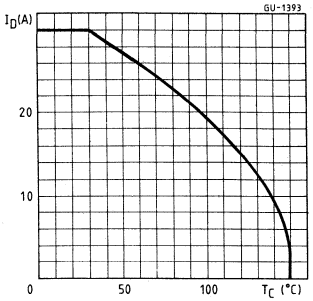
Transconductance



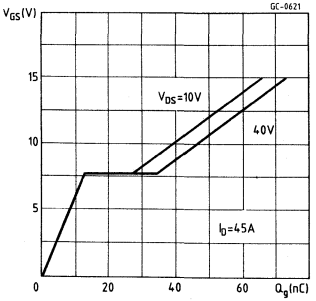
Static drain-source on resistance



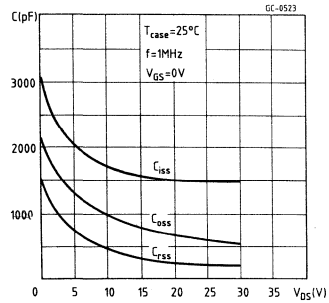
Maximum drain current vs temperature



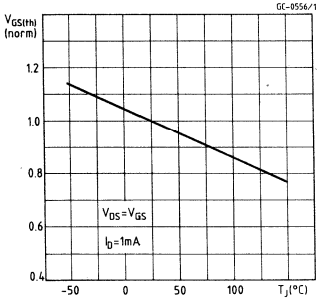
Gate charge vs gate-source voltage



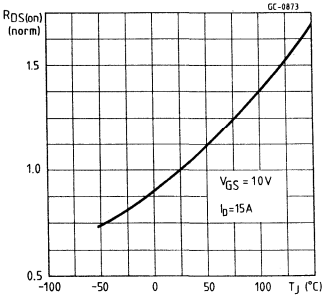
Capacitance variation



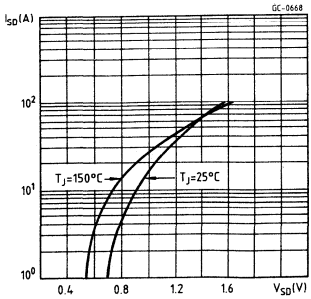
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)}\ (at\ 150°C)}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

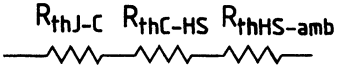
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

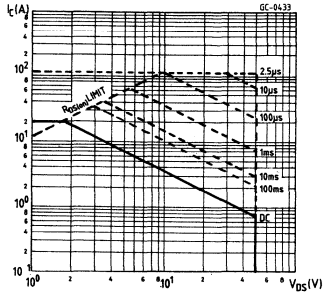
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

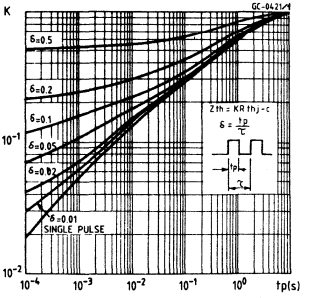


ISOWATT DATA

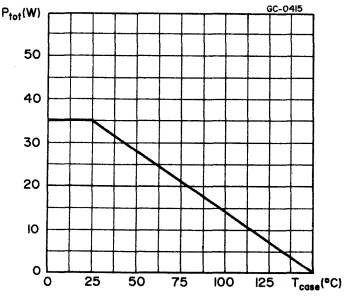
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

BUZ11A

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

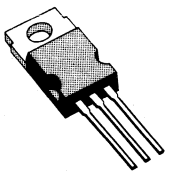
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ11A	50 V	0.06 Ω	25 A

- HIGH CURRENT
- ULTRA FAST SWITCHING
- VERY LOW ON-LOSSES
- LOW DRIVE ENERGY FOR EASY DRIVE

INDUSTRIAL APPLICATIONS:

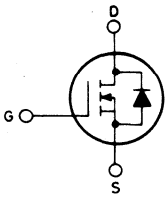
- AUTOMOTIVE POWER ACTUATORS
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical uses include power actuator driving, motor drive including brushless motors, hydraulic actuators and many other uses in automotive applications. It also finds use in DC/DC converters and uninteruptible power supplies.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	50	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c=25°C$	25	A
I_{DM}	Drain current (pulsed)	100	A
P_{tot}	Total dissipation at $T_c<25°C$	75	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1.67	°C/W
$R_{thj\text{ - amb}}$	Thermal resistance junction-ambient	max	75	°C/W

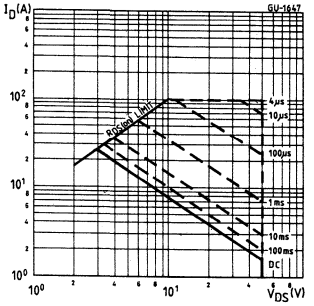
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 15 A			0.06	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 15 A	4.0			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 1100 400	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3 A V_{GS} = 10 V			45 110 230 170	ns ns ns ns

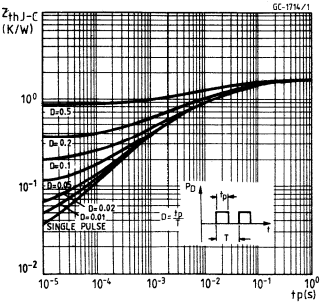
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				25 100	A A
V_{SD}	Forward on voltage	I_{SD} = 50 A	V_{GS} = 0			2.4	V
t_{rr}	Reverse recovery time	I_{SD} = 25 A	di/dt = 100A/μs		200		ns
Q_{rr}	Reverse recovered charge				0.25		μC

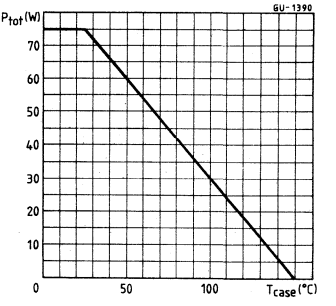
Safe operating areas



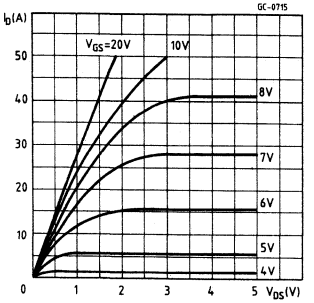
Thermal impedance



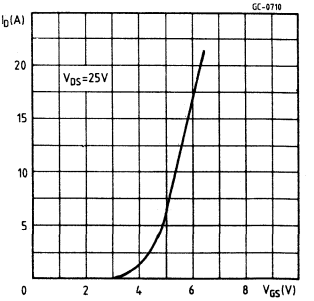
Derating curve



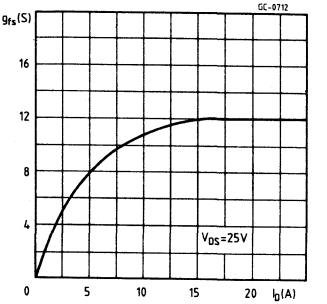
Output characteristics



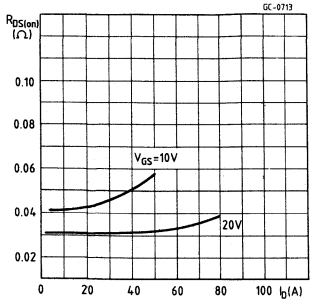
Transfer characteristics



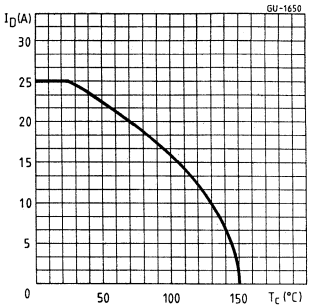
Transconductance



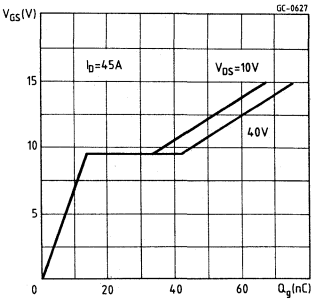
Static drain-source on resistance



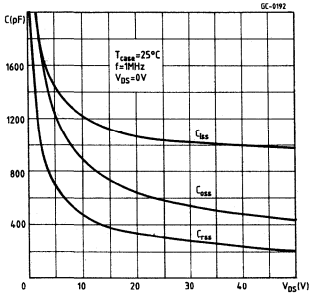
Maximum drain current vs temperature



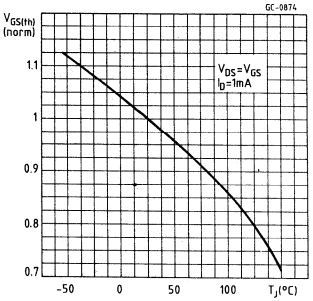
Gate charge vs gate-source voltage



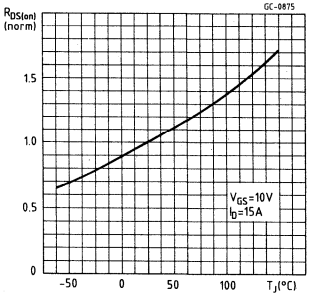
Capacitance variation



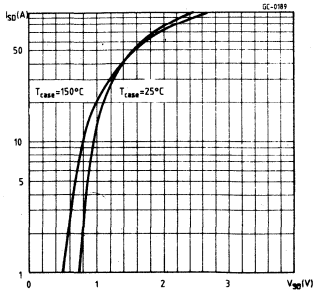
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ71A

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

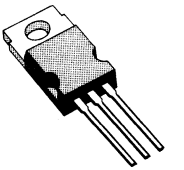
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ71A	50 V	0.12 Ω	13 A

- ULTRA FAST SWITCHING
- LOW DRIVE ENERGY FOR EASY DRIVE
- COST EFFECTIVE

INDUSTRIAL APPLICATIONS:

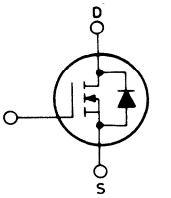
- AUTOMOTIVE POWER ACTUATORS
- MOTORS CONTROL
- INVERTERS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications such as power actuator driving, motor drive including brushless motors, hydraulic actuators and many other uses in automotive and automotive and automatic guided vehicle applications. It also finds use in DC/DC converters and uninteruptable power supplies.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	50	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c=25°C$	13	A
I_{DM}	Drain current (pulsed)	52	A
P_{tot}	Total dissipation at $T_c<25°C$	40	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	3.1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	75	°C/W

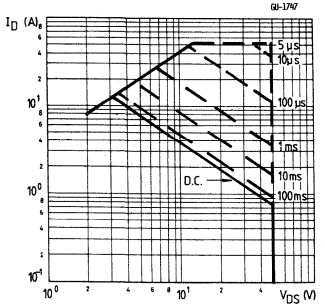
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 9 A			0.12	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 9 A	3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			650 450 280	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3 A V_{GS} = 10 V			30 85 90 110	ns ns ns ns

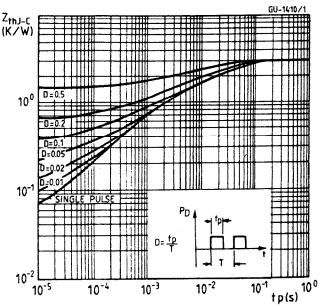
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} Source-drain current (pulsed)	T_c = 25°C			13 52	A A
V_{SD} Forward on voltage	I_{SD} = 26 A V_{GS} = 0			2.2	V
t_{rr} Reverse recovery time Q_{rr} Reverse recovered charge	I_{SD} = 13 A di/dt = 100A/μs		120 0.15		ns μC

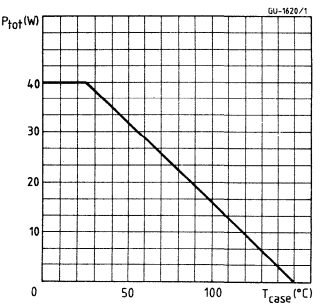
Safe operating areas



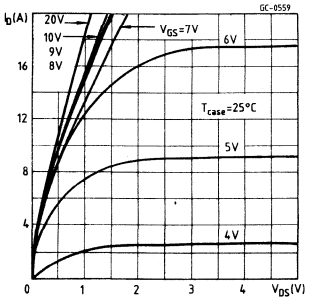
Thermal impedance



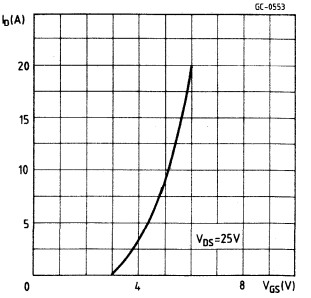
Derating curve



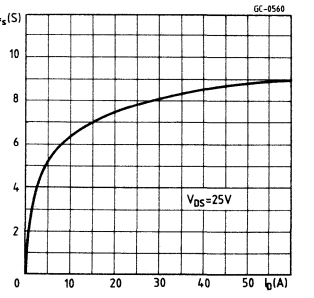
Output characteristics



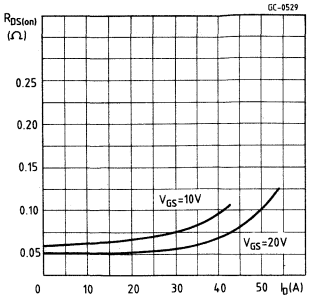
Transfer characteristics



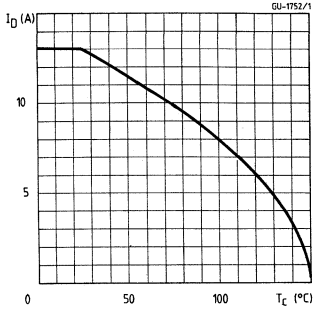
Transconductance



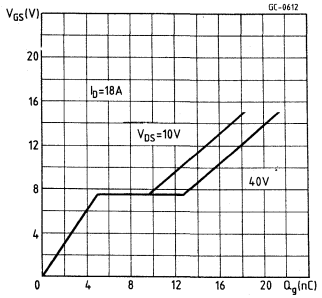
Static drain-source on resistance



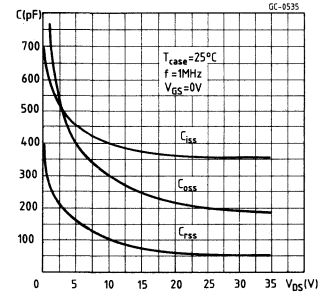
Maximum drain current vs temperature



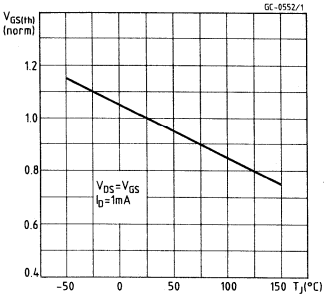
Gate charge vs gate-source voltage



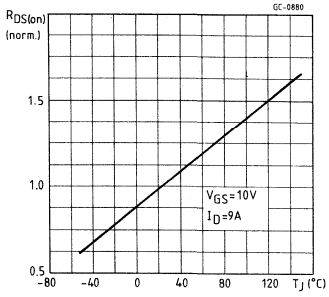
Capacitance variation



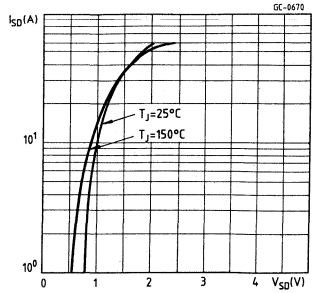
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

IRF 520/FI-521/FI
IRF 522/FI-523/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

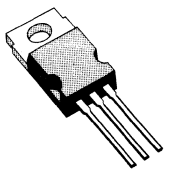
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF520	100 V	0.27 Ω	9.2 A
IRF520FI	100 V	0.27 Ω	7 A
IRF521	80 V	0.27 Ω	9.2 A
IRF521FI	80 V	0.27 Ω	7 A
IRF522	100 V	0.36 Ω	8 A
IRF522FI	100 V	0.36 Ω	6 A
IRF523	80 V	0.36 Ω	8 A
IRF523FI	80 V	0.36 Ω	6 A

- 80-100 VOLTS - FOR DC/DC CONVERTERS
- HIGH CURRENT
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE- FOR REDUCED COST AND SIZE

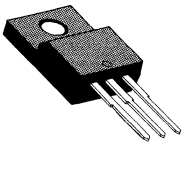
INDUSTRIAL APPLICATIONS:

- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC/DC converters, UPS, battery chargers, secondary regulators, servo control, power-audio amplifiers and robotics.

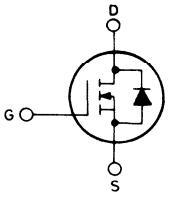


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		IRF 520 / 520FI (TO-220 / ISOWATT220)	IRF 521 / 521FI	IRF 522 / 522FI	IRF 523 / 523FI	
V_{DS} *	Drain-source voltage (V_{GS} = 0)	100	80	100	80	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)	100	80	100	80	V
V_{GS}	Gate-source voltage	±20				V
I_{DM} (•)	Drain current (pulsed)	37	37	32	32	A
		520	521	522	523	
I_D	Drain current (cont.) at T_c = 25°C	9.2	9.2	8	8	A
I_D	Drain current (cont.) at T_c = 100°C	6.5	6.5	5.6	5.6	A
		520FI	521FI	522FI	523FI	
I_D ■	Drain current (cont.) at T_c = 25°C	7	7	6	6	A
I_D ■	Drain current (cont.) at T_c = 100°C	4	4	3.5	3.5	A
		TO-220		ISOWATT220		
P_{tot} ■	Total dissipation at T_c < 25°C	60		30		W
■	Derating factor	0.48		0.24		W/°C
T_{stg}	Storage temperature	−55 to 150				°C
T_j	Max. operating junction temperature	150				°C

* T_j = 25°C to 125°C
(•) Repetitive Rating: Pulse width limited by max junction temperature.
■ See note on ISOWATT220 on this datasheet.
◆ Introduced in 1988 week 44

THERMAL DATA ▪

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	2.08	4.16	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

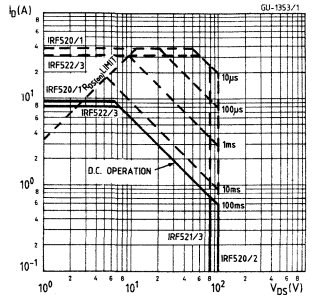
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF520/522/520FI/522FI** for **IRF521/523/521FI/523FI**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF520/521/520FI/521FI** for **IRF521/523/521FI/523FI**	 9.2 8			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 5.6 A for **IRF520/521/520FI/521FI** for **IRF522/523/522FI/523FI**			 0.27 0.36	 Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **IRF520/521/520FI/521FI** for **IRF522/523/522FI/523FI**	 9.2 8			 A A
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 5.6 A	2.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			600 400 100	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

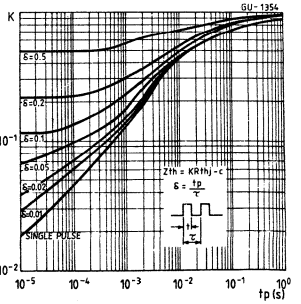
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 40 V I_D = 4.0 A R_i = 50 Ω (see test circuit)			40 70 100 70	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 15 V I_D = 9.2 A V_{DS} = Max Rating × 0.8 (see test circuit)			15	nC
SOURCE DRAIN DIODE						
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)				9.2 37	A A
V_{SD} **	Forward on voltage	I_{SD} = 9.2 A V_{GS} = 0			2.5	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovered charge	T_j = 150°C I_{SD} = 9.2 A di/dt = 100 A/μs		280 1.6		ns μC

** Pulsed: Pulse duration ⩽ 300 μs, duty cycle ⩽ 1.2%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

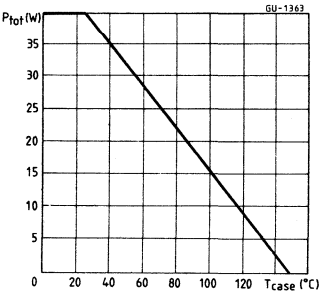
Safe operating areas (standard package)



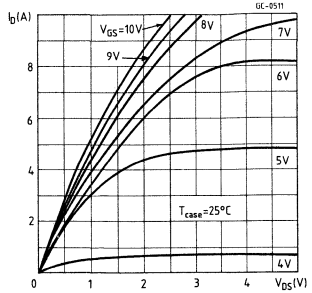
Thermal impedance (standard package)



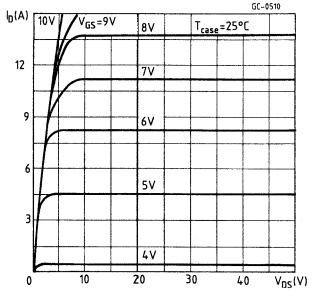
Derating curve (standard package)



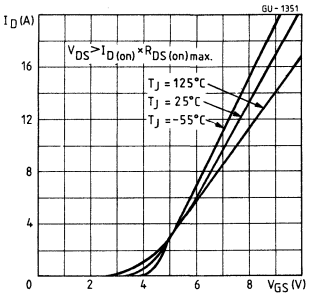
Output characteristics



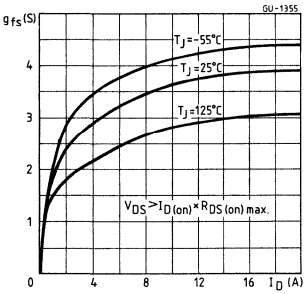
Output characteristics



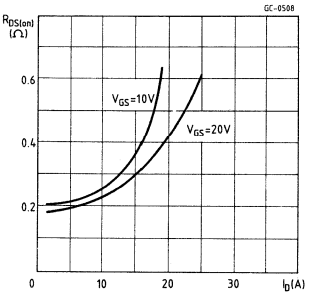
Transfer characteristics



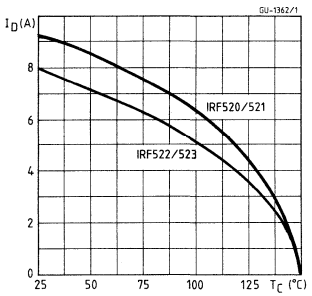
Transconductance



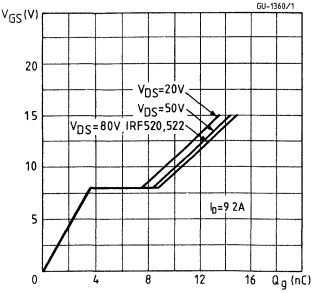
Static drain-source on resistance



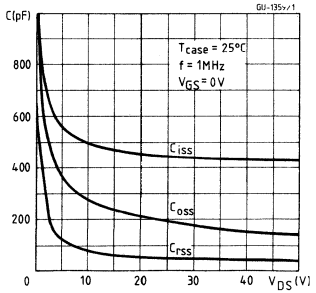
Maximum drain current vs temperature



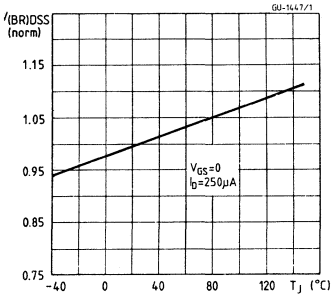
Gate charge vs gate-source voltage



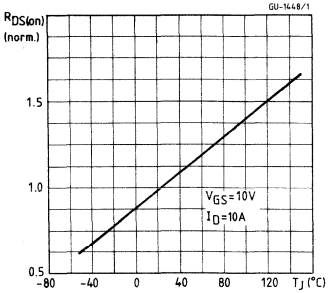
Capacitance variation



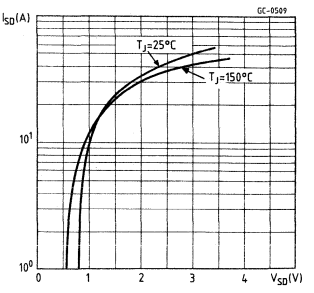
Normalized breakdown voltage vs temperature



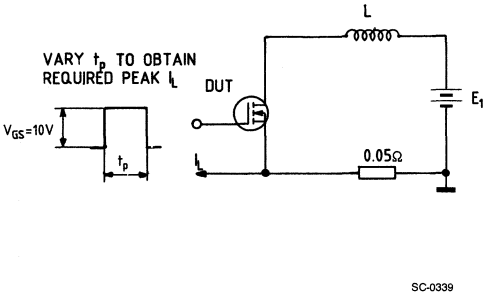
Normalized on resistance vs temperature



Source-drain diode forward characteristics

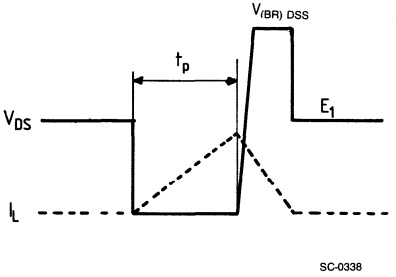


Unclamped inductive test circuit



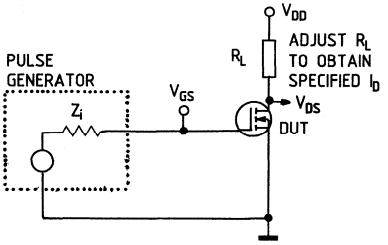
SC-0339

Unclamped inductive waveforms



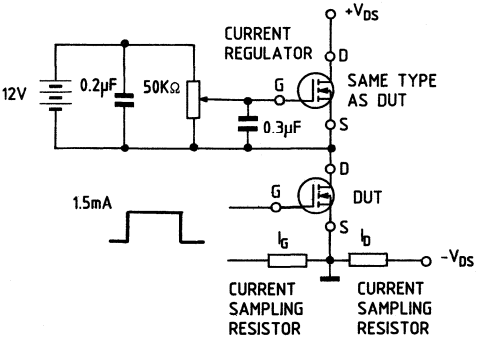
SC-0338

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)}\ (\text{at } 150°C)}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

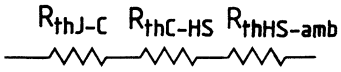
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

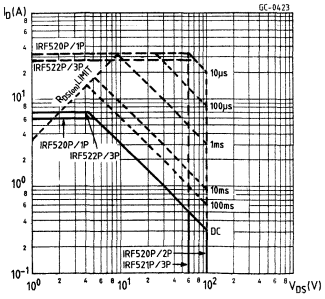
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

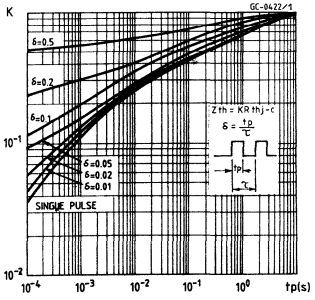


ISOWATT DATA

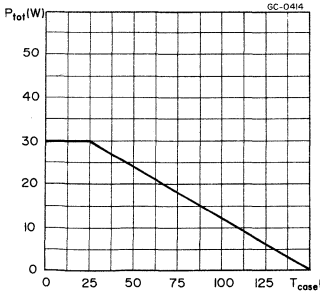
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRF 530/FI-531/FI
IRF 532/FI-533/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

PRELIMINARY DATA

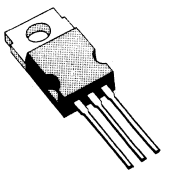
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF530	100 V	0.16 Ω	14 A
IRF530FI	100 V	0.16 Ω	9 A
IRF531	80 V	0.16 Ω	14 A
IRF531FI	80 V	0.16 Ω	9 A
IRF532	100 V	0.23 Ω	12 A
IRF532FI	100 V	0.23 Ω	8 A
IRF533	80 V	0.23 Ω	12 A
IRF533FI	80 V	0.23 Ω	8 A

- 80-100 VOLTS - FOR DC/DC CONVERTERS
- HIGH CURRENT
- ULTRA FAST SWITCHING
- EASY DRIVE- FOR REDUCED COST AND SIZE

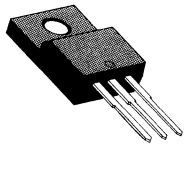
INDUSTRIAL APPLICATIONS:

- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC/DC converters, UPS, battery chargers, secondary regulators, servo control, power-audio amplifiers and robotics.

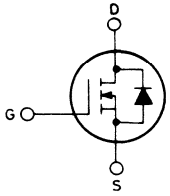


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		IRF 530 / 530FI	IRF 531 / 531FI	IRF 532 / 532FI	IRF 533 / 533FI	
		TO-220 / ISOWATT220				
V_{DS} *	Drain-source voltage (V_{GS} = 0)	100	80	100	80	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)	100	80	100	80	V
V_{GS}	Gate-source voltage	±20				V
I_{DM} (•)	Drain current (pulsed)	56	56	48	48	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)	56	56	48	48	A
		530	**531**	**532**	**533**	
I_D	Drain current (cont.) at T_c = 25°C	14	14	12	12	A
I_D	Drain current (cont.) at T_c = 100°C	9	9	8	8	A
		530FI	**531FI**	**532FI**	**533FI**	
I_D ■	Drain current (cont.) at T_c = 25°C	9	9	8	8	A
I_D ■	Drain current (cont.) at T_c = 100°C	5.5	5.5	5	5	A
		TO-220		**ISOWATT220**		
P_{tot} ■	Total dissipation at T_c < 25°C	79		35		W
■	Derating factor	0.63		0.28		W/°C
T_{stg}	Storage temperature	−55 to 150				°C
T_j	Max. operating junction temperature	150				°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.58	3.57	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF530/532/530FI/532FI** for **IRF531/533/531FI/533FI**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ x $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF530/531/530FI/531FI** for **IRF532/533/532FI/533FI**	 14 12			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 8.3 A for **IRF530/531/530FI/531FI** for **IRF532/533/532FI/533FI**			 0.16 0.23	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ x $R_{DS\ (on)\ max}$ I_D = 8.3 A	5.1			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			850 260 50	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 36 V I_D = 8.0 A R_i = 15 Ω (see test circuit)			30 75 40 45	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 14 A V_{DS} = Max Rating x 0.8 (see test circuit)			30	nC

ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				14 56	A A
V_{SD} ** Forward on voltage	I_{SD} = 14 A V_{GS} = 0			2.5	V
t_{rr} Reverse recovery time	T_j = 150°C		360		ns
Q_{rr} Reverse recovered charge	I_{SD} = 14 A di/dt = 100 A/μs		21		μC

** Pulsed: Pulse duration ≤ 300 μs, duty cycle ≤ 2%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

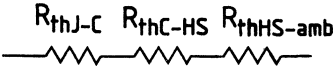
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1



SGS-THOMSON MICROELECTRONICS

IRF 540/FI-541/FI
IRF 542/FI-543/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF540	100 V	0.077 Ω	28 A
IRF540FI	100 V	0.077 Ω	15 A
IRF541	80 V	0.077 Ω	28 A
IRF541FI	80 V	0.077 Ω	15 A
IRF542	100 V	0.100 Ω	25 A
IRF542FI	100 V	0.100 Ω	14 A
IRF543	80 V	0.100 Ω	25 A
IRF543FI	80 V	0.100 Ω	14 A

- 80-100 VOLTS - FOR DC/DC CONVERTERS
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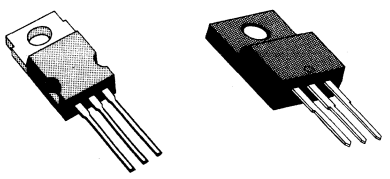
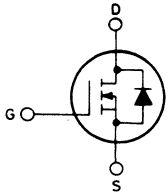


TO-220 **ISOWATT220**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	IRF 540 / 540FI	IRF 541 / 541FI	IRF 542 / 542FI	IRF 543 / 543FI	
V_{DS} *	Drain-source voltage (V_{GS} = 0)		100	80	100	80	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)		100	80	100	80	V
V_{GS}	Gate-source voltage		±20				V
I_{DM} (•)	Drain current (pulsed)		110	110	100	100	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)		110	110	100	100	A
			540	**541**	**542**	**543**	
I_D	Drain current (cont.) at T_c = 25°C		28	28	25	25	A
I_D	Drain current (cont.) at T_c = 100°C		20	20	17	17	A
			540FI	**541FI**	**542FI**	**543FI**	
I_D ■	Drain current (cont.) at T_c = 25°C		15	15	14	14	A
I_D ■	Drain current (cont.) at T_c = 100°C		9	9	8	8	A
			TO-220		**ISOWATT220**		
P_{tot} ■	Total dissipation at T_c < 25°C		125		40		W
■	Derating factor		1		0.32		W/°C
T_{stg}	Storage temperature		−55 to 150				°C
T_j	Max. operating junction temperature		150				°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1	3.12	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

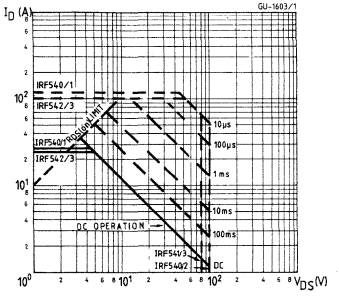
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF540/542/540FI/542FI** for **IRF541/543/541FI/543FI**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ x $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF540/541/540FI/541FI** for **IRF542/543/542FI/543FI**	 28 25			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 17 A for **IRF540/541/540FI/541FI** for **IRF542/543/542FI/543FI**			 0.077 0.100	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ x $R_{DS\ (on)\ max}$ I_D = 17 A	8.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			1600 800 300	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V I_D = 15 A R_i = 4.7 Ω (see test circuit)			30 60 80 30	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 28 A V_{DS} = Max Rating x 0.8 (see test circuit)			59	nC

ELECTRICAL CHARACTERISTICS (Continued)

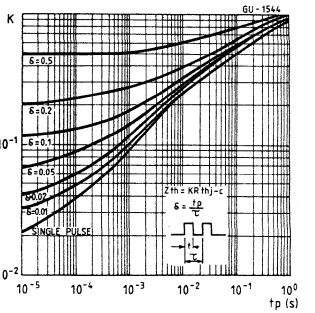
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				28 110	A A
V_{SD} ** Forward on voltage	I_{SD} = 28 A V_{GS} = 0			2.5	V
t_{rr} Reverse recovery time	T_j = 150°C		500		ns
Q_{rr} Reverse recovered charge	I_{SD} = 28 A di/dt = 100 A/µs		2.9		µC

** Pulsed: Pulse duration ≤ 300 µs, duty cycle ≤ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

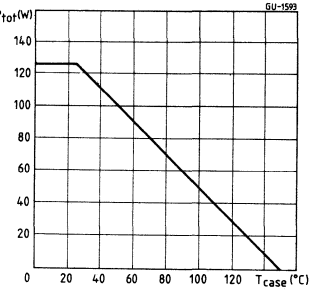
Safe operating areas (standard package)



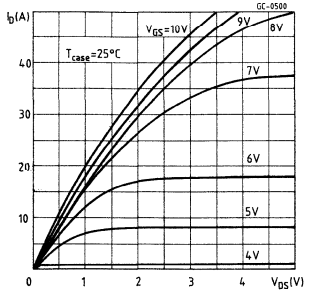
Thermal impedance (standard package)



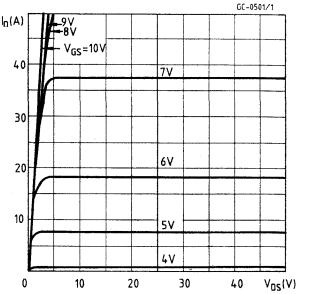
Derating curve (standard package)



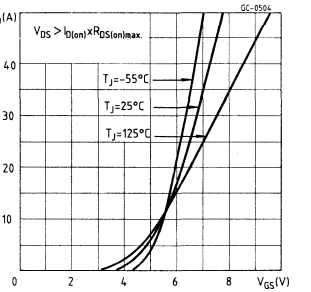
Output characteristics



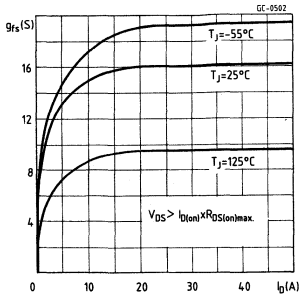
Output characteristics



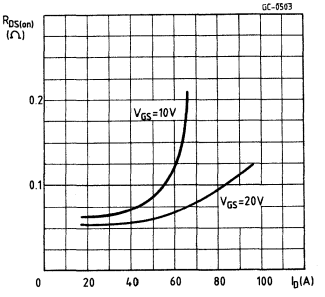
Transfer characteristics



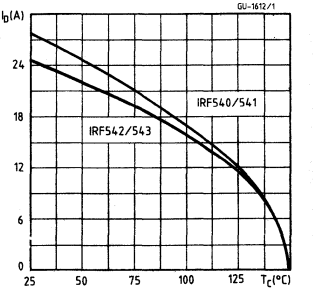
Transconductance



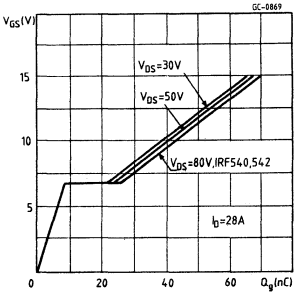
Static drain-source on resistance



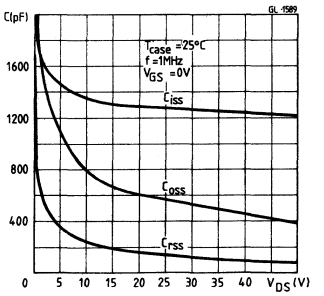
Maximum drain current vs temperature



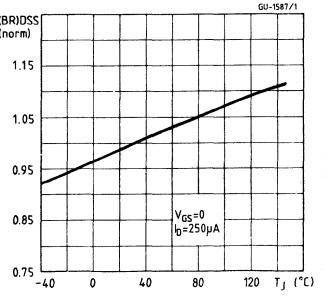
Gate charge vs gate-source voltage



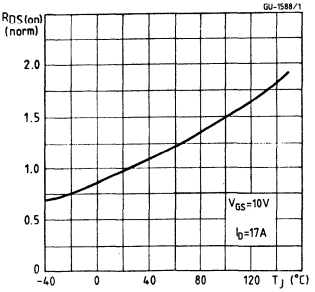
Capacitance variation



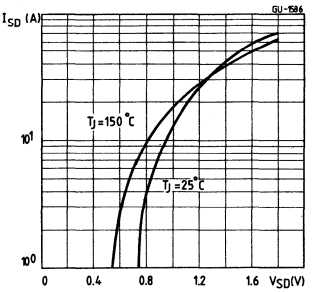
Normalized breakdown voltage vs temperature



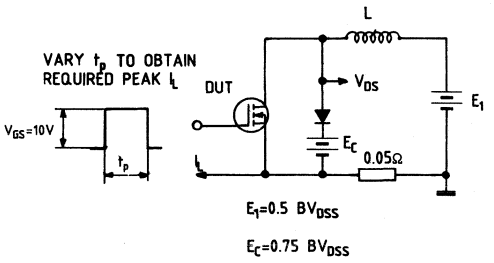
Normalized on resistance vs temperature



Source-drain diode forward characteristics

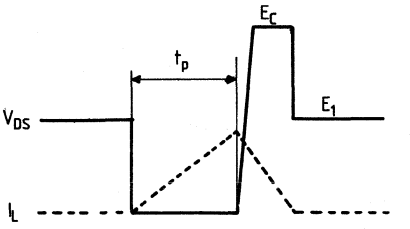


Clamped inductive test circuit



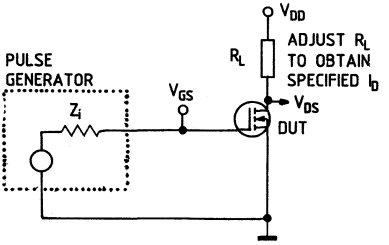
SC-0242

Clamped inductive waveforms



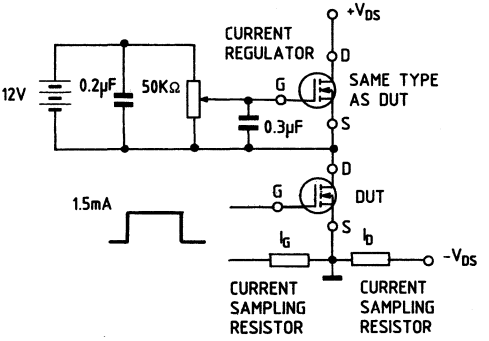
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

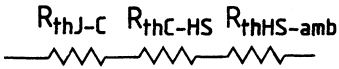
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

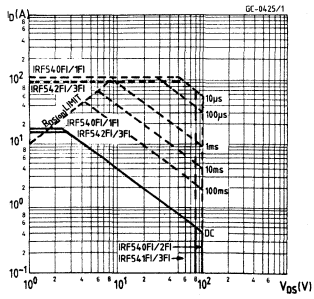
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

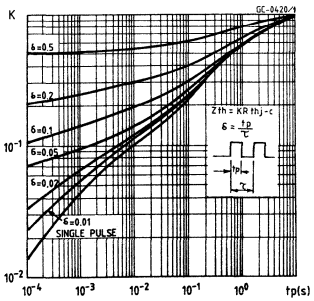


ISOWATT DATA

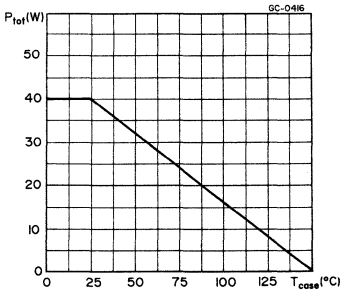
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRFZ40
IRFZ42

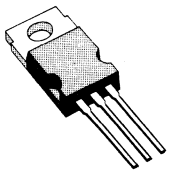
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRFZ40	50 V	0.028 Ω	35 A
IRFZ42	50 V	0.035 Ω	35 A

- VERY LOW $R_{DS\ (on)}$
- LOW DRIVE ENERGY FOR EASY DRIVE
- HIGH TRANSCONDUCTANCE /C_{rss} RATIO

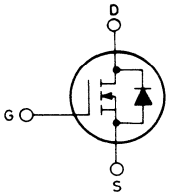
INDUSTRIAL APPLICATIONS:

- AUTOMOTIVE POWER ACTUATORS
- MOTOR CONTROLS
- INVERTERS



TO-220

INTERNAL SCHEMATIC DIAGRAM



N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits applications such as power actuators driving, motor drive including brushless motor, hydraulic actuators and many other in automotive and automatic guided vehicle applications. They also find use DC/DC converters and uninterruptible power supplies

ABSOLUTE MAXIMUM RATINGS

		IRFZ40	IRFZ42	
V_{DS} *	Drain-source voltage ($V_{GS}=0$)	50		V
V_{DGR} *	Drain-gate voltage ($R_{GS}=20$ KΩ)	50		V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	35	35	A
I_D	Drain current (cont.) at $T_c=100°C$	32	29	A
I_{DM}(•)	Drain current (pulsed)	160	145	A
I_{DLM}	Drain inductive current, clamped (L= 100 μH)	160	145	A
P_{tot}	Total dissipation at $T_c<25°C$	125		W
	Derating factor	1.2		W/°C
T_{stg}	Storage temperature	−55 to 150		°C
T_j	Max. operating junction temperature	150		°C

* T_j = 25°C to 125°C
(•) Repetitive Rating: Pulse width limited by max junction temperature

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.0	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
T_l	Maximum lead temperature for soldering purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

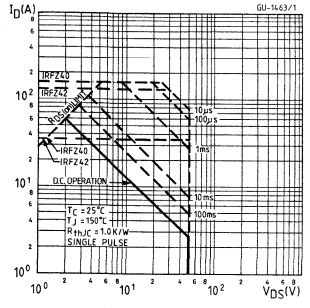
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ x $R_{DS(on)\ max}$ V_{GS} = 10 V	35			A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D ≃ 29 A for **IRFZ40** for **IRFZ42**			 0.028 0.035	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ x $R_{DS\ (on)\ max}$ I_D = 29 A	17			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			3000 1200 400	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 29 A Z_i = 4.7 Ω (see test circuit)			25 60 70 25	ns ns ns ns
Q_g	Total gate charge	V_{GS} = 10 V I_D = 64 A V_{DS} = Max Rating x 0.8 (see test circuit)			60	nC

ELECTRICAL CHARACTERISTICS (Continued)

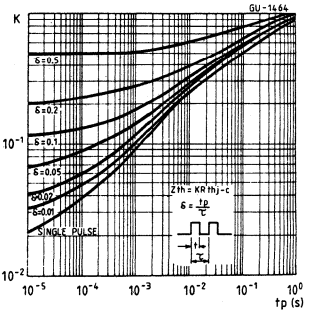
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)	for **IRFZ40** for **IRFZ42**			35 160 145	A A A
V_{SD} ** Forward on voltage	V_{GS} = 0 for **IRFZ40** I_{SD} = 51 A for **IRFZ42** I_{SD} = 46 A			2.5 2.2	V V
t_{rr} Reverse recovery time Q_{rr} Reverse recovered charge	T_j = 150°C I_{SD} = 51 A di/dt = 100 A/μs		350 2.1		ns μC

** Pulsed: Pulse duration ⩽ 300 μs, duty cycle ⩽ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature

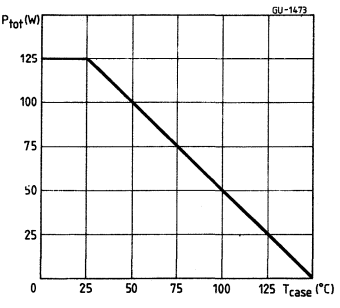
Safe operating areas



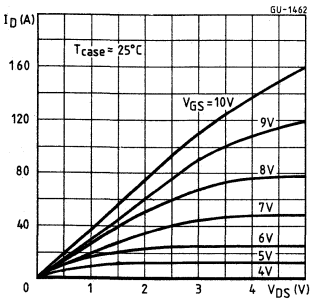
Thermal impedance



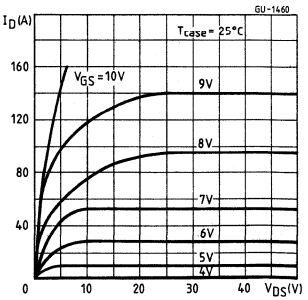
Derating curve



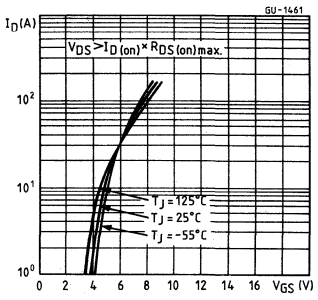
Output characteristics



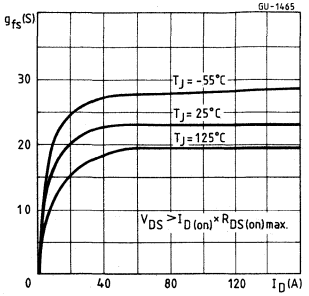
Output characteristics



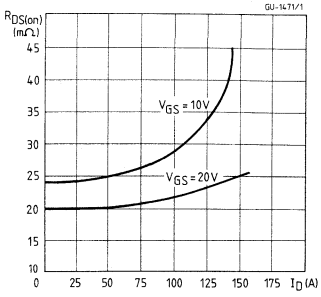
Transfer characteristics



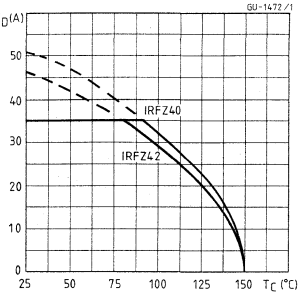
Transconductance



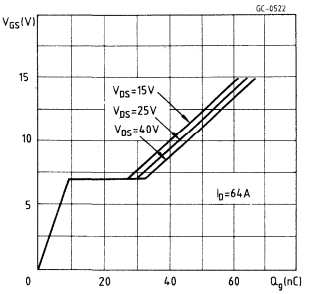
Static drain-source on resistance



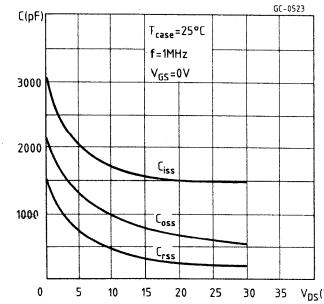
Maximum drain current vs temperature



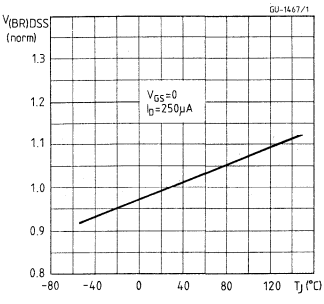
Gate charge vs gate-source voltage



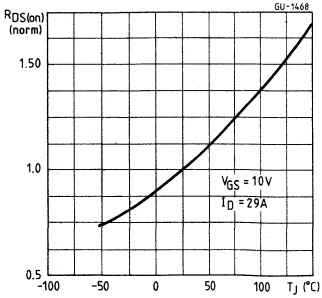
Capacitance variation



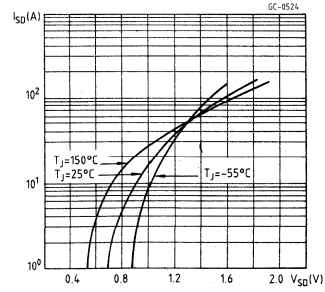
Normalized breakdown voltage vs temperature



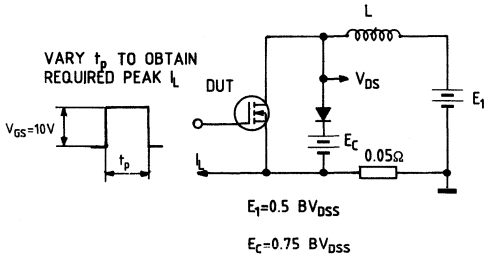
Normalized on resistance vs temperature



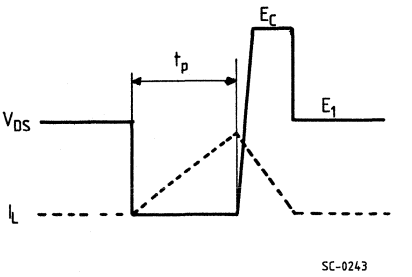
Source-drain diode forward characteristics



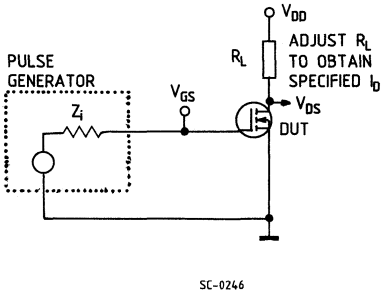
Clamped inductive test circuit



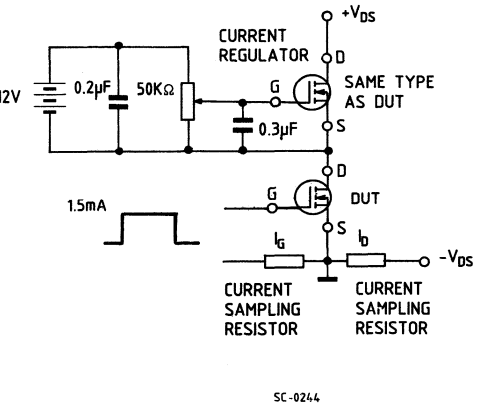
Clamped inductive waveforms



Switching times test circuit



Gate charge test circuit



SGS-THOMSON MICROELECTRONICS

MTP3055A
MTP3055AFI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

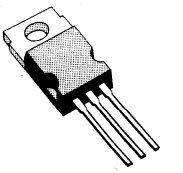
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
MTP3055A	60 V	0.15 Ω	12 A
MTP3055AFI	60 V	0.15 Ω	10 A

- ULTRA FAST SWITCHING - UP TO > 100KHz
- LOW DRIVE ENERGY FOR EASY DRIVE REDUCES SIZE AND COST
- INTEGRAL SOURCE - DRAIN DIODE

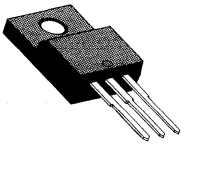
INDUSTRIAL APPLICATIONS:

- GENERAL PURPOSE SWITCH
- SERIES REGULATOR

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast times make these POWER MOS transistors ideal for high speed switching circuit in applications such as power actuator driving, motor drive including brushless motors, robotics, actuators lamp driving, series regulator and many other uses in industrial control applications. They also find use in DC/DC converters and uninterruptible power supplies.

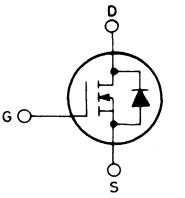


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	MTP3055A / MTP3055AFI	
V_{DS}	Drain-source voltage ($V_{GS}=0$)		60	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)		60	V
V_{GS}	Gate-source voltage		±20	V
I_{DM}	Drain current (pulsed)		26	A
I_{GM}	Gate current (pulsed)		1.5	A
		TO-220	**ISOWATT220**	
I_D ■	Drain current (continuous)	12	10	A
P_{tot} ■	Total dissipation at T_c <25°C	40	30	W
■	Derating factor	0.32	0.24	W/°C
T_{stg}	Storage temperature		−65 to 150	°C
T_j	Max. operating junction temperature		150	°C

■ See note on ISOWATT220 in this datasheet

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	3.12	4.16	°C/W
T_l	Maximum lead temperature for soldering purpose	max	275		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			50 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON *						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA V_{DS} = V_{GS} I_D = 1 mA T_c = 100°C	2 1.5		4.5 4	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 6 A		0.15	Ω	
$V_{DS\ (on)}$	Drain-source on voltage	V_{GS} = 10 V I_D = 12 A V_{GS} = 10 V I_D = 6 A V_{GS} = 10 V I_D = 6 A T_c = 100°C			2.0 0.9 1.5	V V V
DYNAMIC						
g_{fs}*	Forward transconductance	V_{DS} = 10 V I_D = 6 A	4.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			500 200 100	pF pF pF
Q_g	Total gate charge	V_{DS} = 48 V I_D = 12A V_{GS} = 10 V			17	nC
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 6 A R_{gen} = 50 Ω			20 60 65 65	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit

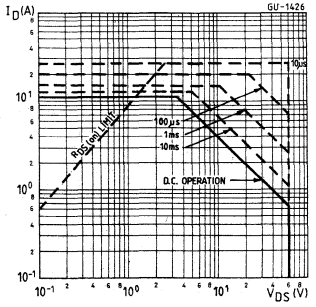
SOURCE DRAIN DIODE

V_{SD}	Forward on voltage	I_{SD} = 12 A	V_{GS} = 0			2	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A	V_{GS} = 0			75	ns

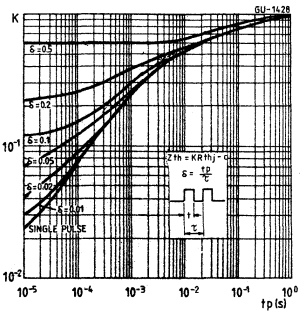
* Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 2%

■ See note on ISOWATT220 in this datasheet

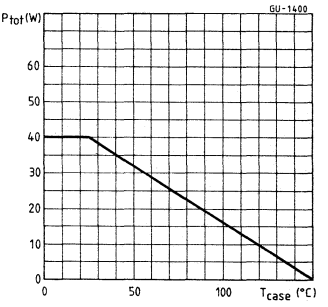
Safe operating areas (standard package)



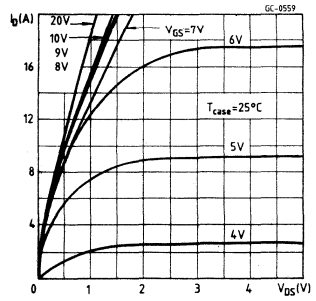
Thermal impedance (standard package)



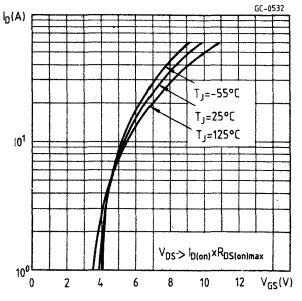
Derating curve (standard package)



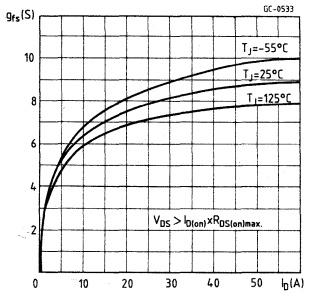
Output characteristics



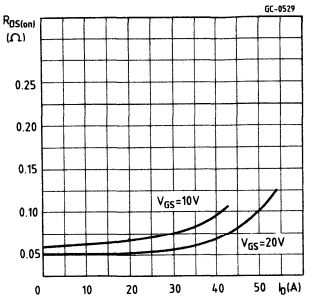
Transfer characteristics



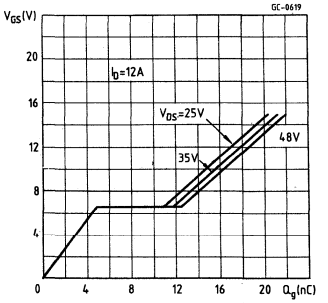
Transconductance



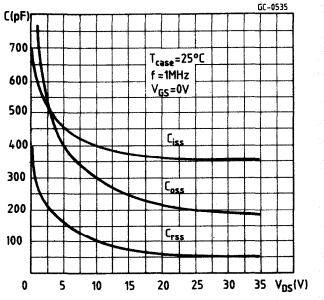
Static drain-source on resistance



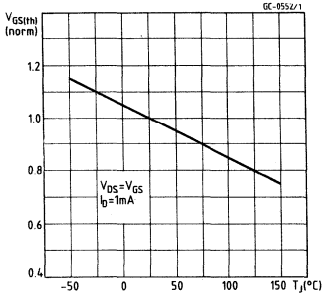
Gate charge vs gate-source voltage



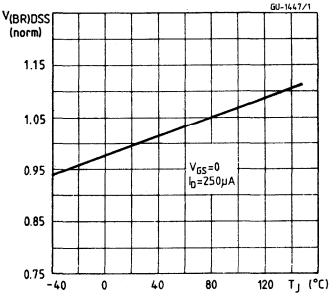
Capacitance variation



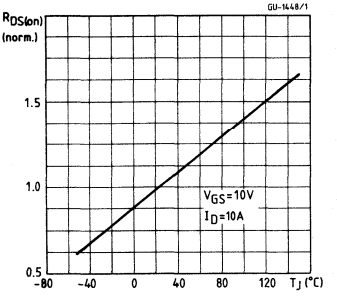
Normalized gate threshold voltage vs temperature



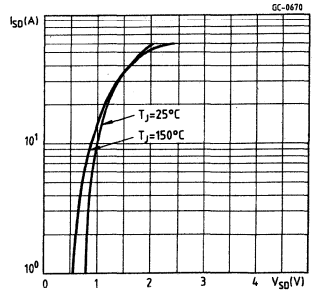
Normalized breakdown voltage vs temperature



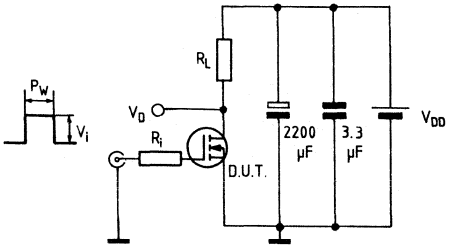
Normalized on resistance vs temperature



Source-drain diode forward characteristics

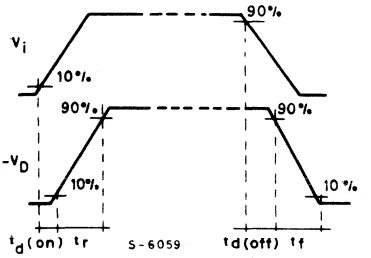


Switching times test circuit for resistive load

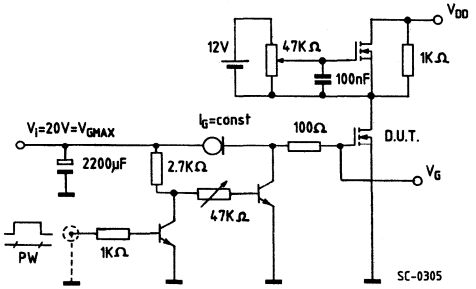


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

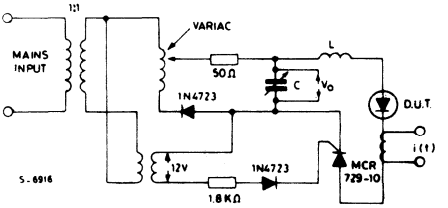


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)}\ (at\ 150°C)}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

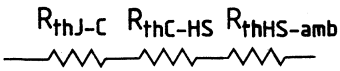
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

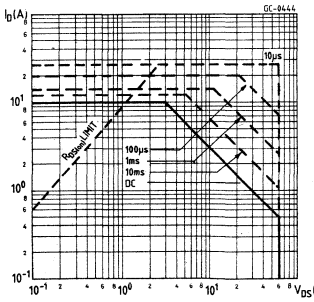
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

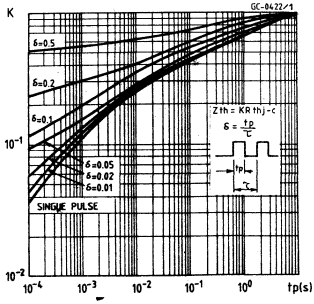


ISOWATT DATA

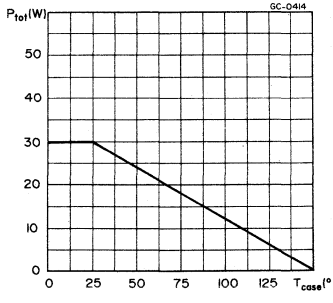
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

SGSP201

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

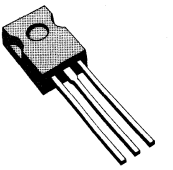
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP201	100 V	1.4 Ω	2.0 A

- HIGH SPEED SWITCHING APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

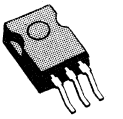
INDUSTRIAL APPLICATIONS:

- GENERAL PURPOSE SWITCHING

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include general purpose low voltage switching, solenoid driving, motor and lamp control, switching power supplies, and driving, bipolar power switching transistors.

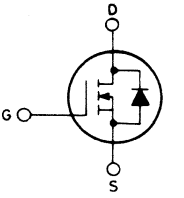


SOT-82



OPTION SOT-194

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	2.0	A
I_D	Drain current (cont.) at $T_c=100°C$	1.2	A
I_{DM} (•)	Drain current (pulsed)	6	A
I_{DLM} (•)	Drain inductive current, clamped	6	A
P_{tot}	Total dissipation at $T_c<25°C$	18	W
	Derating factor	0.144	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	6.95	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

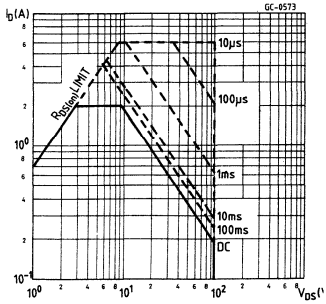
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1.2 A V_{GS} = 10 V I_D = 1.2 A T_c = 100°C			1.4 2.8	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 1.2 A	0.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		90	125 45 30	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 50 V I_D = 1.2 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		10 20 15 15	15 30 20 20	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

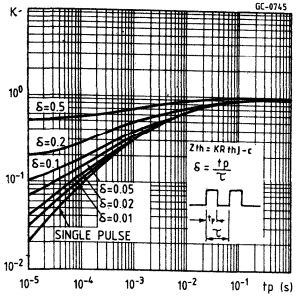
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (*) Source-drain current (pulsed)				2.0 6	A A
V_{SD} Forward on voltage	I_{SD} = 2.0 A V_{GS} = 0			1.35	V
t_{rr} Reverse recovery time	I_{SD} = 2.0 A V_{GS} = 0 di/dt = 25 A/μs		90		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

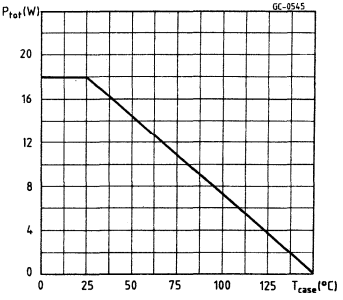
Safe operating areas



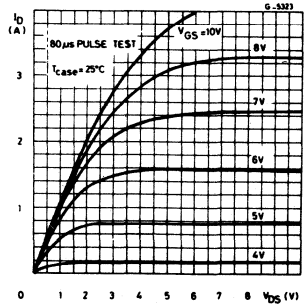
Thermal impedance



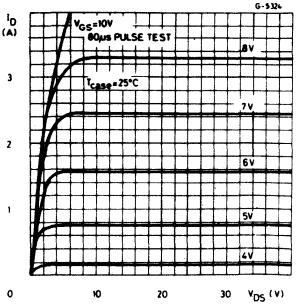
Derating curve



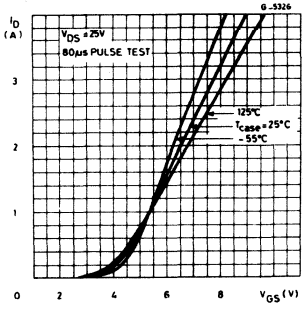
Output characteristics



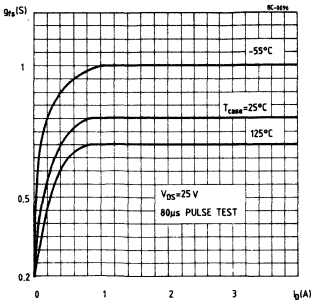
Output characteristics



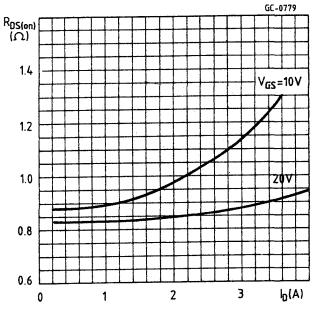
Transfer characteristics



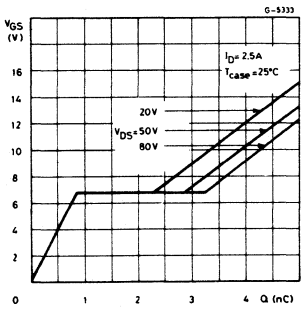
Transconductance



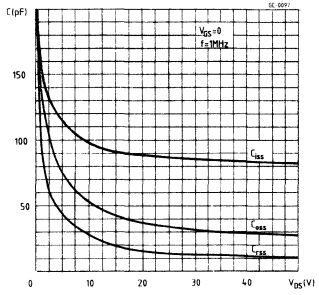
Static drain-source on resistance



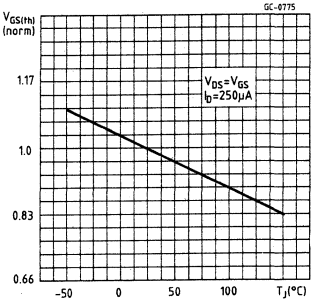
Gate charge vs gate-source voltage



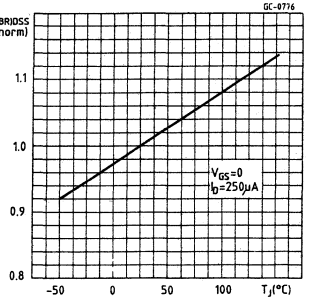
Capacitance variation



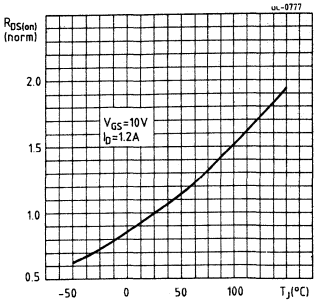
Normalized gate threshold voltage vs temperature



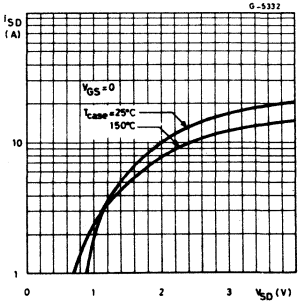
Normalized breakdown voltage vs temperature



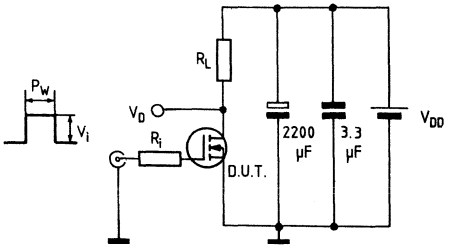
Normalized on resistance vs temperature



Source-drain diode forward characteristics

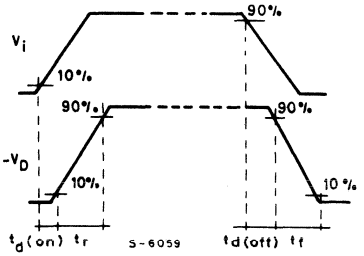


Switching times test circuit for resistive load

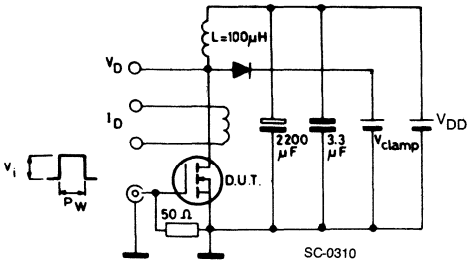


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

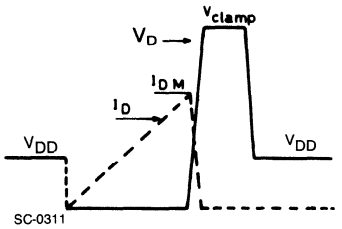


Clamped inductive load test circuit

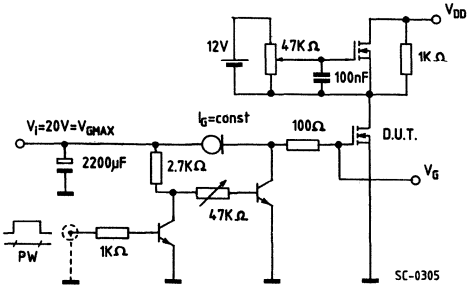


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

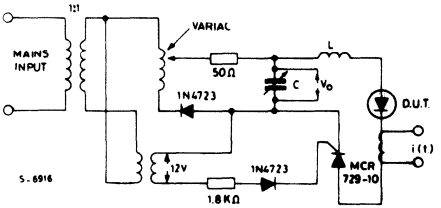


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP222

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

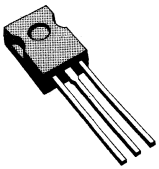
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP222	50 V	0.13 Ω	10 A

- HIGH SPEED SWITCHING APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

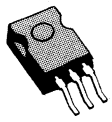
INDUSTRIAL APPLICATIONS:

- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS.

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Uses include general motor speed control, low voltage DC/DC converters and solenoid driving.

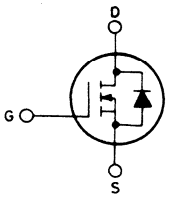


SOT-82



OPTION SOT-194

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	50	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	10	A
I_D	Drain current (cont.) at $T_c=100°C$	6.3	A
I_{DM} (•)	Drain current (pulsed)	40	A
I_{DLM} (•)	Drain inductive current, clamped	40	A
P_{tot}	Total dissipation at $T_c<25°C$	50	W
	Derating factor	0.4	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	2.5	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 5 A V_{GS} = 10 V I_D = 5 A T_c = 100°C			0.13 0.26	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 5 A	3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		460	550 350 180	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 5 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		15 40 40 20	20 55 55 30	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

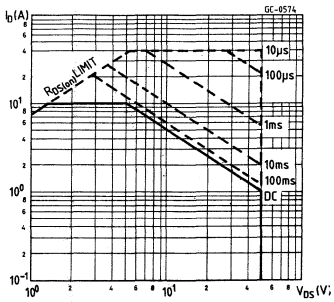
Parameters	Test Conditions	Min.	Typ.	Max.	Unit

SOURCE DRAIN DIODE

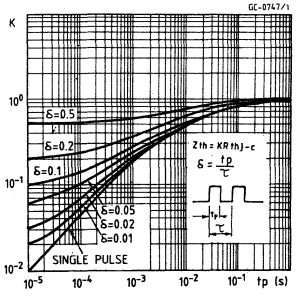
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)				10 40	A A
V_{SD}	Forward on voltage	I_{SD} = 10 A V_{GS} = 0			1.4	V
t_{rr}	Reverse recovery time	I_{SD} = 10 A V_{GS} = 0 di/dt = 25 A/μs		100		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

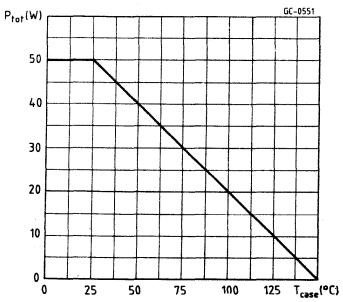
Safe operating areas



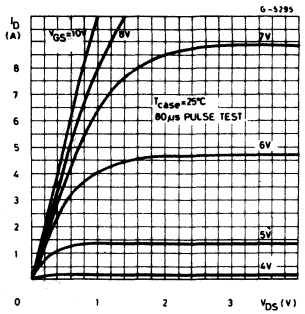
Thermal impedance



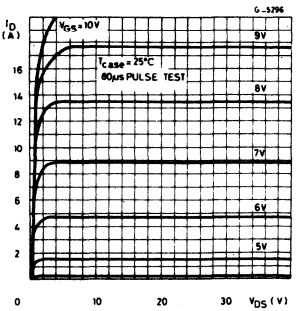
Derating curve



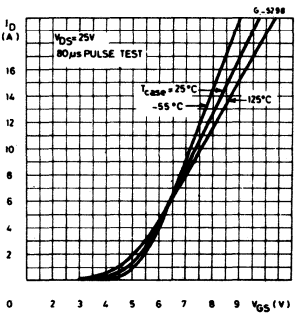
Output characteristics



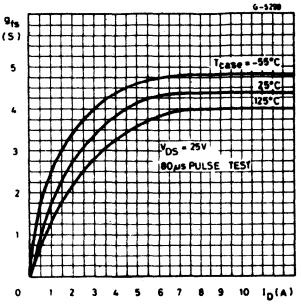
Output characteristics



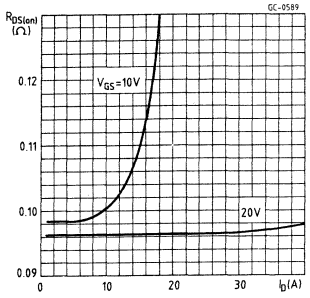
Transfer characteristics



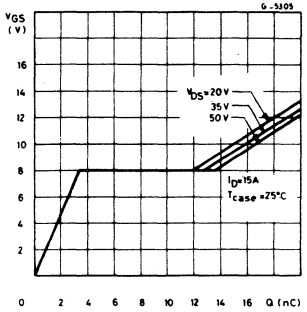
Transconductance



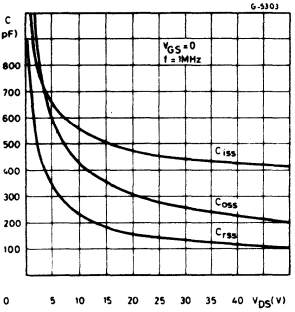
Static drain-source on resistance



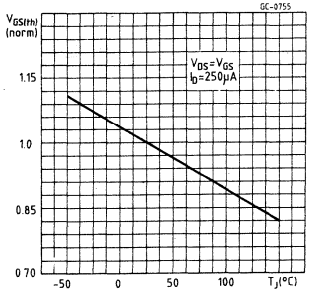
Gate charge vs gate-source voltage



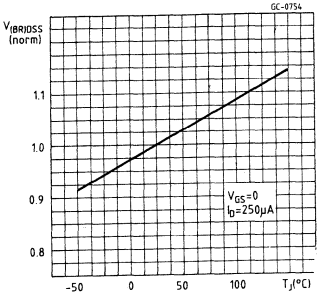
Capacitance variation



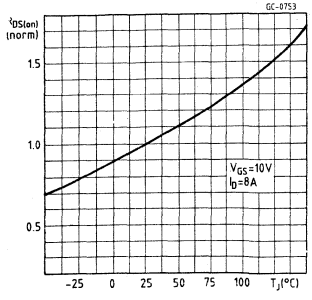
Normalized gate threshold voltage vs temperature



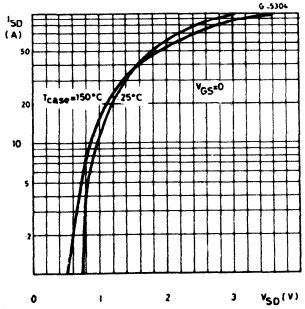
Normalized breakdown voltage vs temperature



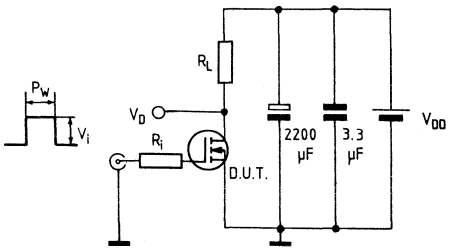
Normalized on resistance vs temperature



Source-drain diode forward characteristics

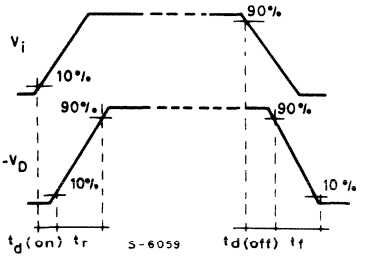


Switching times test circuit for resistive load

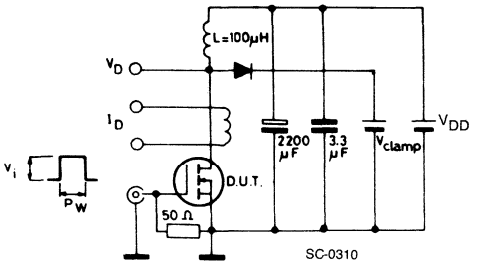


Pulse width ≤ 100 µs
Duty cycle ≤ 2%

Switching time waveforms for resistive load

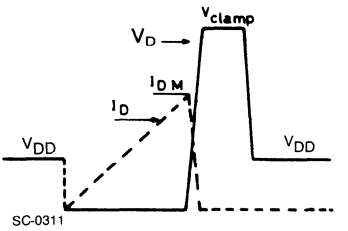


Clamped inductive load test circuit

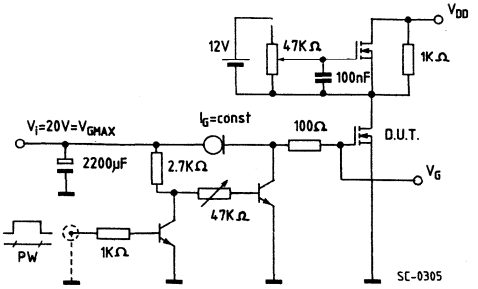


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

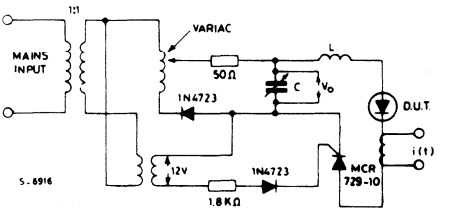


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP361
SGSP362

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

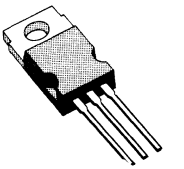
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP361	100 V	0.15 Ω	18 A
SGSP362	80 V	0.1 Ω	22 A

- HIGH SPEED SWITCHING APPLICATIONS
- 80 - 100 VOLTS - FOR UPS APPLICATIONS
- ULTRA FAST SWITCHING
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- EASY DRIVE FOR REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

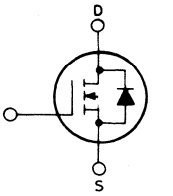
- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include UPS, battery chargers, printer hammer drivers, solenoid drivers and motor control.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP361	SGSP362	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	80	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	80	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	18	22	A
I_D	Drain current (cont.) at $T_c=100°C$	11	14	A
I_{DM} (•)	Drain current (pulsed)	72	88	A
P_{tot}	Total dissipation at $T_c<25°C$	100		W
	Derating factor	0.8		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area
◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.25	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

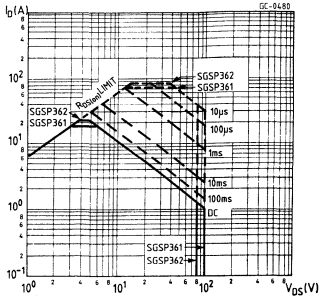
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP361** for **SGSP362**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 9 A for **SGSP361** I_D = 11 A for **SGSP362** V_{GS} = 10 V T_c = 100°C I_D = 9 A for **SGSP361** I_D = 11 A for **SGSP362**			 0.15 0.1 0.3 0.2	 Ω Ω Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **SGSP361** for **SGSP362**	 18 22			 A A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 9 A	4.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	 V_{DS} = 25 V f = 1 MHz V_{GS} = 0		950	1200 480 230	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

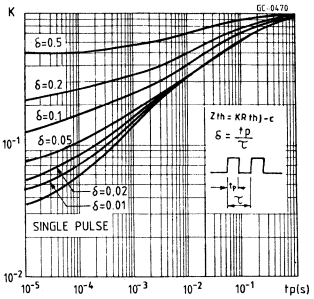
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 50 V I_D = 11 A		20	30	ns
t_r	Rise time	V_i = 10 V R_i = 4.7 Ω		50	65	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		65	85	ns
t_f	Fall time			25	35	ns
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current	for **SGSP361**			18	A
		for **SGSP362**			22	A
I_{SDM} (•)	Source-drain current (pulsed)	for **SGSP361**			72	A
		for **SGSP362**			88	A
V_{SD}	Forward on voltage	V_{GS} = 0				
		I_{SD} = 18 A for **SGSP361**			1.35	V
		I_{SD} = 22 A for **SGSP362**			1.35	V
t_{rr}	Reverse recovery time	I_{SD} = 22 A V_{GS} = 0 di/dt = 25 A/μs		180		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

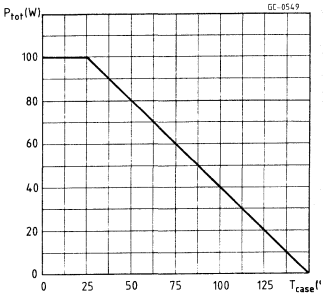
Safe operating areas



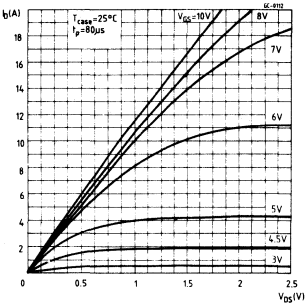
Thermal impedance



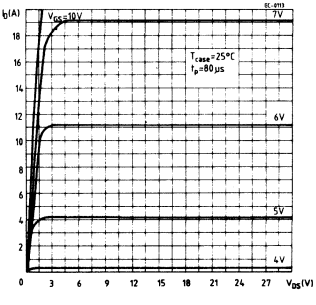
Derating curve



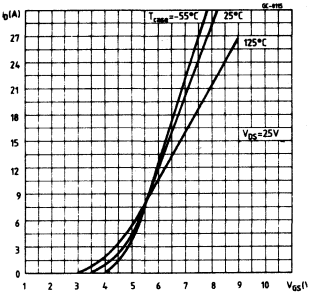
Output characteristics



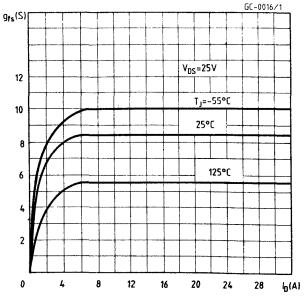
Output characteristics



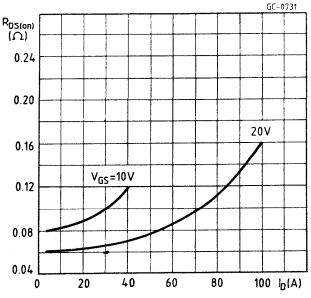
Transfer characteristics



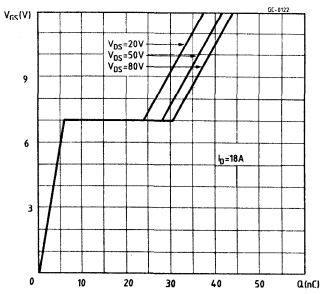
Transconductance



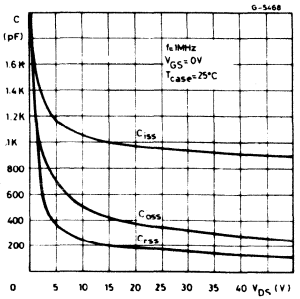
Static drain-source on resistance



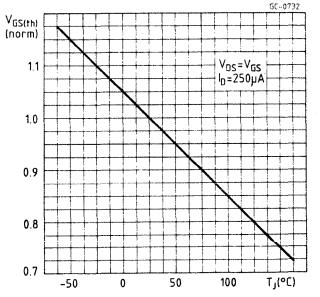
Gate charge vs gate-source voltage



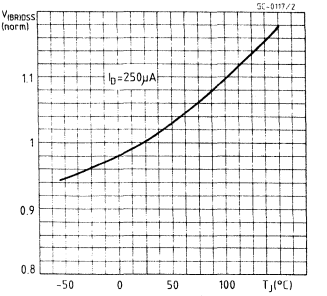
Capacitance variation



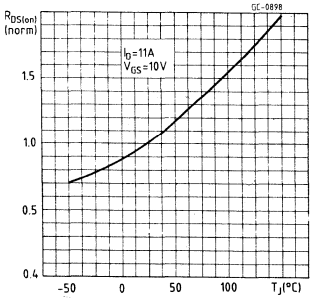
Normalized gate threshold voltage vs temperature



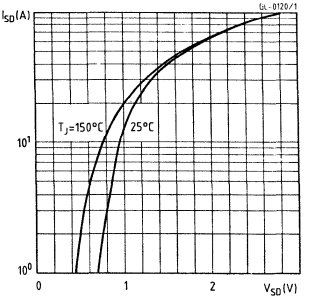
Normalized breakdown voltage vs temperature



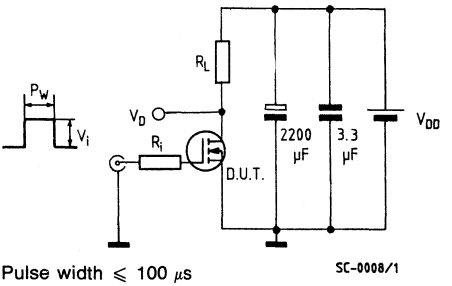
Normalized on resistance vs temperature



Source-drain diode forward characteristics

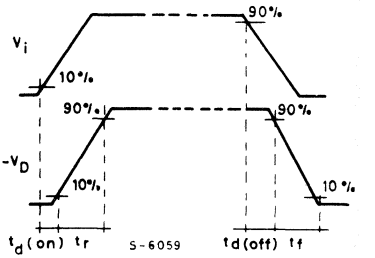


Switching times test circuit for resistive load

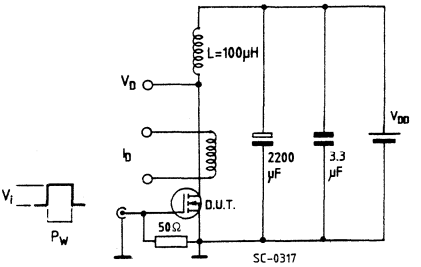


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

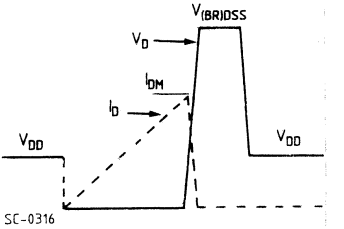


Unclamped inductive load test circuit

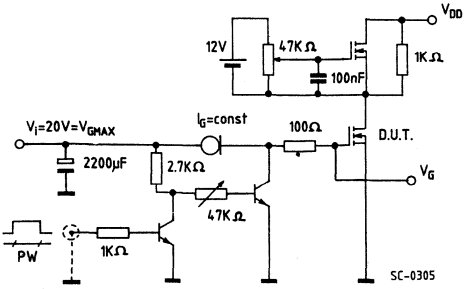


I_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms

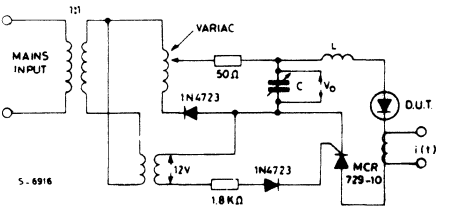


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP461
SGSP462

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

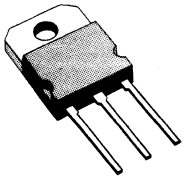
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP461	100 V	0.15 Ω	20 A
SGSP462	80 V	0.1 Ω	25 A

- HIGH SPEED SWITCHING APPLICATIONS
- 80 - 100 VOLTS - FOR UPS APPLICATIONS
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

J - channel enhancement mode POWER MOS field ffect transistors. Easy drive and very fast switching mes make these POWER MOS transistors ideal or high speed switching applications. Typical ap- lications include UPS, battery chargers, printer ammer drivers, solenoid drivers and motor control.



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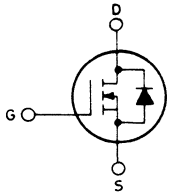
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP461	SGSP462	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	80	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	80	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	20	25	A
I_D	Drain current (cont.) at $T_c=100°C$	13	16	A
I_{DM} (•)	Drain current (pulsed)	80	100	A
P_{tot}	Total dissipation at $T_c<25°C$	125		W
	Derating factor	1		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

•) Pulse width limited by safe operating area
' Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

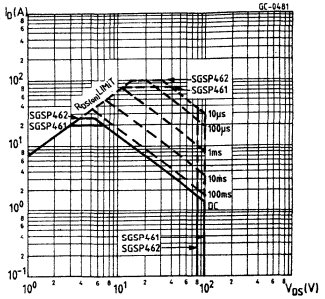
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP461** for **SGSP462**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 10 A for **SGSP461** I_D = 12.5 A for **SGSP462** V_{GS} = 10 V T_c = 100°C I_D = 10 A for **SGSP461** I_D = 12.5 A for **SGSP462**			 0.15 0.1 0.3 0.2	 Ω Ω Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **SGSP461** for **SGSP462**	 20 25			 A A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 12.5 A	4.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		950	1200 480 230	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

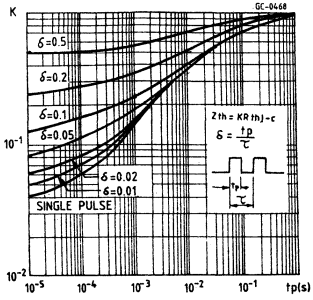
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 50 V I_D = 12.5 A		20	30	ns
t_r	Rise time	V_i = 10 V R_i = 4.7 Ω		60	80	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		65	85	ns
t_f	Fall time			25	35	ns
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current	for **SGSP461**			20	A
		for **SGSP462**			25	A
I_{SDM} (*)	Source-drain current (pulsed)	for **SGSP461**			80	A
		for **SGSP462**			100	A
V_{SD}	Forward on voltage	V_{GS} = 0				
		I_{SD} = 20 A for **SGSP461**			1.35	V
		I_{SD} = 25 A for **SGSP462**			1.35	V
t_{rr}	Reverse recovery time	I_{SD} = 25 A V_{GS} = 0 di/dt = 25 A/μs		190		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(*) Pulse width limited by safe operating area

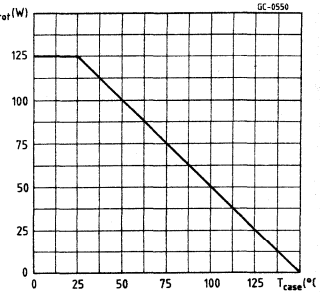
Safe operating areas



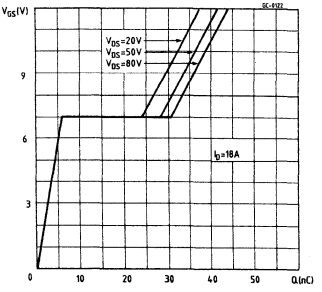
Thermal impedance



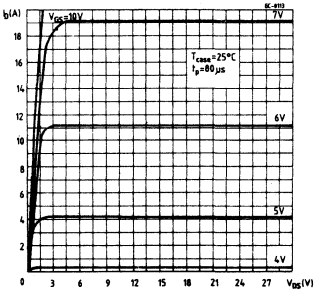
Derating curve



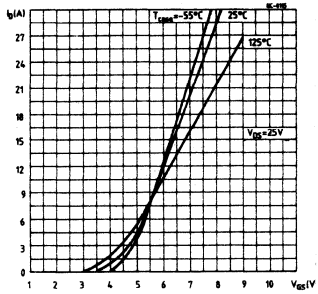
Output characteristics



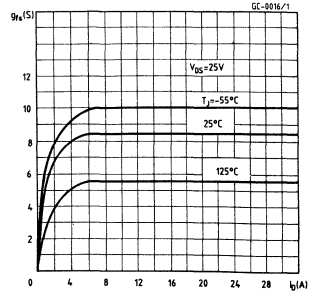
Output characteristics



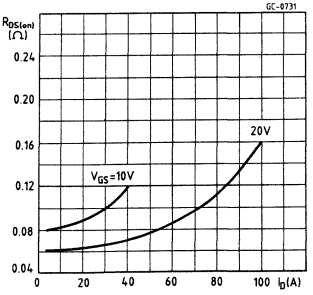
Transfer characteristics



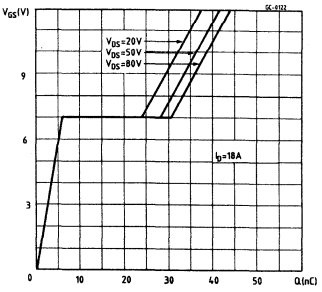
Transconductance



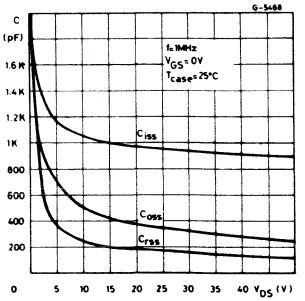
Static drain-source on resistance



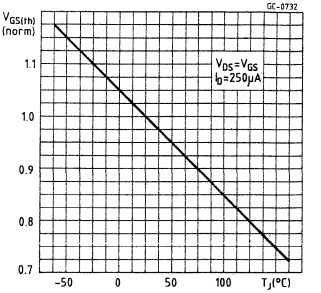
Gate charge vs gate-source voltage



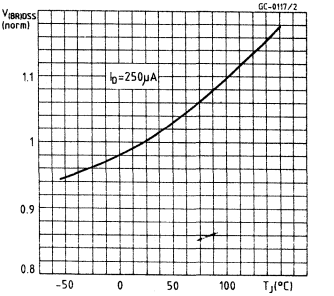
Capacitance variation



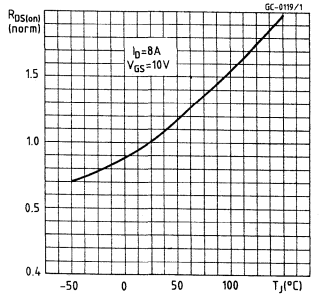
Normalized gate threshold voltage vs temperature



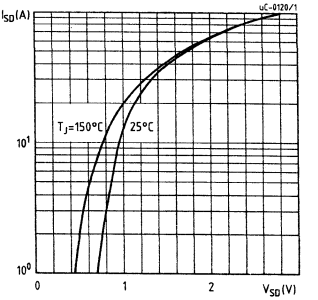
Normalized breakdown voltage vs temperature



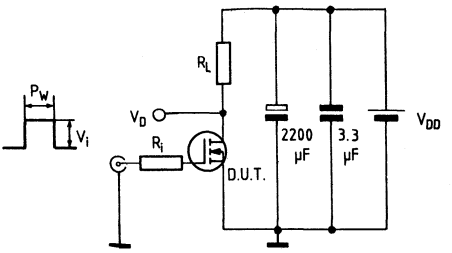
Normalized on resistance vs temperature



Source-drain diode forward characteristics

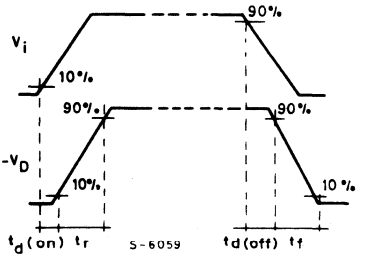


Switching times test circuit for resistive load

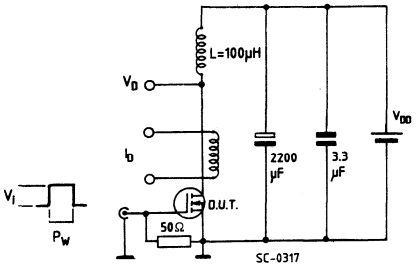


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

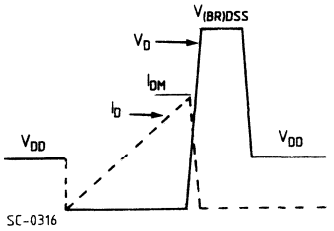


Unclamped inductive load test circuit

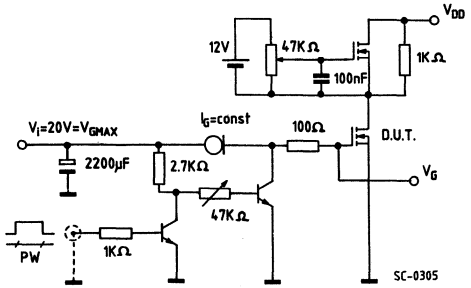


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms

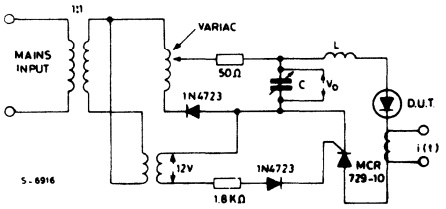


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP491
SGSP492

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

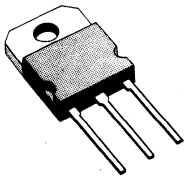
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP491	60 V	0.033 Ω	40 A
SGSP492	50 V	0.033 Ω	40 A

- HIGH SPEED SWITCHING APPLICATIONS
- 50 - 60 VOLTS FOR INVERTER AND UPS
- HIGH CURRENT - $V_{DS\ (on)} \leq 1V$ at 20A
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- EASY DRIVE - REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

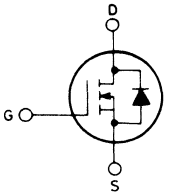
- DC/DC CONVERTERS
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications such as DC/DC converters, UPS, inverters, battery changers and solar power converters.



TO-218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP491	SGSP492	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	60	50	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c = 25°C$	40		A
I_D	Drain current (cont.) at $T_c = 100°C$	25		A
I_{DM} (•)	Drain current (pulsed)	160		A
P_{tot}	Total dissipation at $T_c < 25°C$	150		W
	Derating factor	1.2		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area
◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

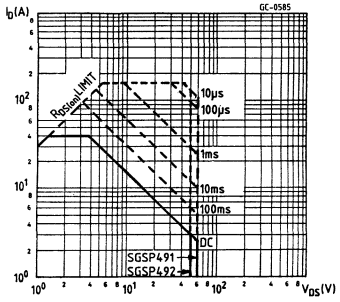
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP491** for **SGSP492**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 20 A V_{GS} = 10 V I_D = 20 A T_c = 100°C			33 66	mΩ mΩ
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C	40			A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 20 A	10			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1900	2800 1500 850	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 20 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		35 110 90 55	45 145 120 70	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

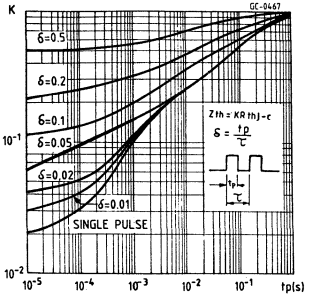
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (*) Source-drain current (pulsed)				40 160	A A
V_{SD} Forward on voltage	I_{SD} = 40 A V_{GS} = 0			1.4	V
t_{rr} Reverse recovery time	I_{SD} = 40 A V_{GS} = 0 di/dt = 25 A/μs		140		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(*) Pulse width limited by safe operating area

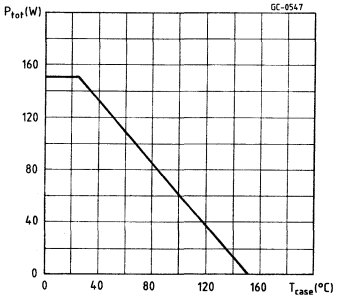
Safe operating areas



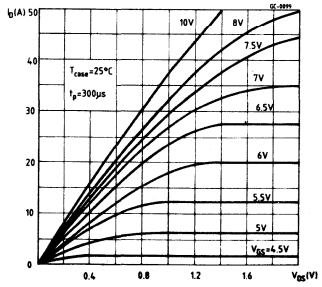
Thermal impedance



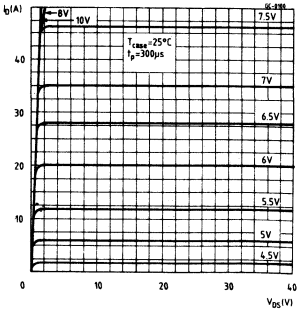
Derating curve



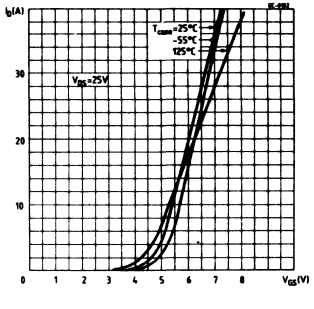
Output characteristics



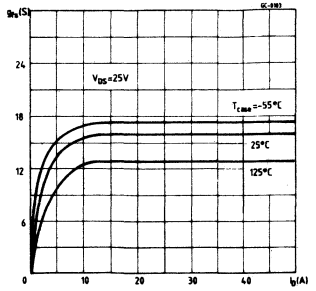
Output characteristics



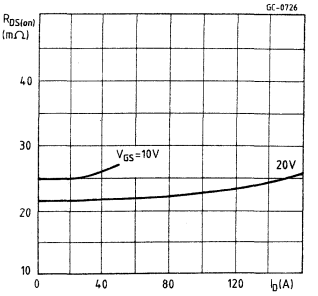
Transfer characteristics



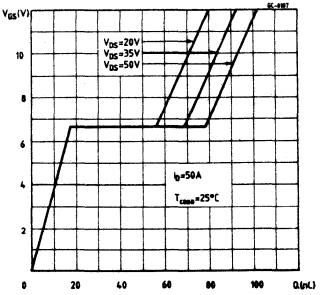
Transconductance



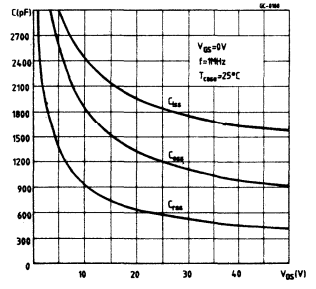
Static drain-source on resistance



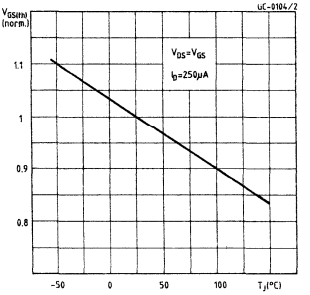
Gate charge vs gate-source voltage



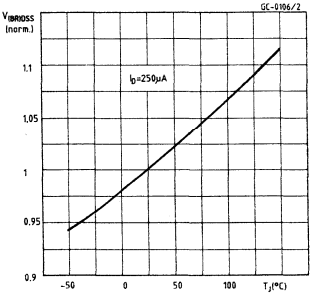
Capacitance variation



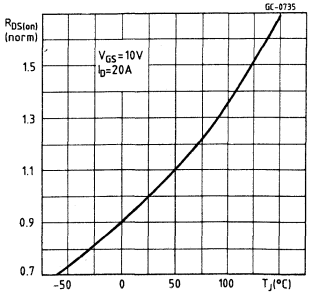
Normalized gate threshold voltage vs temperature



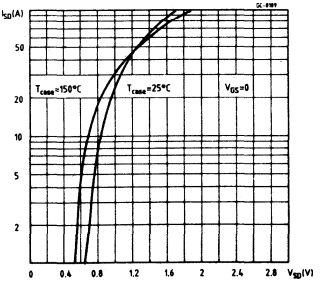
Normalized breakdown voltage vs temperature



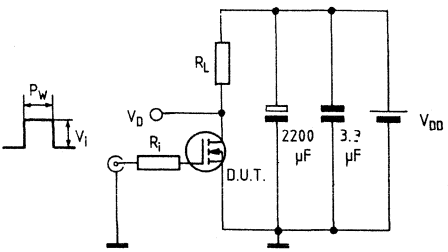
Normalized on resistance vs temperature



Source-drain diode forward characteristics

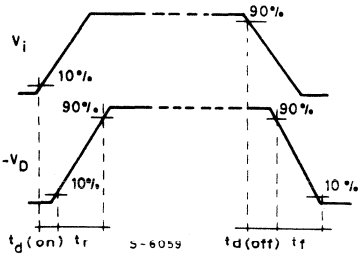


Switching times test circuit for resistive load

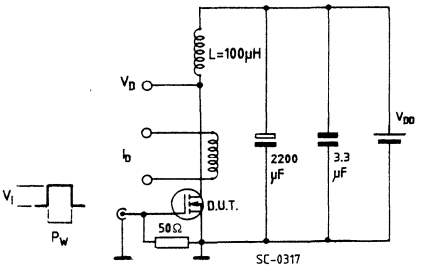


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

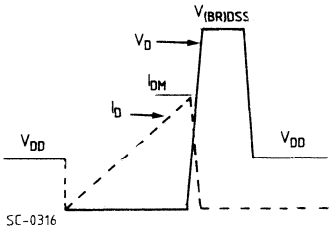


Unclamped inductive load test circuit

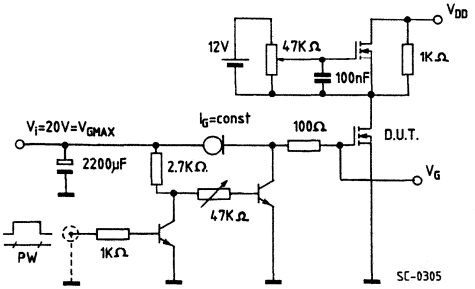


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms

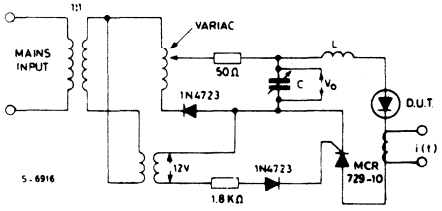


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement Jedec test circuit



SGS-THOMSON MICROELECTRONICS

STLT20/FI
STLT19/FI

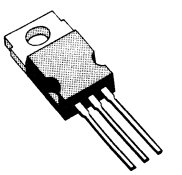
N - CHANNEL ENHANCEMENT MODE LOW THRESHOLD POWER MOS TRANSISTORS

PRELIMINARY DATA

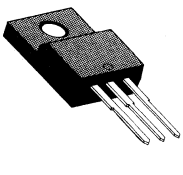
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STLT20	60 V	0.15 Ω	15 A
STLT20FI	60 V	0.15 Ω	10 A
STLT19	50 V	0.15 Ω	15 A
STLT19FI	50 V	0.15 Ω	10 A

- LOGIC LEVEL (+5V) CMOS/TTL COMPATIBLE INPUT
- HIGH INPUT IMPEDANCE
- ULTRA FAST SWITCHING

N - channel enhancement mode POWER MOS field effect transistors. The low input voltage - logic level - and easy drive make these devices ideal for automotive and industrial applications. Typical uses are in relay and actuator driving in the automotive enviroment.

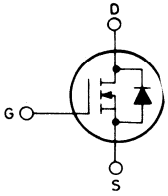


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 ISOWATT220	STLT20 STLT20FI	STLT19 STLT19FI	
V_{DS}	Drain-source voltage ($V_{GS}=0$)		60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)		60	50	V
V_{GS}	Gate-source voltage		±15		V
			TO-220	**ISOWATT220**	
I_D	Drain current (cont.) at $T_c=25°C$		15	10	A
I_D	Drain current (cont.) at $T_c=100°C$		9.5	6.3	A
I_{DM}(•)	Drain current (pulsed)		40	40	A
P_{tot}	Total dissipation at $T_c<25°C$		75	30	W
	Derating factor		0.6	0.24	W/°C
T_{stg}	Storage temperature		−65 to 150		°C
T_j	Max. operating junction temperature		150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1.67	4.16	°C/W
T_l	Maximum lead temperature for soldering purpose	max	275		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

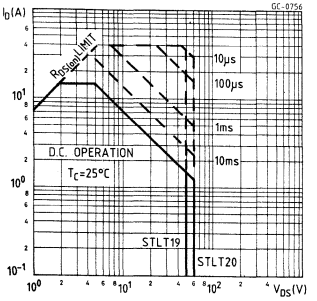
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA for **STLT20/FI** for **STLT19/FI**	V_{GS} = 0	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8	T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±15 V				±100	nA
ON **							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 250 μA	1		2.5	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 5 V	I_D = 7.5 A			0.15	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 15 V	I_D = 7.5 A	5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		480 170 40		pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V V_i = 5 V	I_D = 7.5 A R_i = 50 Ω		10 70 35 40		ns ns ns ns
Q_g	Total Gate Charge	V_{DD} = 48 V V_{GS} = 5 V	I_D = 15 A		8	13	nC

ELECTRICAL CHARACTERISTICS (Continued)

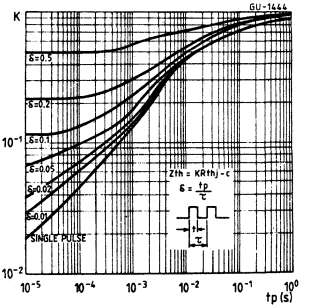
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD}	Source-drain current					15	A
I_{SDM}(•)	Source-drain current (pulsed)					60	A
V_{SD}**	Forward on voltage	I_{SD} = 15 A	V_{GS} = 0			1.25	V
t_{rr}	Reverse recovery time				80		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 15 A	di/dt = 100A/μs		0.15		μC

** Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 2%
(•) Pulse width limited by safe operating area

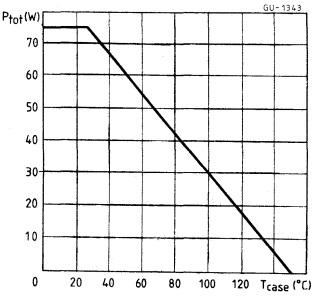
Safe operating areas (standard package)



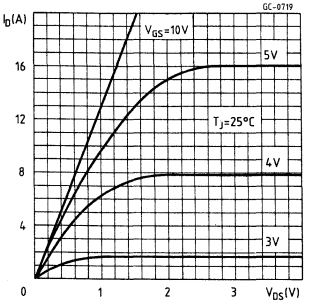
Thermal impedance (standard package)



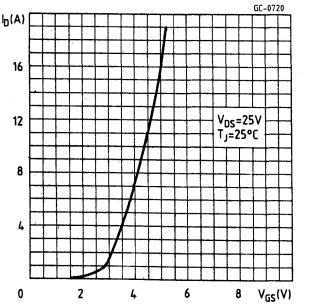
Derating curve (standard package)



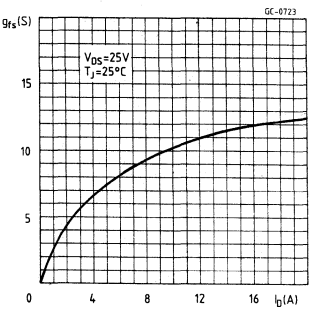
Output characteristics



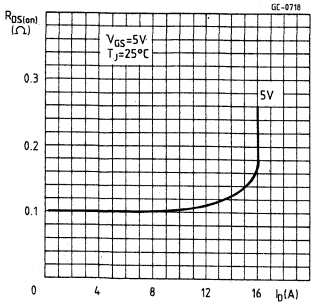
Transfer characteristics



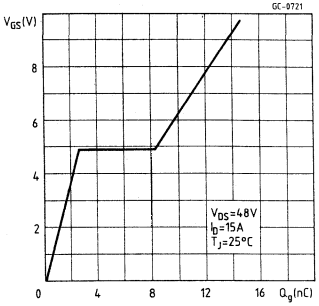
Transconductance



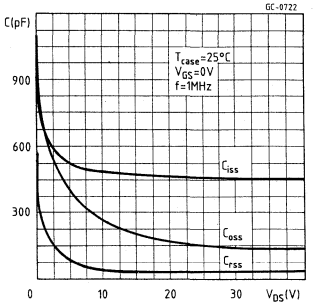
Static drain-source on resistance



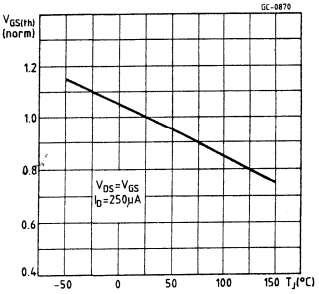
Gate charge vs gate-source voltage



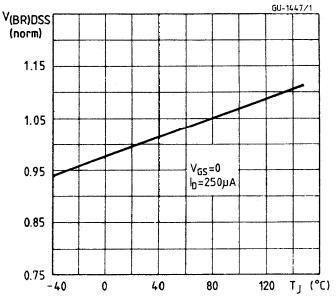
Capacitance variation



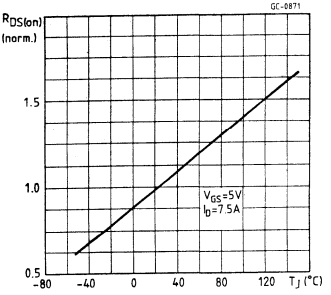
Normalized gate threshold voltage vs temperature



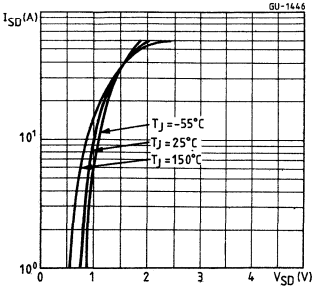
Normalized breakdown voltage vs temperature



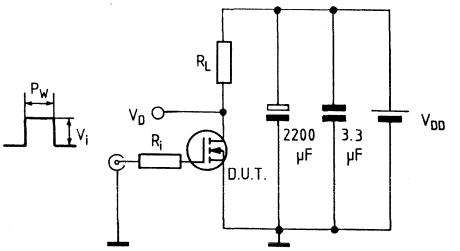
Normalized on resistance vs temperature



Source-drain diode forward characteristics



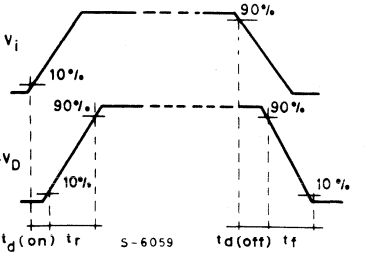
Switching times test circuit for resistive load



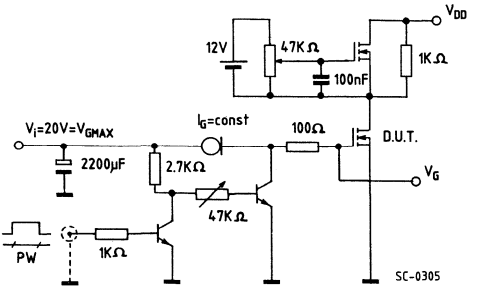
Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

SC-0008/1

Switching time waveforms for resistive load

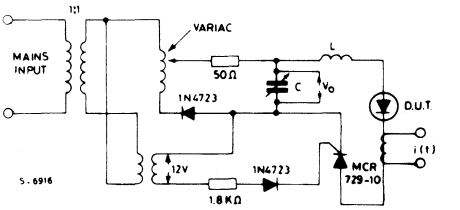


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

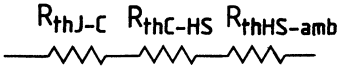
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

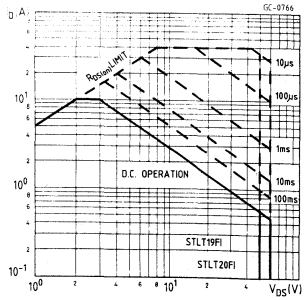
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

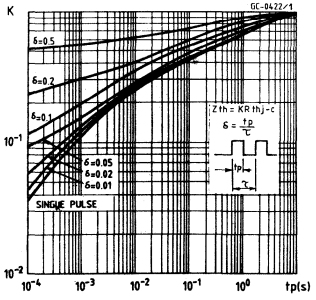


ISOWATT DATA

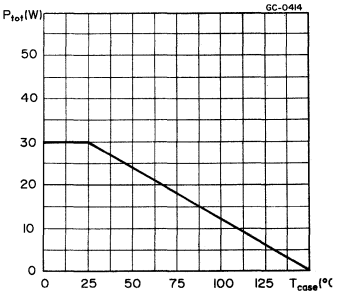
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

STLT30/FI
STLT29/FI

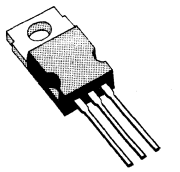
N - CHANNEL ENHANCEMENT MODE LOW THRESHOLD POWER MOS TRANSISTORS

ADVANCE DATA

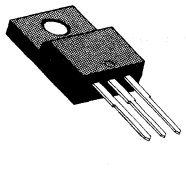
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STLT30	60 V	0.08 Ω	25 A
STLT30/FI	60 V	0.08 Ω	15 A
STLT29	50 V	0.08 Ω	25 A
STLT29/FI	50 V	0.08 Ω	15 A

- LOGICAL LEVEL (+5V) CMOS/TTL COMPATIBLE INPUT
- HIGH INPUT IMPEDANCE
- ULTRA FAST SWITCHING

N - channel enhancement mode POWER MOS field effect transistors. The low input voltage - logic level - and easy drive make these devices ideal for automotive and industrial applications. Typical uses are in relay and actuator driving in the automotive enviroment.

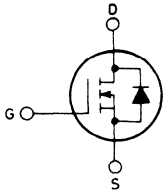


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 ISOWATT220	STLT30 STLT30FI	STLT29 STLT29FI	
V_{DS}	Drain-source voltage ($V_{GS}=0$)		60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)		60	50	V
V_{GS}	Gate-source voltage		±15		V
			TO-220	**ISOWATT220**	
I_D	Drain current (cont.) at $T_c=25°C$		25	15	A
I_D	Drain current (cont.) at $T_c=100°C$		15.7	9.5	A
I_{DM}	Drain current (pulsed)		80	80	A
P_{tot}	Total dissipation at $T_c<25°C$		100	35	W
	Derating factor		0.8	0.28	W/°C
T_{stg}	Storage temperature		−65 to 150		°C
T_j	Max. operating junction temperature		150		°C

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.25	3.75	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	75		°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA for **STLT30/FI** for **STLT29/FI**	V_{GS} = 0	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8	 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±15 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 250 μA	1		2.5	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 5V	I_D = 12.5 A			0.08	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 15 V	I_D = 12.5 A	9			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		930	1200 600 130	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V R_{GS} = 50 Ω	I_D = 12.5 A V_{GS} = 5 V		25 210 55 75		ns ns ns ns
Q_g	Total Gate Charge	V_{DS} = 25 V V_{GS} = 5 V	I_D = 25 A		19		nC

ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)					25 80	A A
V_{SD}	Forward on voltage	I_{SD} = 25 A	V_{GS} = 0		1.5		V
t_{rr}	Reverse recovery time				300		ns
Q_{rr}	Reverse recovery charge	I_{SD} = 25 A	di/dt = 100A/μs		0.3		μC

SGS-THOMSON MICROELECTRONICS

STVHD90

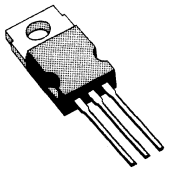
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STVHD90	50 V	0.023 Ω	52 A

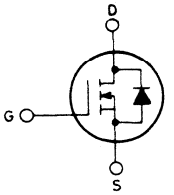
- VERY HIGH DENSITY
- VERY LOW $R_{DS\ (on)}$
- VERY HIGH CURRENT
- HIGH TRANSCONDUCTANCE/C_{rss} RATIO
- LOW DRIVE ENERGY
- ULTRA FAST SWITCHING

N - channel enhancement mode very high density POWER MOS transistors. Easy drive and low on voltage make this device ideal for automotive and industrial applications requiring high current and low on-losses. Typical uses are actuators lamp and motor control in the automotive and industrial enviroments. It can also be used in DC/DC converters.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	52	A
I_D	Drain current (cont.) at $T_c=125°C$	32	A
I_{DM} (•)	Drain current (pulsed)	200	A
I_{DLM}	Drain inductive current clamped	200	A
P_{tot}	Total dissipation at $T_c<25°C$	125	W
	Derating factor	1	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

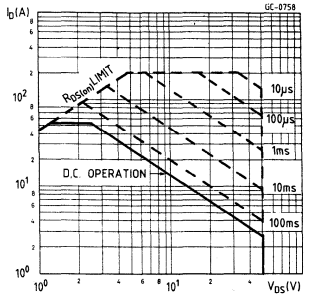
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8	 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				100	nA
ON (*)							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 30 A			23	mΩ
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 30 A		30		mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		2500 850 120	3000 1000 150	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 40 V V_i = 50 V (see test circuit)	I_D = 25 A R_i = 50 Ω			40 100 250 170	ns ns ns ns
Q_g	Total Gate Charge	V_{DD} = 25 V V_{GS} = 10 V	I_D = 30 A		56		nC

ELECTRICAL CHARACTERISTICS (Continued)

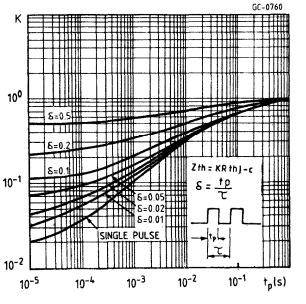
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				52 200	A A
V_{SD} Forward on voltage	I_{SD} = 52 A V_{GS} = 0			1.5	V
t_{rr} Reverse recovery time Q_{rr} Reverse recovery charge	I_{SD} = 52 A V_{GS} = 0 di/dt = 100 A/μs		70 110		ns μC

(•) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%

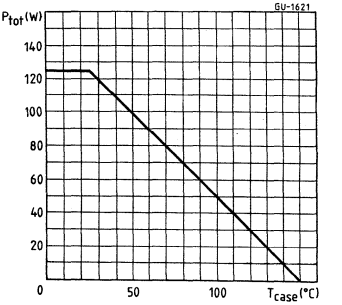
Safe operating areas



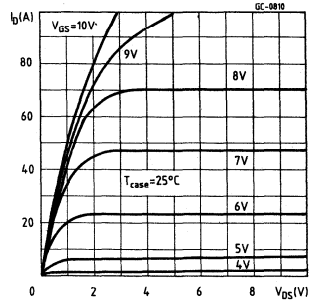
Thermal impedance



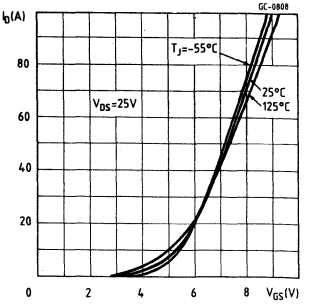
Derating curve



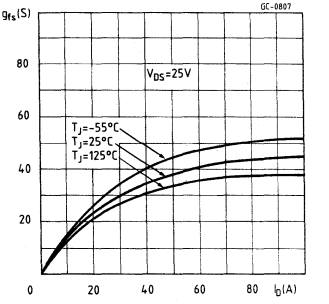
Output characteristics



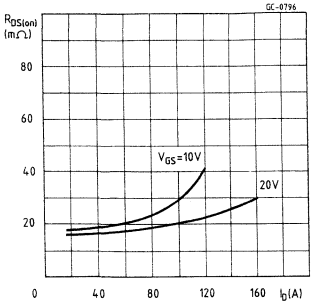
Transfer characteristics



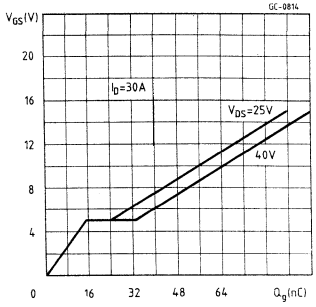
Transconductance



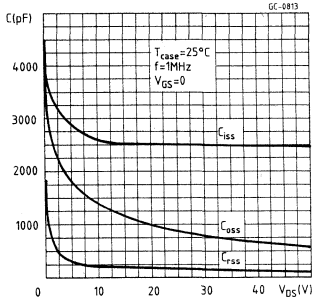
Static drain-source on resistance



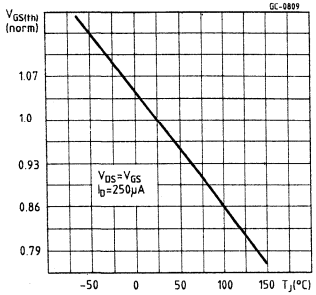
Gate charge vs gate-source voltage



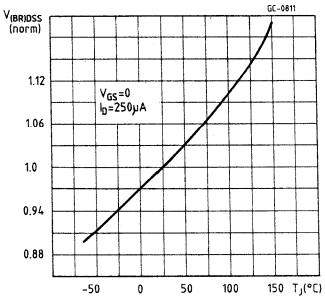
Capacitance variation



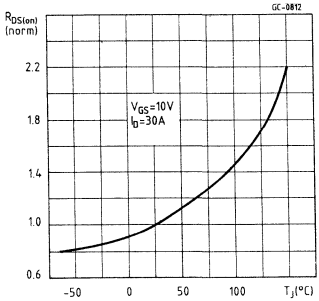
Normalized gate threshold voltage vs temperature



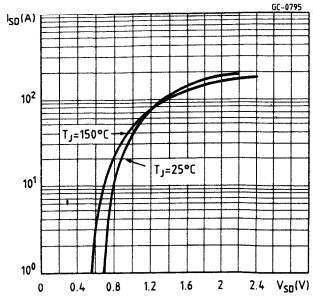
Normalized breakdown voltage vs temperature



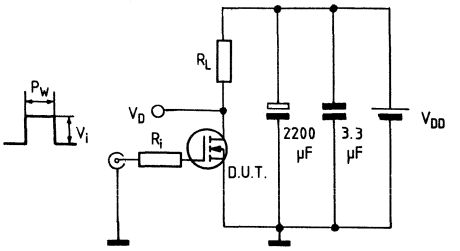
Normalized on resistance vs temperature



Static drain diode forward characteristics

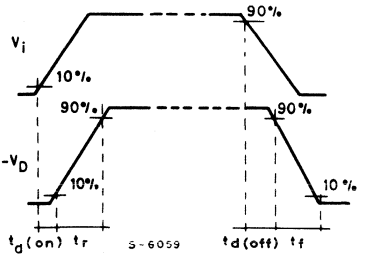


Switching times test circuit for resistive load

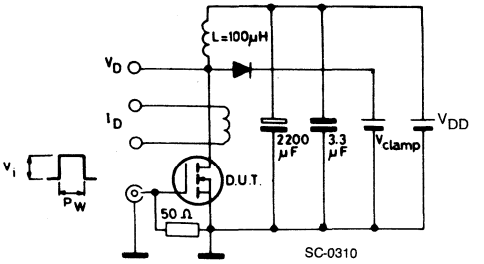


Pulse width ≤ 100 µs
Duty cycle ≤ 2%

Switching time waveforms for resistive load

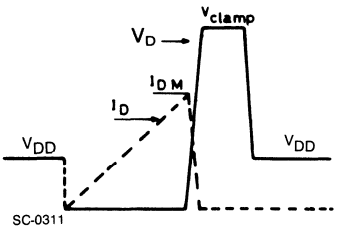


Clamped inductive load test circuit

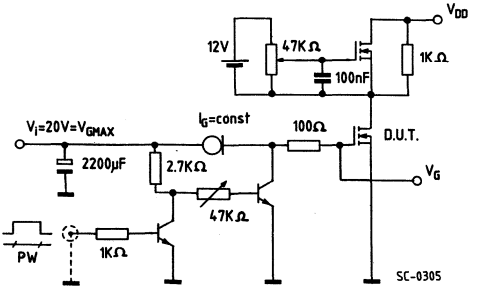


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

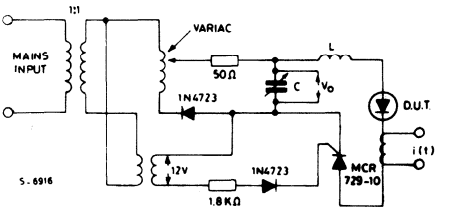


Gate charge test circuit



PW adjusted to obtain required V_G

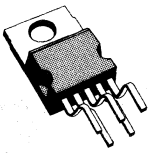
Body-drain diode t_{rr} measurement
Jedec test circuit



HIGH SIDE SMART SOLID STATE RELAY

ADVANCE DATA

- DRAIN CURRENT (continous) : 25A AT T_C = 25°C
- INRUSH CURRENT LIMITATION
- TTL/CMOS COMPATIBLE INPUT
- SHORT CIRCUIT PROTECTION
- LOAD OVER–VOLTAGE PROTECTION
- THERMAL SHUTDOWN
- OPEN DRAIN DIAGNOSTIC OUTPUT
- VERY LOW STAND–BY POWER DISSIPATION
- DIGITAL DIAGNOSTIC FILTERING



PENTAWATT

DESCRIPTION

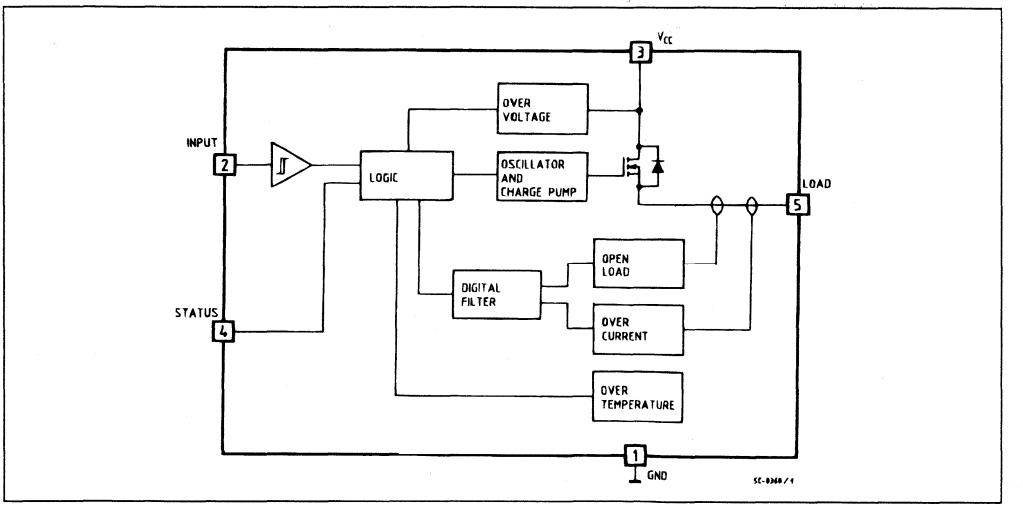
The VM200 is a Monolithic device made using SGS-THOMSON Microelectronics Vertical Intelligent Power Technology, intended for driving resistive or inductive loads, with one side connected to ground.

Built-in thermal shut-down protects the chip from over temperature. The power stage uses a low dissipation mosfet current sensing technique which provides short circuit and open load protection.

The input control is TTL/CMOS compatible. The diagnostic output provides an indication of open load and short circuit conditions, and thermal and overvoltage shut-down status.

Type	V_{DSS}	I_D*	$R_{DS\ (ON)}$
VM200	60V	25A	0.05Ω

TEST AND APPLICATION CIRCUIT

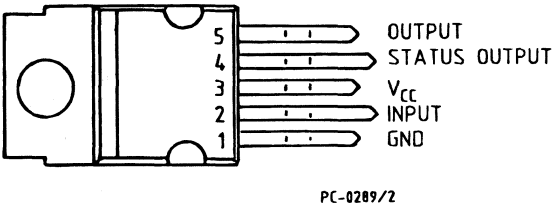


* See note 1.

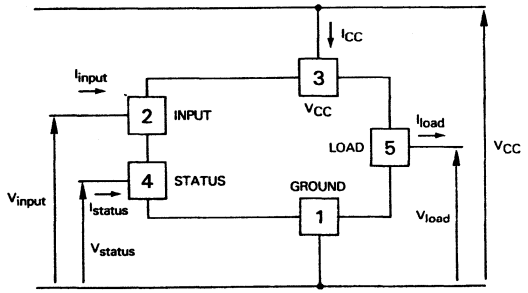
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain–source Breakdown Voltage	60	V
I_D	Drain Current (cont.)	25	A
I_R	Reverse Output Current	– 25	A
V_{IN}	Input Voltage	60	V
V_S	Status Voltage	60	V
I_D	Diagnostic Current (sink)	2	mA
V_{ESD}	Electrostatic Discharge (1.5KΩ, 100pF)	2000	V
P_{tot}	Power Dissipation	Internally Limited	
T_j	Junction Operating Temperature	– 40 to 150	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

CONNECTION DIAGRAM



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

$R_{th\ j-case}$	Thermal Resistance Junction–case	Max.	1.67	°C/W
$R_{th\ j-amb}$	Thermal Resistance Junction–ambient	Max.	0.60	°C/W

ELECTRICAL CHARACTERISTICS : (V_{CC} = 13V; T_j = 25°C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage		6		30	V
R_{on}	On State Resistance	I_D = 12A T_j = 25°C			0.05	Ω
I_S	Supply Current	Off State			100	µA

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn–on Delay Time of Output Current	I_D = 12A Resistive Load Input Rise Time < 0.1µs		16		µs
t_r	Rise Time of Output Current	I_D = 12A Resistive Load Input Rise Time < 0.1µs		130		µs
$t_{d\ (off)}$	Turn–off Delay Time of Output Current	I_D = 12A Resistive Load Input Fall Time < 0.1µs		16		µs
t_f	Fall Time of Output Current	I_D = 12A Resistive Load Input Fall Time < 0.1µs		6		µs
$(di/dt)_{on}$	Turn–on Current Slope	I_D = 12A $I_D = I_{SC}$		0.1 2		A/µs
$(di/dt)_{off}$	Turn–off Current Slope	I_D = 12A $I_D = I_{SC}$		1.5		3

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2			V
$V_{I\ (hyst)}$	Input Hysteresis Voltage			0.2		V
I_{IN}	Input Current	V_I = 5V		10		µA

ELECTRICAL CHARACTERISTICS (continued)

PROTECTIONS AND DIAGNOSTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DIAGL}	Diagnostic Voltage Output Low	I_{sink} = 1.6mA			0.8	V
I_{DIAGH}	Diagnostic Current Output High	V_{CC} = 5V			1	µA
V_{OSD}	Over Voltage Shut Down		30		40	V
I_{SC}	Short Circuit Current		25			A
I_{OL}	Open Load Current Level				50	mA
$t_{d\ (SC)}$	Short Circuit Delay Turn–off Time	IN TURN ON IN OPERATION	30 1		 1.5	ms
$t_{d\ (OL)}$	Open Load Delay Turn–off Time		1		1.5	ms
T_{TSD}	Thermal Shut Down Temperature		150			°C
$T_{RSD\ (hyst)}$	Thermal Shut Down Hysteresis		10		20	°C

The device has a diagnostic output which indicates open circuit (no load), short circuit, over current and over temperature conditions.

The truth table shows input, diagnostic output voltage level in normal operation and in fault condition.

The output signals are processed by internal logic.

The internally generated short circuit/over current signal is ignored for 33ms at turn-on, the load current is limited at the short circuit value without diagnostic signalling during this period. After this time if a fault is present the device is turned off and the diagnostic signal becomes low.

If, during normal conduction, a fault condition is detected for more than 1ms (see truth table), the device is turned off and the diagnostic output goes low. This allows short load current interruptions caused typically by brush contacts in a D. C. motor.

TRUTH TABLE

	Input	Diagnostic		Output
		Output	Delay (ms)	
Normal Operation	L H	H H		L H
Open Circuit (no load)	L H	H L	1	L H
Short-circuit/ Over-current	L H	H L	33 Turn–on 1 Normal Op.	L L
Over–temperature	L H	H L		L

L = Low Level
H = High Level
Note : 1. Internally limited by overcurrent protection (typical value).

SHORT-CIRCUIT BEHAVIOUR

Figure 1 : Test Circuit.

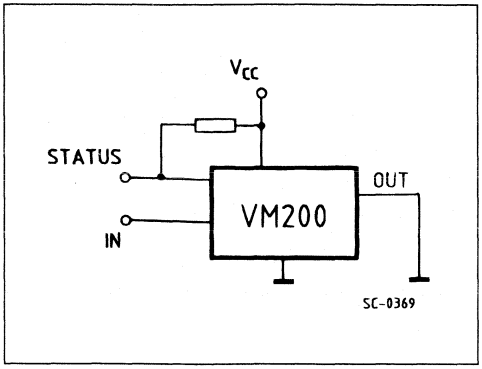
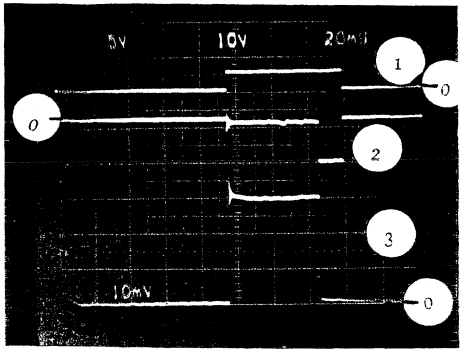


Photo 1 : Waveform.



1 : Input Voltage 5V/div.
2 : Status Voltage 10V/div.
3 : Output Current 10A/div.

SWITCHING A LAMP

Figure 2 : Application Circuit.

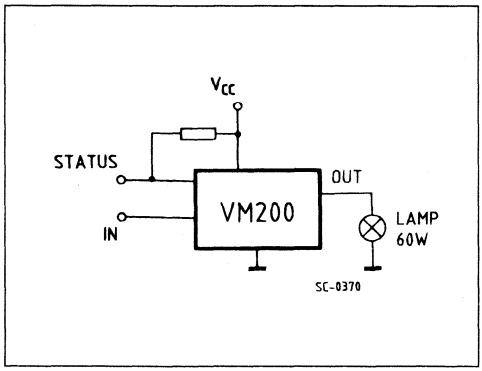
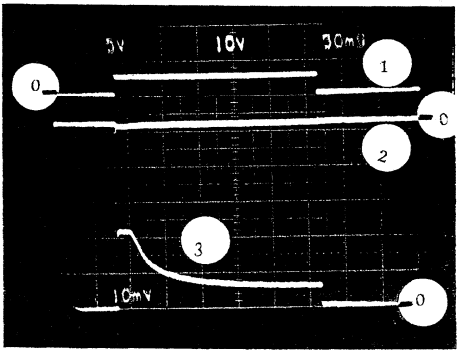


Photo 2 : Waveform.



1 : Input Voltage 5V/div.
2 : Status Voltage 10V/div.
3 : Output Current 10A/div.

SWITCHING A SOLENOID

Figure 3 : Application Circuit.

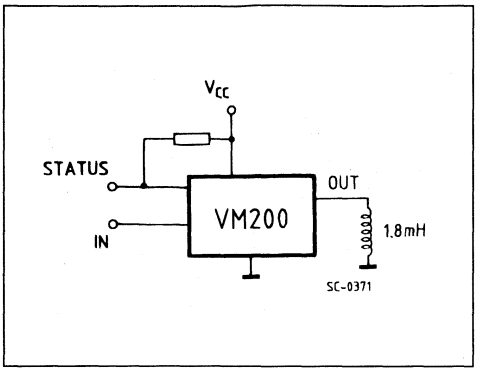
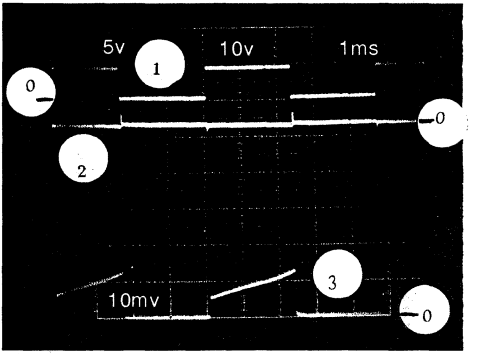


Photo 3 : Waveform.



1 : Input Voltage 5V/div.
2 : Status Voltage 10V/div.
3 : Output Current 10A/div.

OPEN LOAD BEHAVIOUR

Figure 4 : Test Circuit.

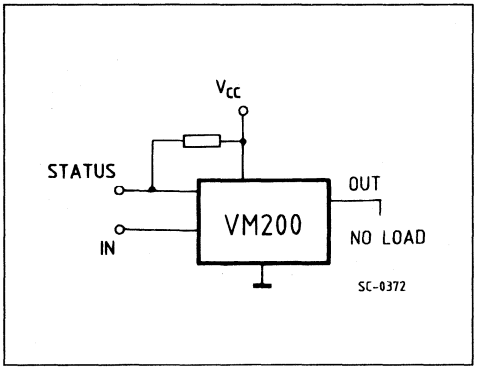
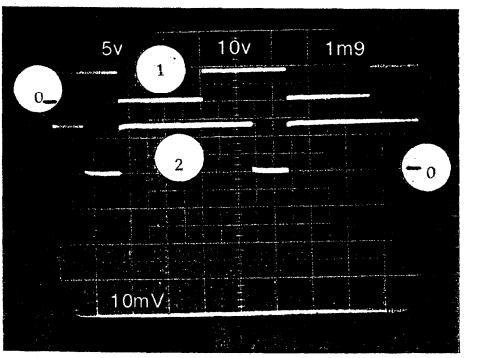
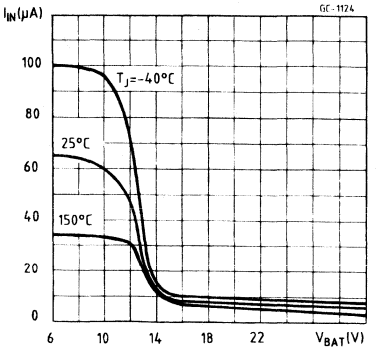


Photo 4 : Waveform.

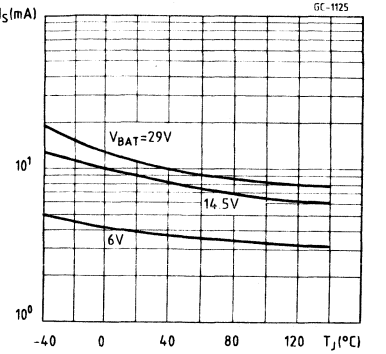


1 : Input Voltage 5V/div.
2 : Status Voltage 10V/div.
3 : Output Current 10A/div.

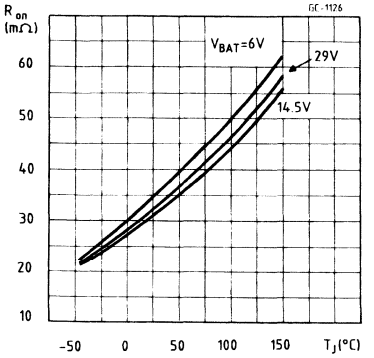
Input Current vs V_{bat}.



Status Current vs Junction Temperature.



On Resistance vs Junction Temperature.



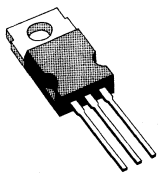
SGS-THOMSON MICROELECTRONICS

BDW93/A/B/C
BDW94/A/B/C

NPN/PNP POWER DARLINGTONS

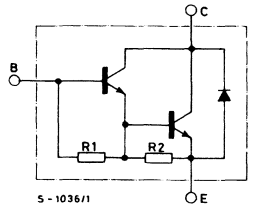
DESCRIPTION

The BDW93, BDW93A, BDW93B and BDW93C are silicon epitaxial-base NPN transistors in monolithic Darlington configuration and are mounted in Jedec TO-220 plastic package. They are intended for use in power linear and switching applications. The complementary PNP types are the BDW94, BDW94A, BDW94B and BDW94C respectively.



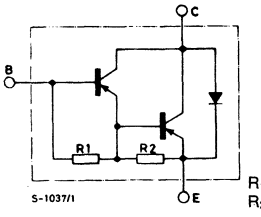
TO-220

INTERNAL SCHEMATIC DIAGRAM



NPN

R_1 Typ. 10 kΩ
R_2 Typ. 150 Ω.



PNP

R_1 Typ. 10 kΩ
R_2 Typ. 150 Ω.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	NPN PNP*	Value				Unit
			BDW93 BDW94	BDW93A BDW94A	BDW93B BDW94B	BDW93C BDW94C	
V_{CBO}	Collector-base Voltage (I_E = 0)		45	60	80	100	V
V_{CEO}	Collector-emitter Voltage (I_B = 0)		45	60	80	100	V
I_C	Collector Current		12				A
I_{CM}	Collector Peak Current		15				A
I_B	Base Current		0.2				A
P_{tot}	Total Power Dissipation at $T_{case} \leq 25$ °C		80				W
T_{stg}	Storage Temperature		– 65 to 150				°C
T_j	Junction Temperature		150				°C

* For PNP types voltage and current values are negative.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.56	°C/W

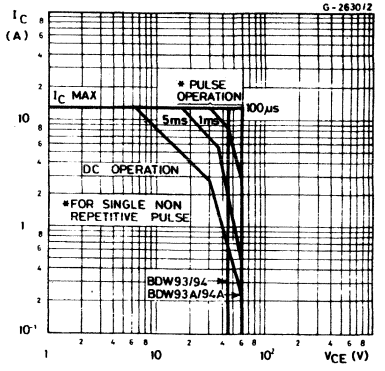
ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cutoff Current (I_E = 0)	for **BDW93/94** V_{CB} = 45 V			100	μA
		for **BDW93A/94A** V_{CB} = 60 V			100	μA
		for **BDW93B/94B** V_{CB} = 80 V			100	μA
		for **BDW93C/94C** V_{CB} = 100 V			100	μA
		T_{case} = 150 °C				
		for **BDW93/94** V_{CB} = 45 V			5	mA
		for **BDW93A/94A** V_{CB} = 60 V			5	mA
		for **BDW93B/94B** V_{CB} = 80 V			5	mA
		for **BDW93C/94C** V_{CB} = 100 V			5	mA
I_{CEO}	Collector Cutoff Current (I_B = 0)	for **BDW93/94** V_{CE} = 40 V			1	mA
		for **BDW93A/94A** V_{CE} = 60 V			1	mA
		for **BDW93B/94B** V_{CE} = 80 V			1	mA
		for **BDW93C/94C** V_{CE} = 80 V			1	mA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{EB} = 5 V			2	mA
$V_{CEO(sus)}$*	Collector-emitter Sustaining Voltage (I_B = 0)	I_C = 100 mA for **BDW93/94**	45			V
		for **BDW93A/94A**	60			V
		for **BDW93B/94B**	80			V
		for **BDW93C/94C**	100			V
$V_{CE(sat)}$*	Collector-emitter Saturation Voltage	I_C = 5 A I_B = 20 mA			2	V
		I_C = 10 A I_B = 100 mA			3	V
$V_{BE(sat)}$*	Base-emitter Saturation Voltage	I_C = 5 A I_B = 20 mA			2.5	V
		I_C = 10 A I_B = 100 mA			4	V
h_{FE}*	DC Current Gain	I_C = 3 A V_{CE} = 3 V	1000			
		I_C = 5 A V_{CE} = 3 V	750		20000	
		I_C = 10 A V_{CE} = 3 V	100			
V_F*	Parallel-diode Forward Voltage	I_F = 5 A		1.3	2	V
		I_F = 10 A		1.8	4	V
h_{fe}	Small Signal Current Gain	I_C = 1 A V_{CE} = 10 V f = 1 MHz	20			

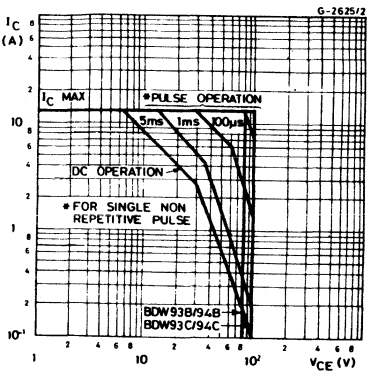
* Pulsed : pulse duration = 300 μs, duty cycle = 1.5 %.

For PNP types voltage and current values are negative.

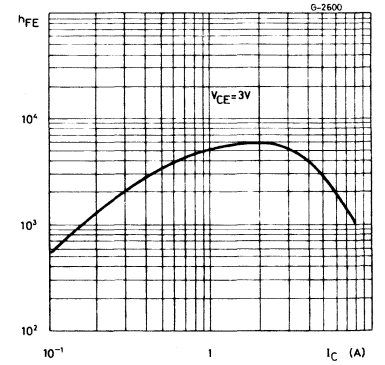
Safe Operating Areas (for **BDW93**, **BDW93A**, **BDW94**, **BDW94A**).



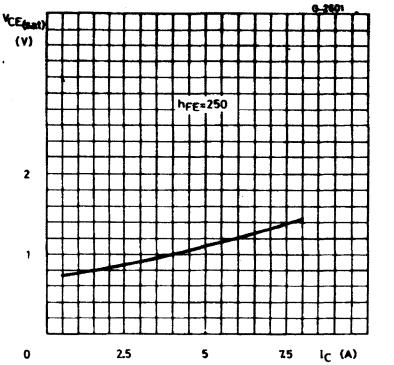
Safe Operating Areas (for **BDW93B**, **BDW93C**, **BDW94B**, **BDW94C**).



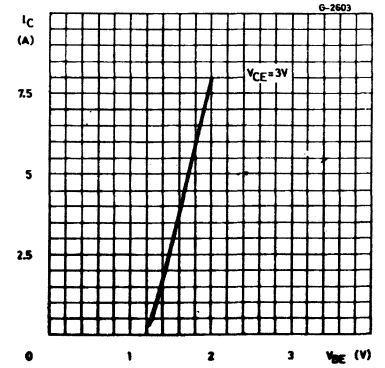
DC Current Gain (NPN types).



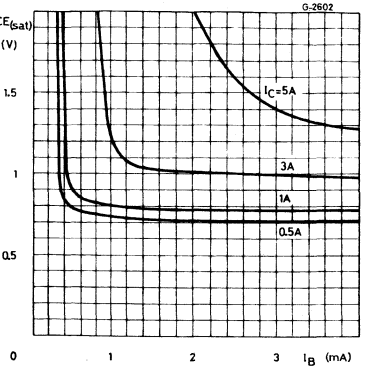
Collector-emitter Saturation Voltage (NPN types).



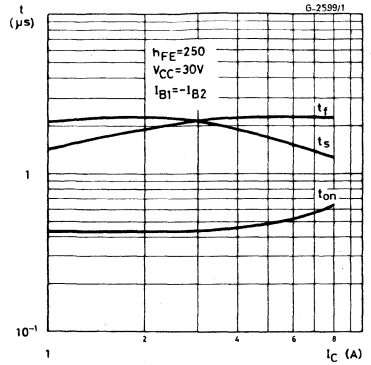
DC Transconductance (NPN types).



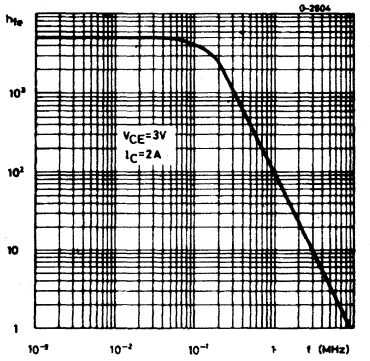
Collector-emitter Saturation Voltage (NPN types).



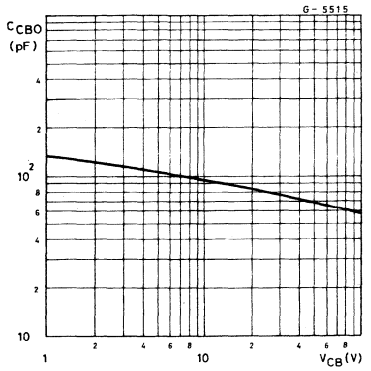
Saturated Switching Characteristics (NPN types).



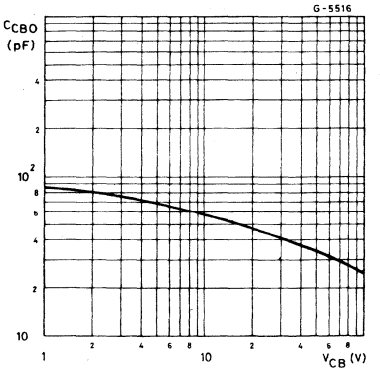
Small Signal Current Gain (NPN types).



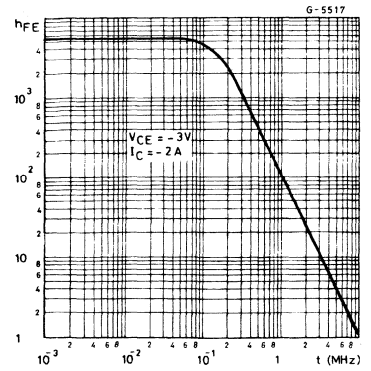
Collector-base Capacitance (PNP types).



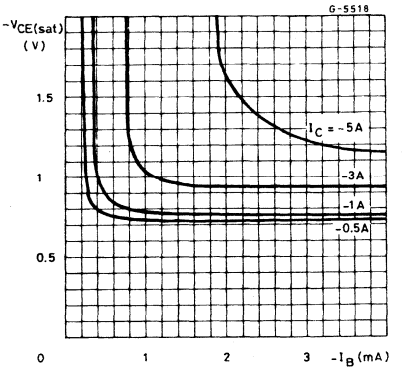
Collector-base Capacitance (NPN types).



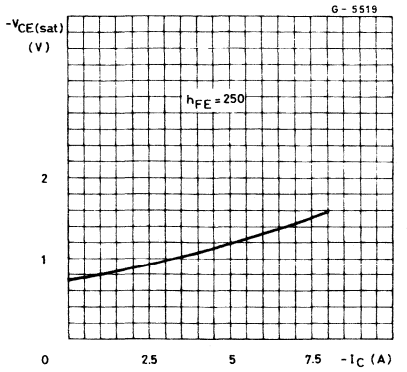
Small Signal Current Gain (PNP types).

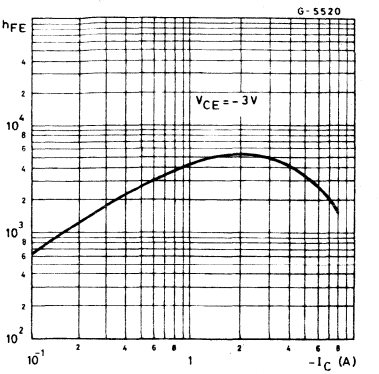


Collector-emitter Saturation Voltage (PNP types).

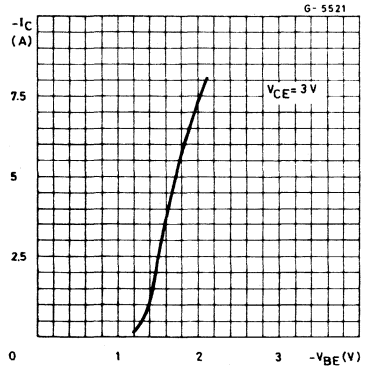


Collector-emitter Saturation Voltage (PNP types).

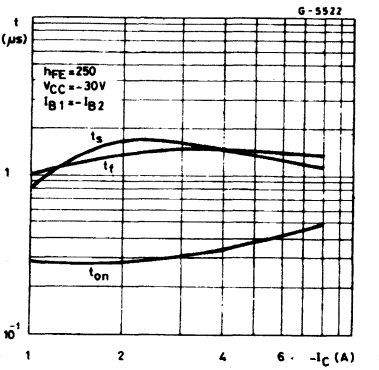




DC Transconductance (PNP types).

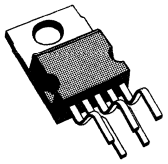


Saturated Switching Characteristics (PNP types).



VERY LOW DROP 5V REGULATOR

- PRECISE OUTPUT VOLTAGE (5 V ± 4 %)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)
- HIGH NOISE IMMUNITY ON RESET DELAY CAPACITOR



Pentawatt®

ORDER CODE : L387A

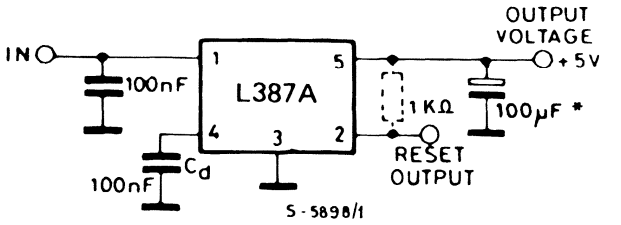
DESCRIPTION

The L387A is a very low drop voltage regulator in a Pentawatt® package specially designed to provide stabilized 5V supplies in consumer and industrial applications. Thanks to its very low input/output voltage drop this device is very useful in battery powered equipment, reducing consumption and prolonging battery life. A reset output makes the L387A particularly suitable for microprocessor systems. This output provides a reset signal when power is applied (after an external programmable delay) and goes low when power is removed, inhibiting the microprocessor. An hysteresis on reset delay capacitor raises the immunity to the ground noise.

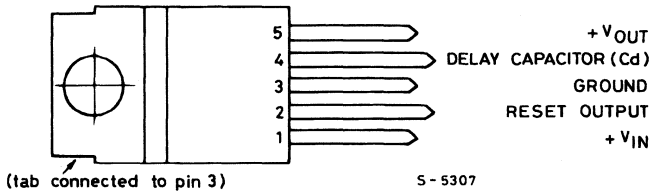
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	D.C. Input Voltage	35	V
T_J, T_{STG}	Junction and Storage Temperature Range	– 55 to 150	°C

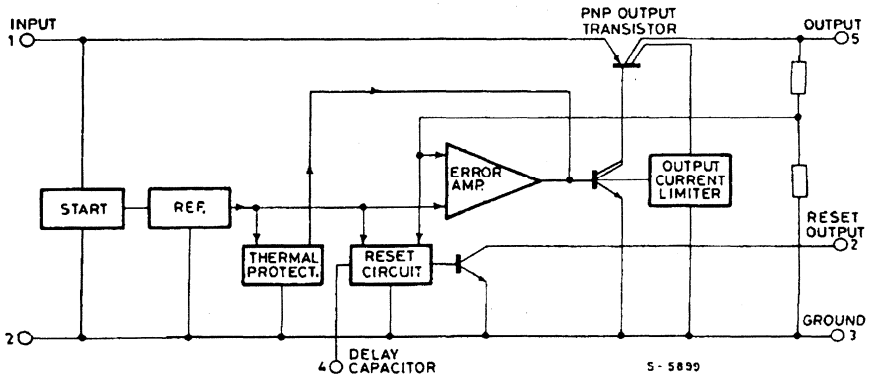
TEST AND APPLICATION CIRCUIT



PIN CONNECTIONS (top views)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3.5	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_i = 14.4V, T_j = 25°C, C_o = 100µF; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 5mA to 500mA T_j = 25°C $-40 \le T_j \le 125$°C	4.80 4.75	5.00 5.00	5.20 5.25	V
V_I	Operating Input Voltage	(*), Over Full T Range (– 40 to 125°C) (see note **)			26	V
ΔV_o	Line Regulation	V_i = 6V to 26V I_o = 5mA		5	50	mV
ΔV_o	Load Regulation	I_o = 5mA to 500mA		15	60	mV
$V_I - V_o$	Dropout Voltage	I_o = 350mA I_o = 500mA		0.40 0.60	0.65 0.80	V
I_q	Quiescent Current	I_o = 0mA I_o = 150mA I_o = 350mA I_o = 500mA		5 20 60 100	15 35 100 160	mA
		V_i = 6.2V I_o = 500mA		160	180	
$\frac{\Delta V_o}{\Delta T}$	Temperature Output Voltage Drift			– 0.5		mV/°C
SVR	Supply Voltage Rejection	I_o = 350mA f = 120Hz V_i = 12V ± $5V_{pp}$		60		dB
I_{SC}	Output Short Circuit Current			1.2	1.6	A
V_R	Reset Output Voltage	I_R = 3mA $1 < V_o < 4.75$V I_R = 16mA $1.5 < V_o < 4.75$V Over Full T (-40°C $\le T_j \le 125$°C)			0.5 0.8	V
I_R	Reset Output Leakage Current	V_o in Regulation Over Full T Range			50	µA
t_d	Delay Time for Reset Output	Cd = 100nF Over Full T Range		20		ms
$V_{RT\ (off)}$		V_o @ Reset out H to L Transition, Over Full T Range	4.75	V_o – 0.15		V
I_{C4}	Charging Current (current generator)	V_4 = 3V	10	20	30	µA
$V_{RT\ (on)}$	Power on V_o Threshold	V_o @ Reset out L to H Transition, Over Full T Range		$V_{RT\ (off)}$ + 0.05V	V_o – 0.04V	V
V_4	Comparator Threshold (pin 4)	V_4 @ Reset out H to L Transition	3.2		3.9	V
		V_4 @ Reset out L to H Transition	3.7	4.0	4.3	V
V_H	Hysteresis Voltage	Over Full T Range		450		mV

(*) For a DC voltage 26 < Vi < 35V the device is not operating.
(**) The limits are guaranteed by design, correlation and statistical control on production samples over the indicated temperature and supply voltage ranges.

Figure 1 :Dropout Voltage vs. Output Current.

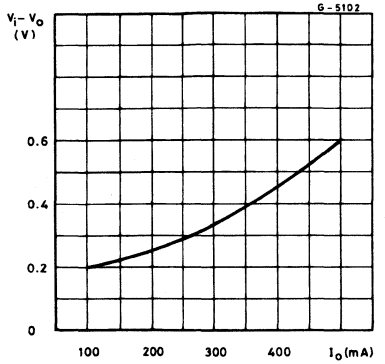


Figure 2 :Quiescent Current vs. Output Current.

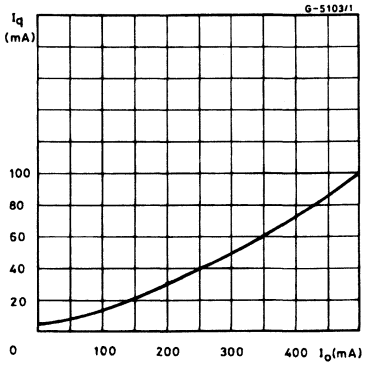
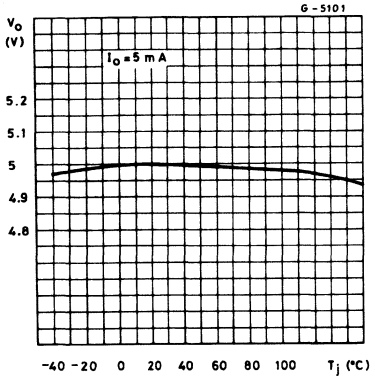


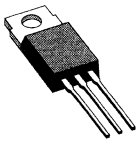
Figure 3 :Output Voltage vs. Temperature.



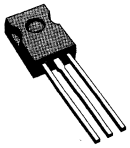
LOW DROPOUT VOLTAGE REGULATORS

- OUTPUT VOLTAGE OF 5, 8.5 AND 10 V
- OUTPUT CURRENT UP TO 500 mA
- NO EXTERNAL COMPONENTS
- LOW DROP-OUT VOLTAGE
- OVERVOLTAGE PROTECTION (± 100 V)
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION
- CURRENT LIMITING
- THERMAL SHUTDOWN

TO-220



SOT-82



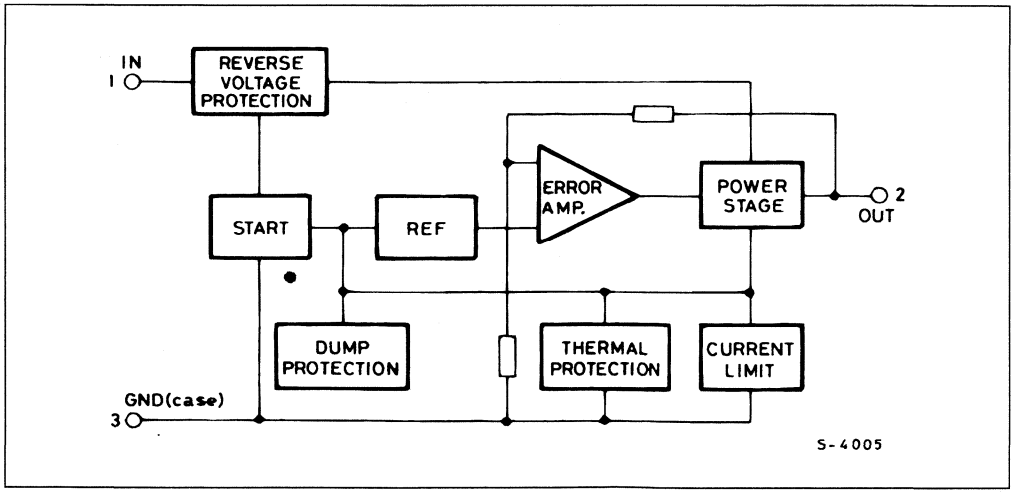
DESCRIPTION

The L2600 series of three terminal positive regulators is specially designed to stabilize power supplies car instrumentation in vehicles with 12V battery.Available with output voltages equal to 5V, 8.5V, 10V, they can supply an output current up to 500mA.

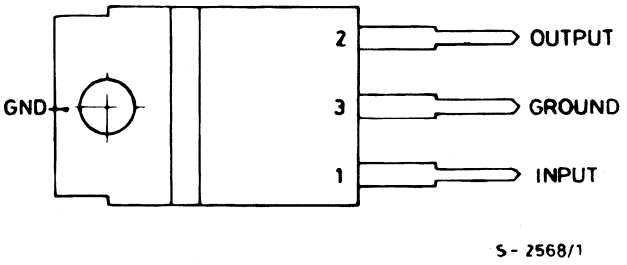
These devices are protected against load dump and field decay transients (± 100V), reverse battery, short circuit and thermal overload.

Order Codes		Output Voltage
TO-220	SOT-82	
L2605V	L2605X	5 V
L2685V	L2685X	8.5 V
L2610V	L2610X	10 V

BLOCK DIAGRAM



PIN CONNECTION (top view)



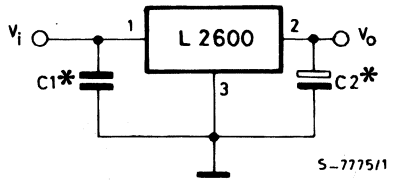
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	35	V
	DC Input Reverse Voltage	– 28	V
	Transient Input Overvoltage :		
	Load Dump : $5ms \leq t_{rise} \leq 10ms$, τ_f Fall Time Constant = 100ms, $R_{source} \geq 0.5\Omega$	+ 100	V
	Field Decay : $5ms \leq t_{fall} \leq 10ms$ τ_r Rise Time Constant = 33ms, $R_{source} \geq 10\Omega$	– 100	V
P_D	Power Dissipation	Internally Limited	
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

THERMAL DATA

			SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	8 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100 °C/W	75 °C/W

APPLICATION CIRCUIT



(*) **Note :** C_1 and C_2 are only needed if the load capacitance exceeds 1000 pF, Recommended values are $C_1 = 0.1\ \mu F$ and $C_2 \geq 100\ \mu F$.

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, V_i = 14 V, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 500 mA	V_i = 12 to 16 V (L2605) V_i = 12 to 16 V (L2685) V_i = 12 to 16 V (L2610)	4.80 8.15 9.60	5.00 8.50 10.00	5.20 8.85 10.40	V
V_i	Operating Input Voltage	See Note (*)				28	V
$\frac{\Delta V_o}{V_o}$	Line Regulation	I_o = 50 mA	V_i = 12 to 20 V		2	8	mV/V
	Load Regulation	V_i = 14 V	I_o = 50 to 500 mA		4	9	mV/V
ΔV_{i-o}	Dropout Voltage	I_o = 500 mA				1.9	V
I_d	Quiescent Current	I_o = 50 mA			20	45	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 50 mA V_i = 14 V	T_{amb} = – 12 to 80 °C		– 1		mV/°C
I_{sc}	Output Short Circuit Current				1.1	1.8	A
SVR	Supply Voltage Rejection	V_i = 16 V f = 100 Hz	V_i = 2 V I_o = 500 mA		60		dB
R_o	Output Resistance	I_o = 500 mA			0.05		Ω
e_N	Output Noise Voltage	BW = 100 Hz to 10 KHz			20		μV

(*) **Note :** For DC input voltage 28 V < V_i < 35 V the device is not operating.

ELECTRICAL CHARACTERISTICS (– 40 ≤ T_j ≤ 125 °C (note 2), V_i = 14 V, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 500 mA	V_i = 12.5 to 16 V (L2605) V_i = 12.5 to 16 V (L2685) V_i = 12.5 to 16 V (L2610)	4.70 8.00 9.40	5.00 8.50 10.00	5.30 9.00 10.60	V
V_i	Operating Input Voltage	See Note (°)				26	V
$\frac{\Delta V_o}{V_o}$	Line Regulation	I_o = 50 mA	V_i = 12.5 to 20 V		3	12	mV/V
	Load Regulation	V_i = 14 V	I_o = 50 to 500 mA		5	13	mV/V
ΔV_{i-o}	Dropout Voltage	I_o = 500 mA				2.5	V
I_d	Quiescent Current	I_o = 50 mA			29	65	mA
I_{sc}	Output Short Circuit Current				1.1	2.1	A

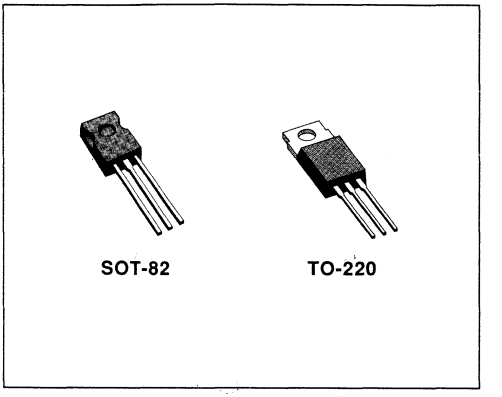
Notes : (°). For a DCinput voltage 26 V < Vi < 35 V the device is not operating.

2. The limits are guaranteed by design, correlation and statistical control on production samples over the indicated temperature and supply voltage ranges.

L4805-L4885-L4892 L4810-L4812

VERY LOW DROP VOLTAGE REGULATORS

- INPUT/OUTPUT DROP TYP. 0.4V
- 400mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- REVERSE POLARITY PROTECTION
- OVERVOLTAGE PROTECTION (± 60V)
- FOLDBACK CURRENT LIMITING
- THERMAL SHUTDOWN

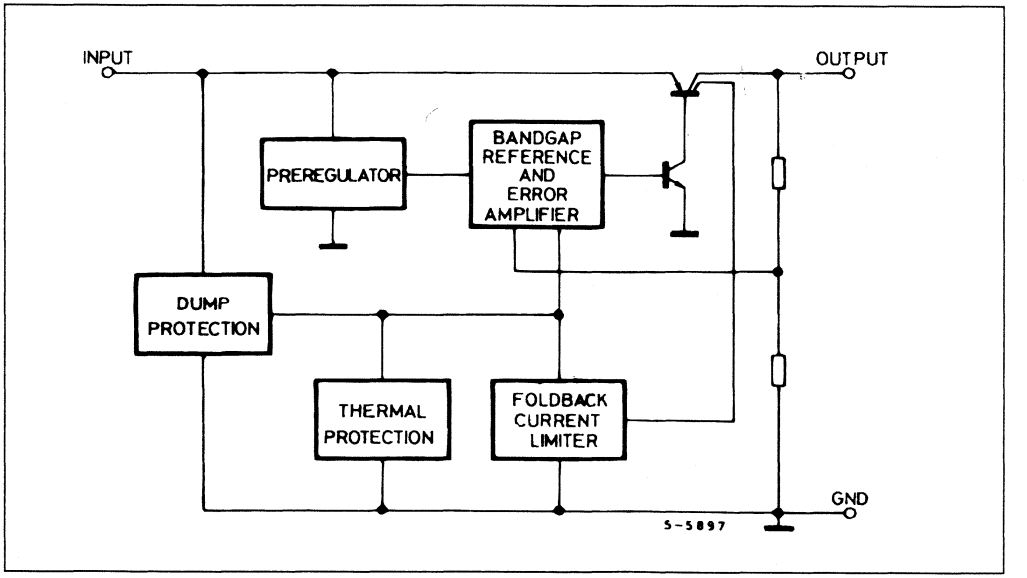


DESCRIPTION

L4800 series devices are voltage regulators with a very low voltage drop (typically O.4V at full rated current), output current up to 400mA, low quiescent current and comprehensive on-chip protection. These devices are protected against load dump and field decay transients of ± 60V, polarity reversal and overheating. A foldback current limiter protects against load short circuits. Available in 5V, 8.5V, 9.2V, 10V and 12V versions (all ± 4%, T_j = 25°C) these regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.

In automotive applications the L4805 is ideal for 5V logic supplies because it functions even when the battery voltage falls below 6V. In battery backup and standby applications the low consumption of these devices extends battery life.

BLOCK DIAGRAM



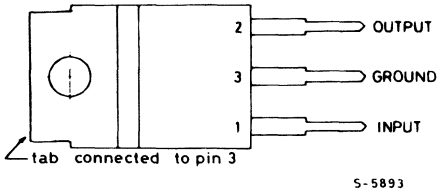
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage	+ 35	V
	Reverse Input Voltage	– 18	V
	Transient Input Overvoltages : Load Dump : 5ms ≤ T_{rise} ≤ 10ms, τ_f Fall Time Constant = 100ms, R_{source} ≥ 0.5Ω	60	V
	Field Decay : 5ms ≤ t_{fall} ≤ 10ms, R_{source} ≥ 10Ω τ_r Rise Time Constant = 33ms	– 60	V
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to + 150	°C

THERMAL DATA

			SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	8 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100 °C/W	75 °C/W

PIN CONNECTION (top view)



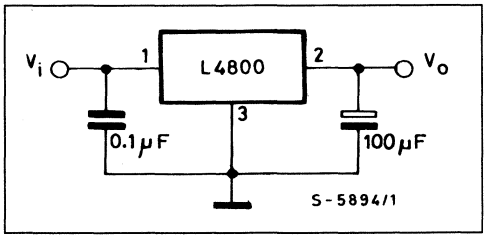
Order Codes		Output Voltage
TO-220	SOT-82	
L4805CV	L4805CX	5 V
L4885CV	L4885CX	8.5 V
L4892CV	L4892CX	9.2 V
L4810CV	L4810CX	10 V
L4812CV	L4812CX	12 V

TEST AND APPLICATION CIRCUIT

The output capacitor is required for stability. Though the 100 µF shown is the minimum recommended value, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristics of a particular system.

Capacitors must also be rated at all ambient temperature expected in the system. Many aluminum type electrolytics will freeze at temperatures less than – 30 °C, reducing their effective capacitance to zero. To maintain regulator stability down to – 40 °C, capacitors rated at that temperature (such as tantalums) must be used.



ELECTRICAL CHARACTERISTICS (V_i = 14.4 V, T_j = 25 °C, C_o = 100 µF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 5 mA to 400 mA*	4.80	5.00	5.20	V
			8.16	8.50	8.84	V
			8.83	9.20	9.57	V
			9.60	10.00	10.40	V
			11.50	12.00	12.50	V
V_i	Operating Input Voltage				26	V
$\Delta V_o/V_o$	Line Regulation	V_i = 13 to 26 V I_o = 5 mA		1	10	mV/V
$\Delta V_o/V_o$	Load Regulation	I_o = 5 to 400 mA*		3	15	mV/V
$V_i - V_o$	Dropout Voltage	I_o = 400 mA*		0.4	0.7	V
		I_o = 150 mA		0.2	0.4	V
I_q	Quiescent Current	I_o = 0 mA		0.8	2	mA
		I_o = 150 mA		25	45	mA
		I_o = 400 mA*		65	90	mA
$\frac{\Delta V_o}{\Delta T \cdot V_o}$	Temperature Output Voltage Drift			0.1		$\frac{mV}{°C \cdot V}$
SVR	Supply Voltage Rejection	I_o = 350 mA f = 120 Hz C_o = 100 µF $V_i = V_o + 3\ V + 2\ V_{PP}$		60		dB
I_o	Max Output Current			800		mA
I_{sc}	Output Short Circuit Current (fold back condition)			350	500	mA

* only for L4892 the current test condition is Io = 300mA.

ELECTRICAL CHARACTERISTICS(V_i = 14.4 V, – 40 ≤ T_J ≤ 125 °C (note 1), C_o = 100 µF, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 5 mA to 400 mA*	4.70	5.00	5.30	V
			8.00	8.50	9.00	V
			8.65	9.20	9.75	V
			9.40	10.00	10.60	V
			11.30	12.00	12.70	V
V_i	Operating Input Voltage	see note 2			26	V
$\Delta V_o/V_o$	Line Regulation	V_i = 14 to 26 V I_o = 5 mA		2	15	mV/V
$\Delta V_o/V_o$	Load Regulation	I_o = 5 to 400 mA*		5	25	mV/V
$V_i - V_o$	Dropout Voltage	I_o = 400 mA*		0.5	0.9	V
		I_o = 150 mA		0.25	0.5	V
I_q	Quiescent Current	I_o = 0 mA		1.2	3	mA
		I_o = 150 mA		40	70	mA
		I_o = 400 mA*		80	140	mA
I_o	Max Output Current			870		mA
I_{sc}	Output Short Circuit Current (fold back condition)			230		mA

Notes : 1. This limits are guaranteed by design, correlation and statistical control on production samples over the indicated temperature and supply voltage ranges..
2. For a DC voltage 26V < Vi < 35V the device is not operating.

Figure 1 : Dropout Voltage vs. Output Current.

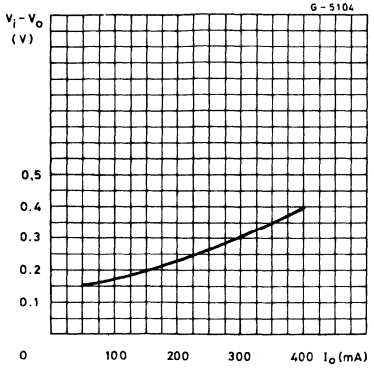


Figure 2 : Quiescent Current vs. Output Current.

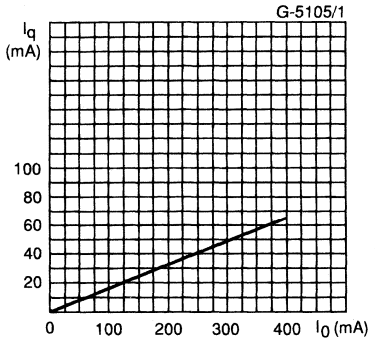


Figure 3 : Output Voltage vs. Temperature.

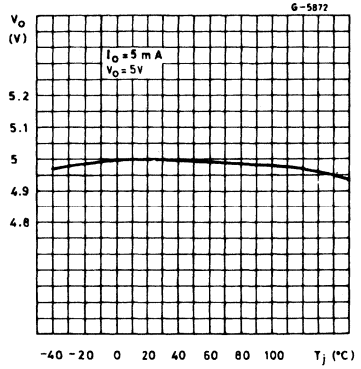


Figure 4 : Foldback Current Limiting (L4805).

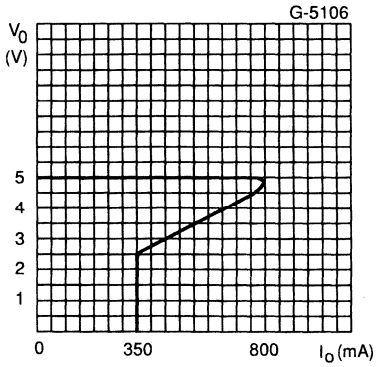
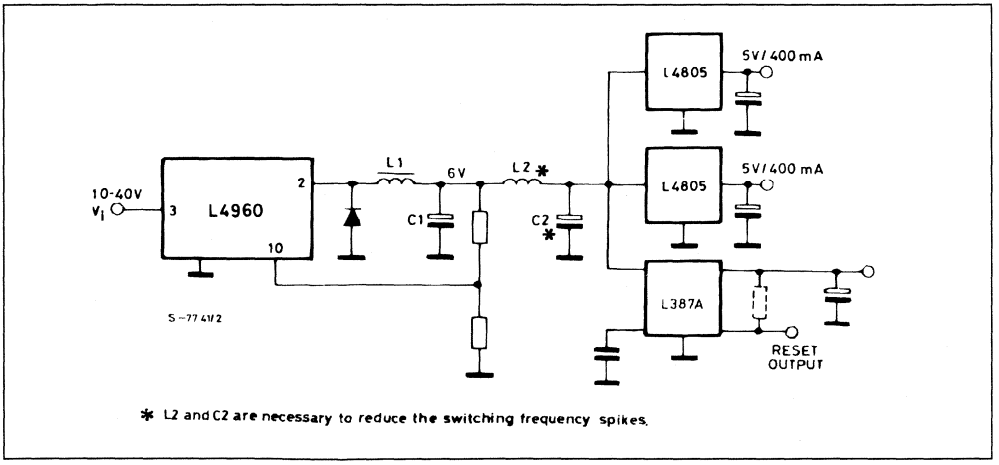


Figure 5 : Preregulator for Distributed Supplies.



SGS-THOMSON MICROELECTRONICS

L4901A

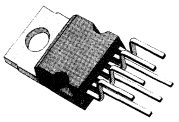
DUAL 5V REGULATOR WITH RESET

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{o1} = 400mA
  I_{o2} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4901A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



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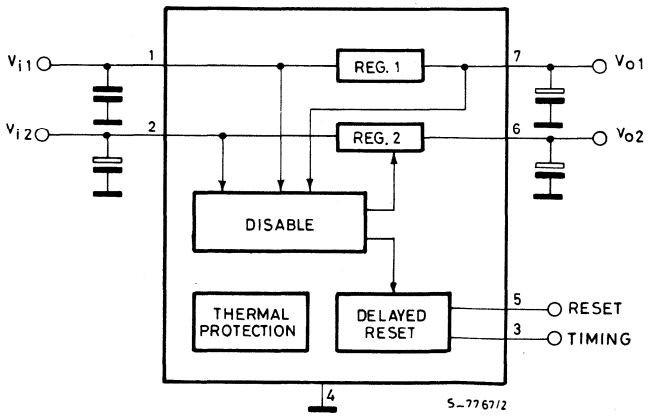
ORDERING NUMBER: L4901A

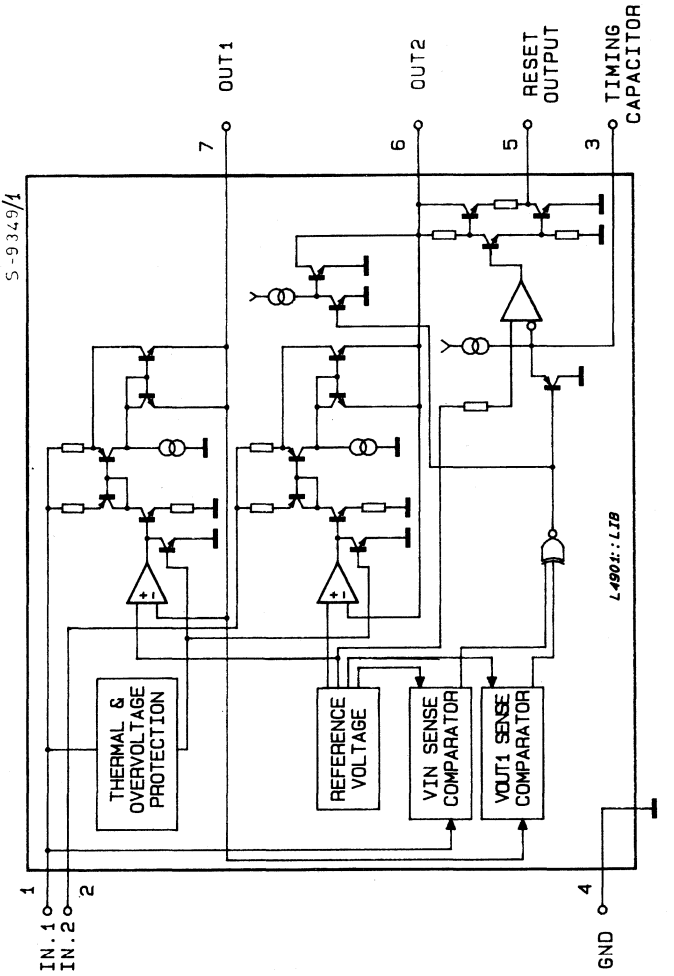
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

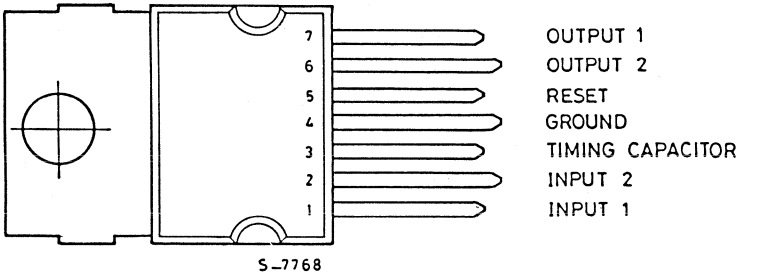
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



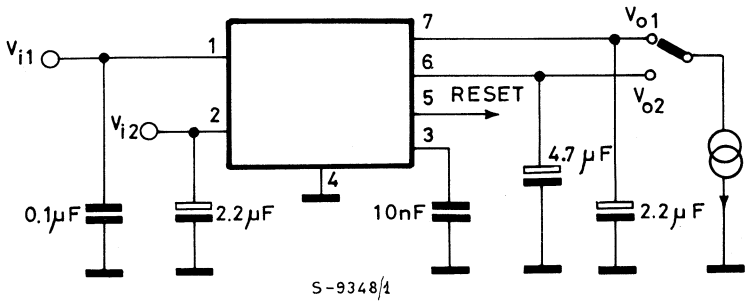
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 400mA regulator input.
2	INPUT 2	400mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF)
6	OUTPUT 2	5V - 400mA regulator output. Enabled if $V_{O\,1} > V_{RT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 400mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_{IN1} = V_{IN2} = 14{,}4V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{o1}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{o2H}	Output voltage 2 HIGH	R load 1KΩ	V_{o1}-0.1	5	V_{o1}	V
V_{o2L}	Output voltage 2 LOW	I_{o2} = -5mA		0.1		V
I_{o1}	Output current 1	ΔV_{o1} = -100mV	400			mA
I_{LO1}	Leakage output 1 current	V_{IN} = 0 $V_{o1} \leq$ 3V			1	µA
I_{o2}	Output current 2	ΔV_{o2} = -100mV	400			mA
V_{io1}	Output 1 dropout voltage (*)	I_{o1} = 10mA I_{o1} = 100mA I_{o1} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input threshold voltage		V_{o1}+1.2	6.4	V_{o1}+1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{o1}	Line regulation 1	7V < V_{IN} < 18V I_{o1} = 5mA		5	50	mV
ΔV_{o2}	Line regulation 2	I_{o2} = 5mA		5	50	mV
ΔV_{o1}	Load regulation 1	5mA < I_{o1} < 400mA		50	100	mV
ΔV_{o2}	Load regulation 2	5mA < I_{o2} < 400mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{o2} = $I_{o1} \leq$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{o1} \leq$ 5mA I_{o2} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4901A makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

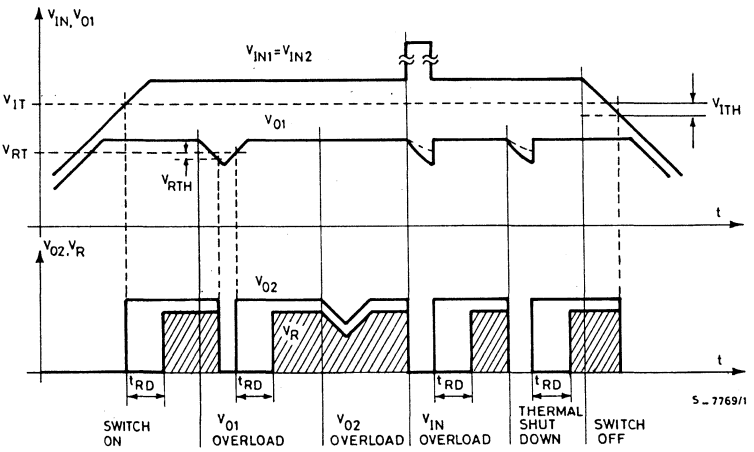
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4901A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

The L4901A is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shown in fig. 5 the reset output is used both to disable the μP and, through the address decoder M74HC138, to ensure that the RAMS are disabled as soon as the main supply starts to fall.

Another interesting application of the L4901A is in μP system with shadow memories. (see fig. 6)

When the input voltage goes below V_{IT}, the reset output enables the execution of a routine that saves the machine's state in the shadow RAM (xicor x 2201 for example).

Thanks to the low consumption of the Reg. 1 a 680μF capacitor on its input is sufficient to provide enough energy to complete the operation. The diode on the input guarantees the supply of the equipment even if a short circuit on V_I occurs.

APPLICATION SUGGESTION (continued)

Fig. 2

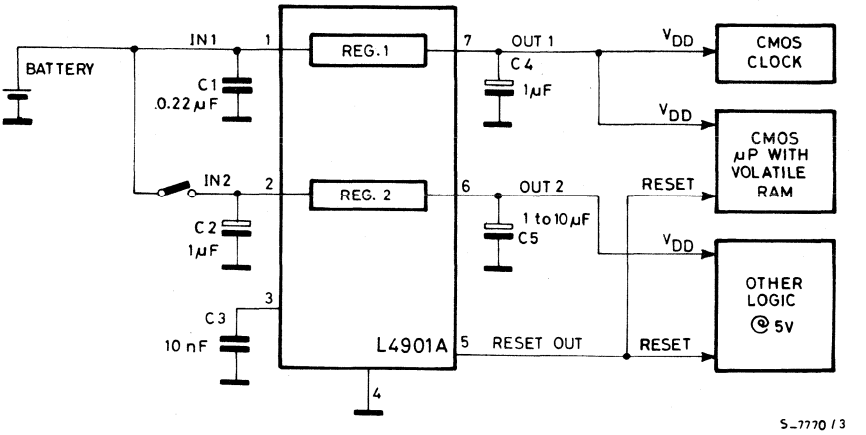
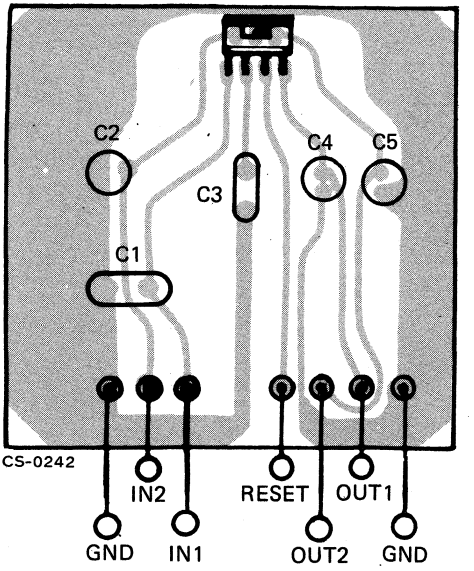


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

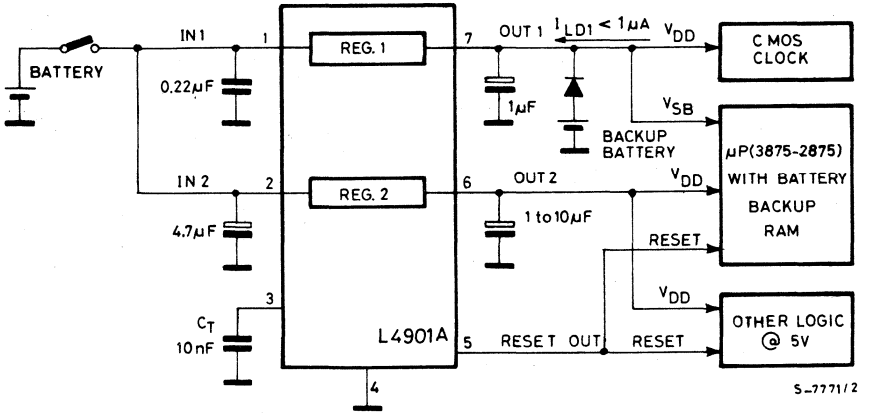
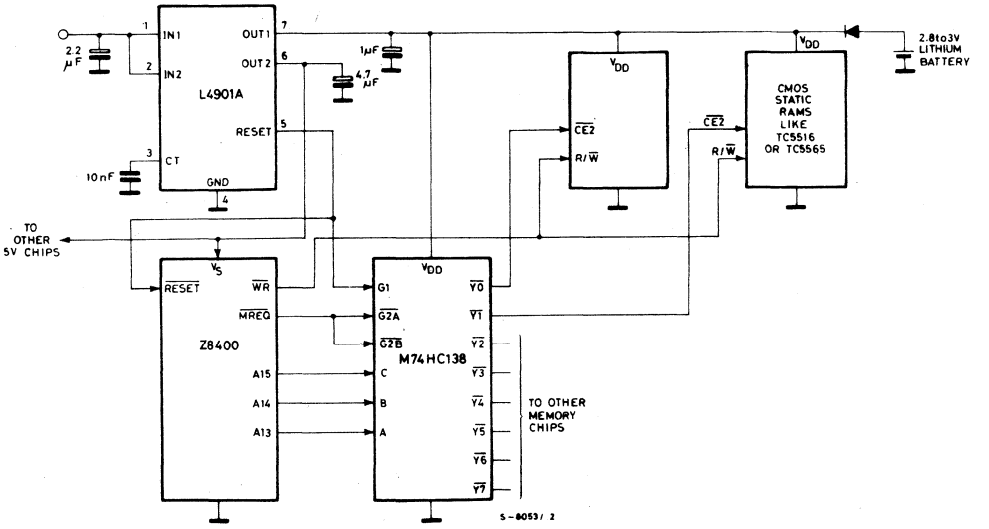


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6

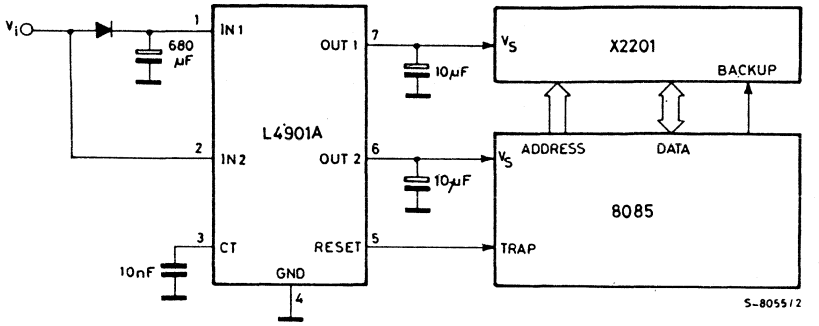


Fig. 7 - Quiescent current (Reg. 1) vs. output current

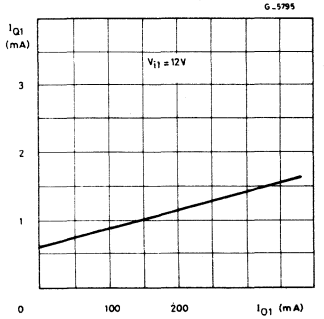


Fig. 8 - Quiescent current (Reg. 1) vs. input voltage

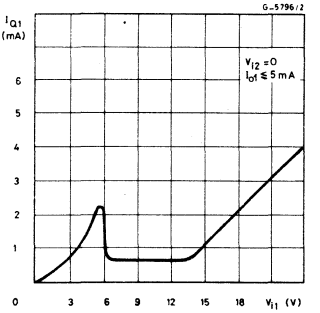


Fig. 9 - Total quiescent current vs. input voltage

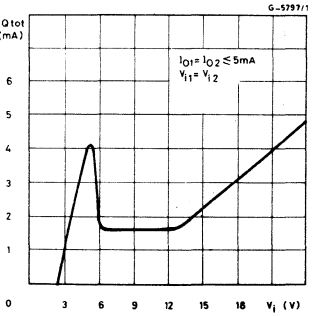


Fig. 10 - Regulator 1 output current and short circuit current vs. input voltage

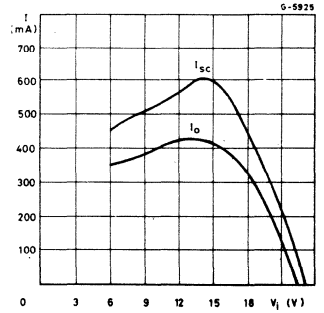


Fig. 11 - Regulator 2 output current and short circuit current vs. input voltage

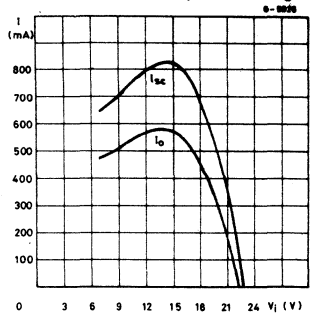
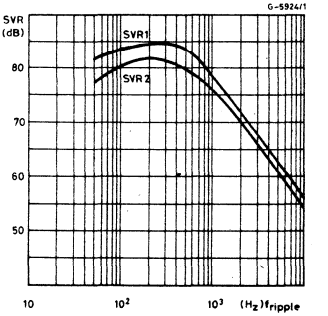


Fig. 12 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence

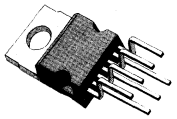


DUAL 5V REGULATOR WITH RESET AND DISABLE

PRELIMINARY DATA

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: I_{01} = 300mA
  I_{02} = 300mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- RESET OUTPUT NORMALLY HIGH
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4902A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.
Reset and data save functions and remote switch on/off control can be realized.



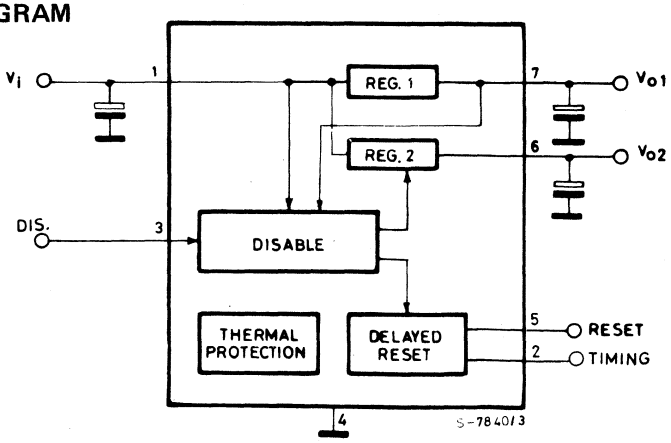
Heptawatt

ORDERING NUMBER: L4902A

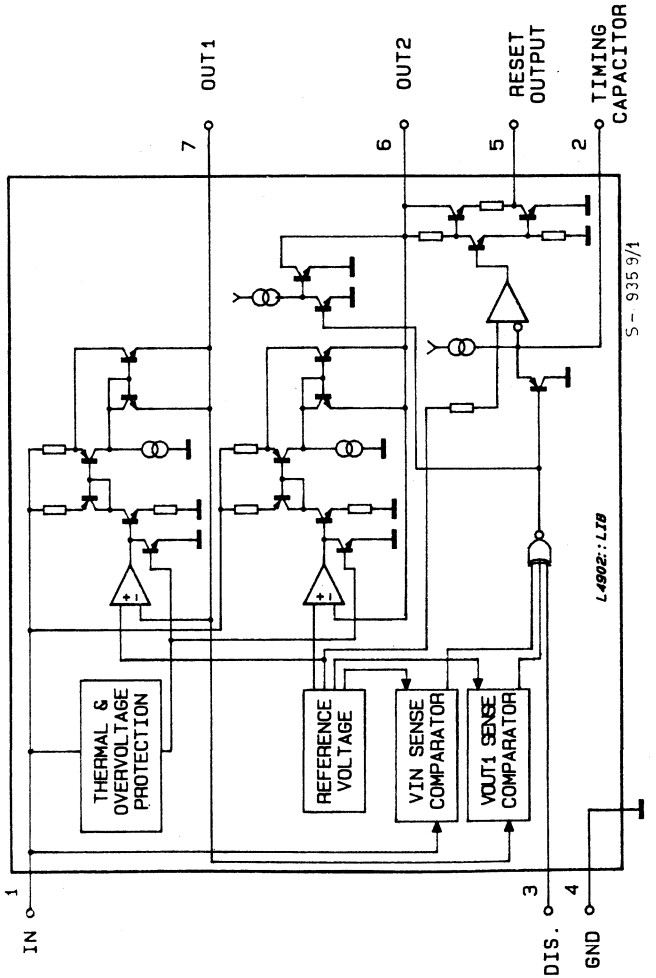
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
	Output current	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

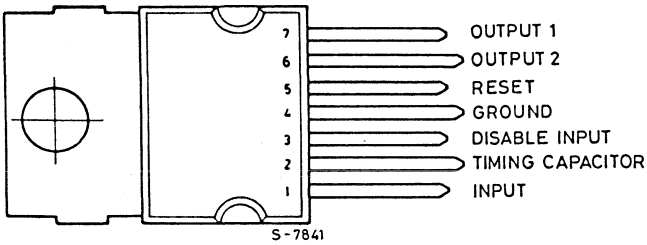
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



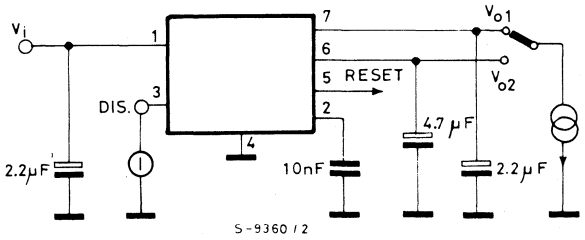
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Regulators common input.
2	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
3	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
4	GND	Common ground.
5	RESET OUTPUT	When pin 2 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF).
6	OUTPUT 2	5V - 300mA regulator output. Enabled if $V_O 1 > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 300mA. Low leakage (in switch-OFF condition) output.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				24	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max.	ΔV_{01} = -100mV	300			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2 max.	ΔV_{02} = -100mV	300			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 24V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 300mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 300mA		50	80	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -1mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-150 -30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R=0.5V I_o = 100mA	50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4902A makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with common inputs plus a reset output for the data save function and a Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:
- a high level ($> V_{DT}$) is applied on pin 3;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:
- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

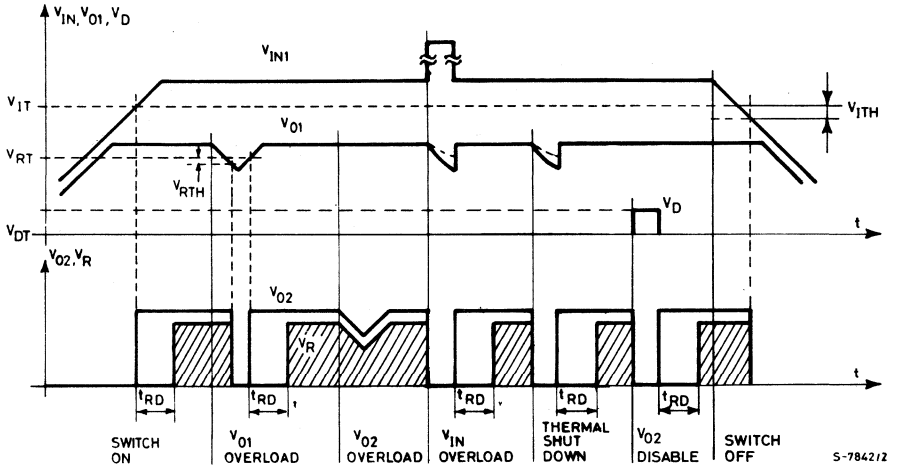
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



APPLICATION SUGGESTION

Fig. 2 illustrate how the L4902A's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Another application for the L4902A is supplying a shadow-ram microcomputer chip (SGS M38SH72 for exemple) where a fast NV memory is backed up on chip by a EEPROM when a low level on the reset output occurs.

By adding two CMOS-SCHMIDT-TRIGGER and few external components, also a watch dog function may be realized (see fig. 5). During normal operation the microsystem supplies a periodical pulse waveform; if an anomalous condition occours (in the program or in the system), the pulses will be absent and the disable input will be activated after a settling time determined by R1 C1. In this condition all the circuitry connected to V_{02} will be disabled, the system will be restarted with a new reset front.

The disable of V_{02} prevent spurious operation during microprocessor malfunctioning.

APPLICATION SUGGESTION (continued)

Fig. 2

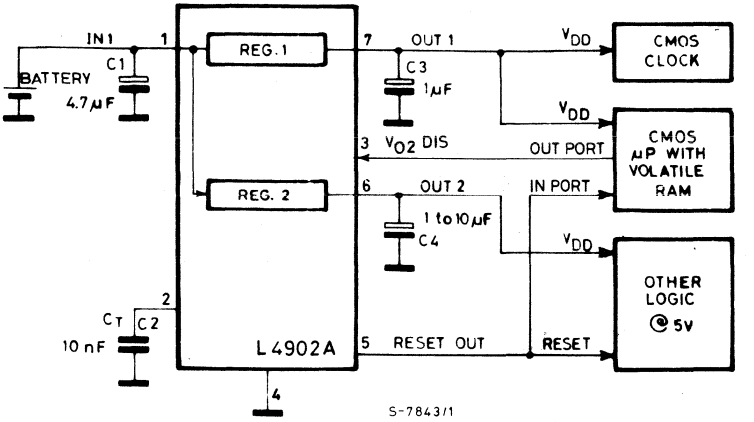
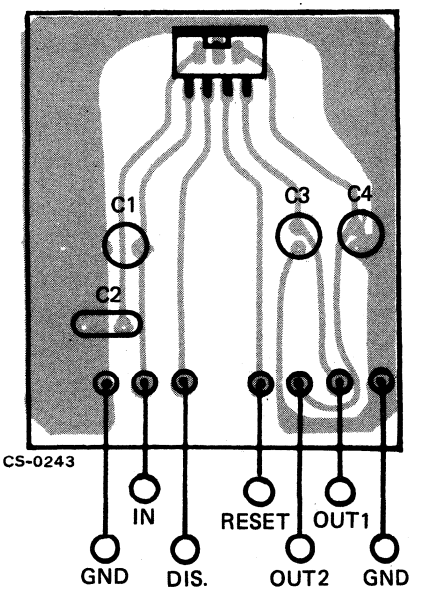


Fig. 3 - P.C. board and component layout of the circuit of Fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

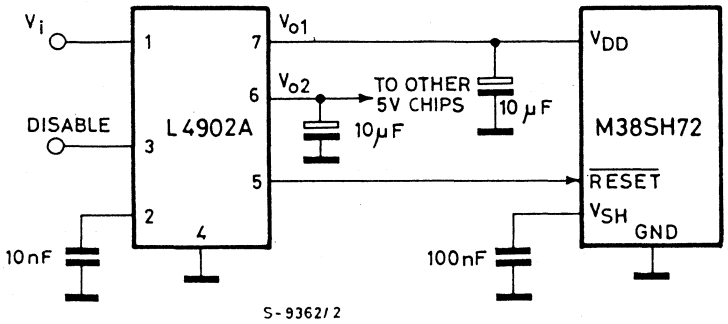
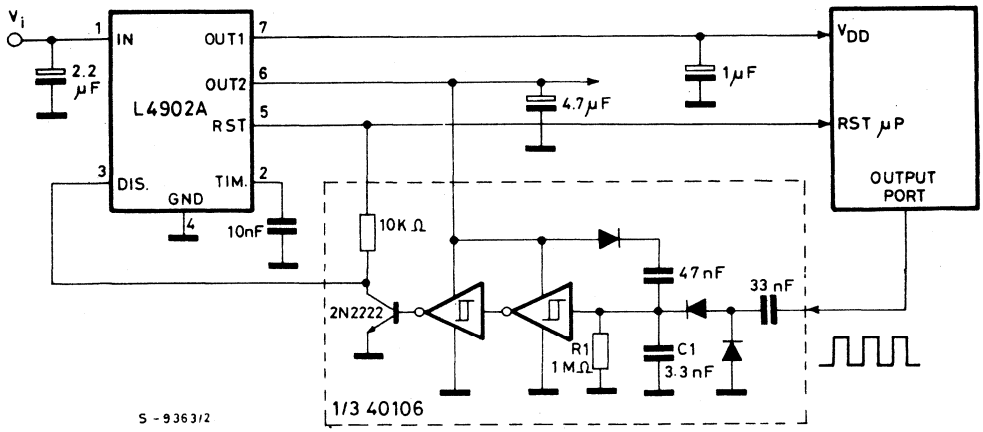


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6 - Quiescent current vs. output current

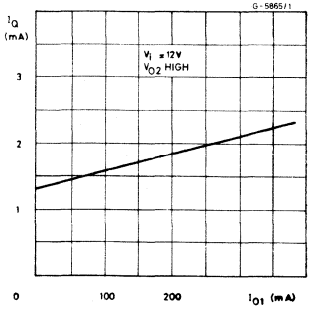


Fig. 7 - Quiescent current vs. input voltage

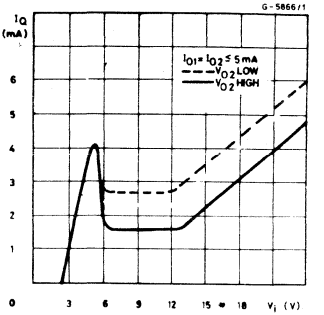
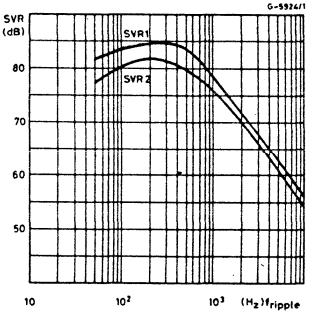


Fig. 8 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 50mA, I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4903 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset, data save functions and remote switch on/off control can be realized.

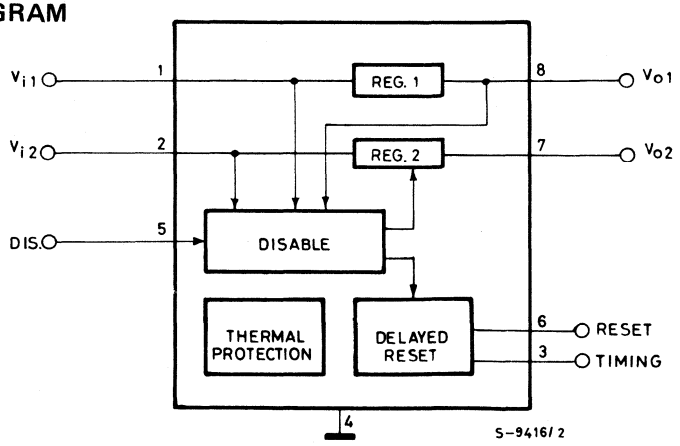
Minidip Plastic

ORDERING NUMBER: L4903

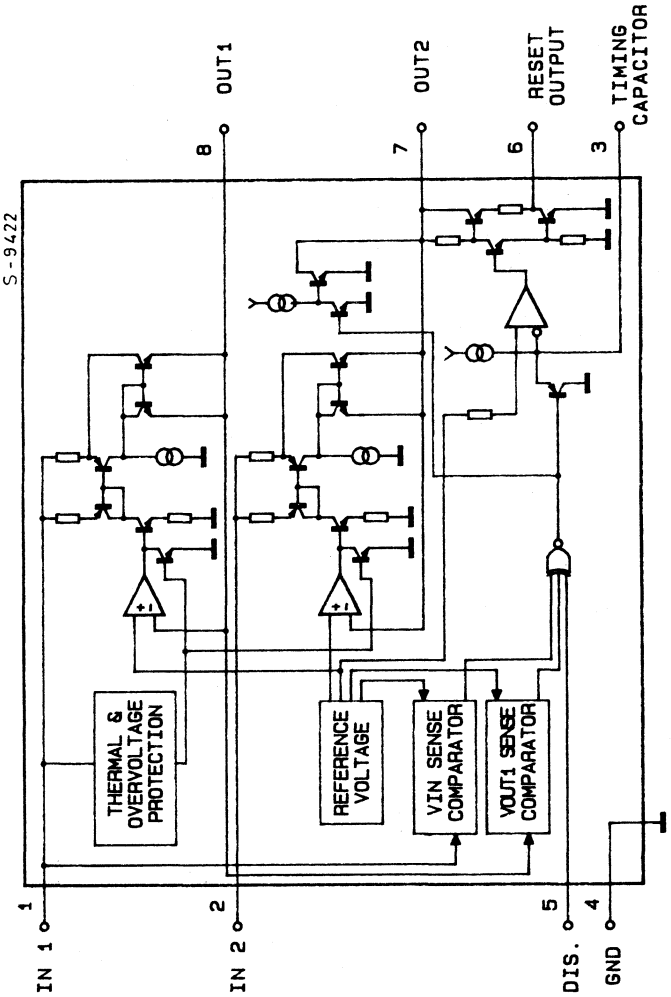
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
V_t	Transient input overvoltage (t = 40 ms)	60	V
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

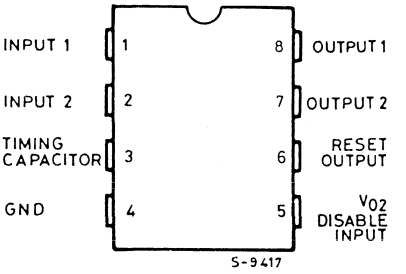
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



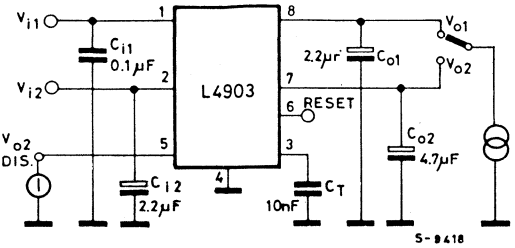
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disables output Reg. 2.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_t (\frac{5V}{10\mu A})$; t_{RD} (ms) = C_t (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if V_O 1 $> V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

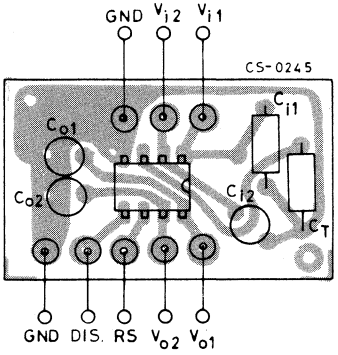
THERMAL DATA

$R_{th\ j\text{-}pin}$	Thermal resistance junction-pin 4	max	70	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max. (*)	ΔV_{01} = -100mV	50			mA
I_{LO1}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2 max. (*)	ΔV_{02} = -100mV	100			mA
V_{io1}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	V_{IN1} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 I_{01} < 5mA I_{02} = 0		0.6	0.9	mA

:LECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.4	4.7	V_{02}-0.2	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-150 30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	50	84		dB
SVR2	Supply voltage rejection	I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current conditions.

\PPLICATION INFORMATION

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:IRCUIT OPERATION (see Fig. 1)

\fter switch on Reg. 1 saturates until V_{01} rises :o the nominal value.

When the input 2 reaches V_{IT} and the output 1 s higher than V_{RT} the output 2 (V_{02} and V_R) switches on and the reset output (V_R) goes low after a programmable time T_{RD} (timing capacitor).

V_{02} is switched at low level and V_R at high level when one of the following conditions occurs:

- a high level ($> V_{DT}$) is applied on pin 5;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

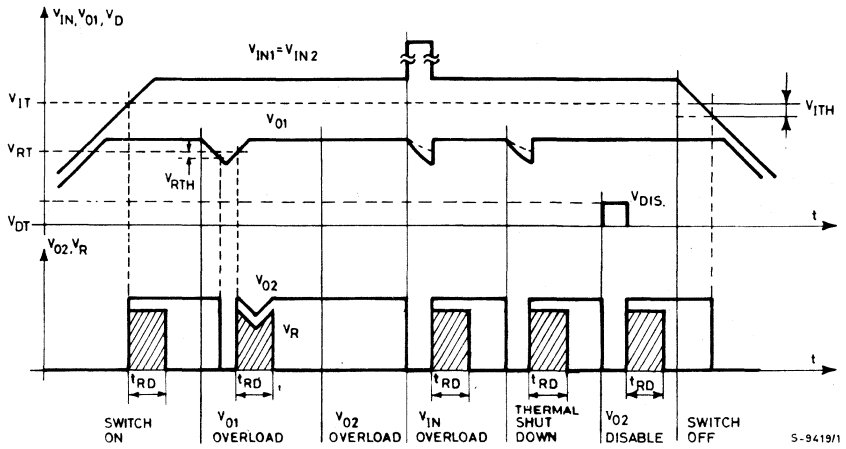
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



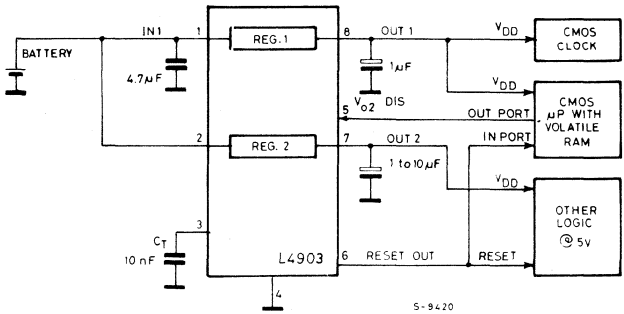
APPLICATION SUGGESTION

Fig. 2 illustrates how the L4903's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Fig. 2



PPLICATION SUGGESTIONS (continued)

Fig. 3 - Quiescent current (Reg. 1) vs. output current

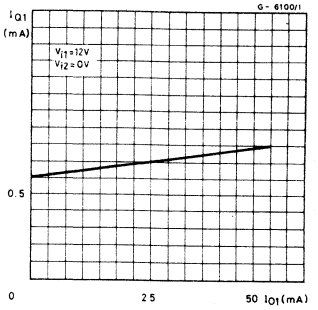


Fig. 4 - Quiescent current (Reg. 1) vs. input voltage

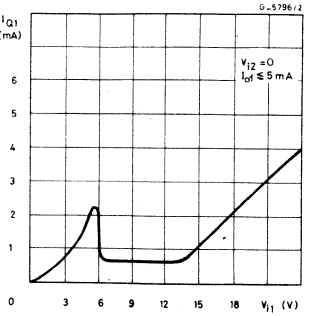


Fig. 5 - Total quiescent current vs. input voltage

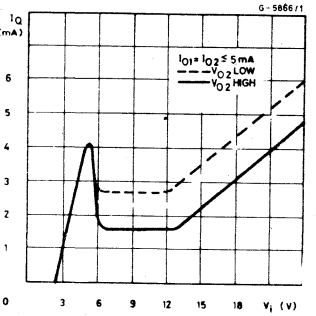
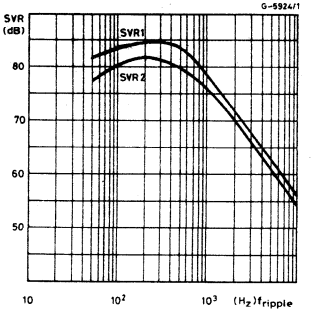


Fig. 6 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



SGS-THOMSON MICROELECTRONICS

L4904A

DUAL 5V REGULATOR WITH RESET

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{o1} = 50mA, I_{o2} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4904A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.

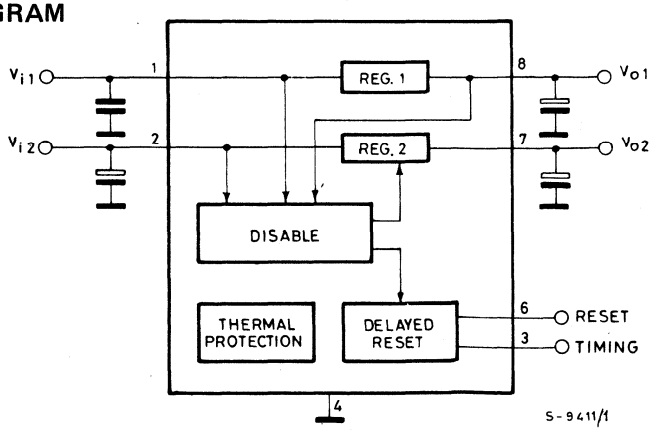
Minidip Plastic

ORDERING NUMBER: L4904A

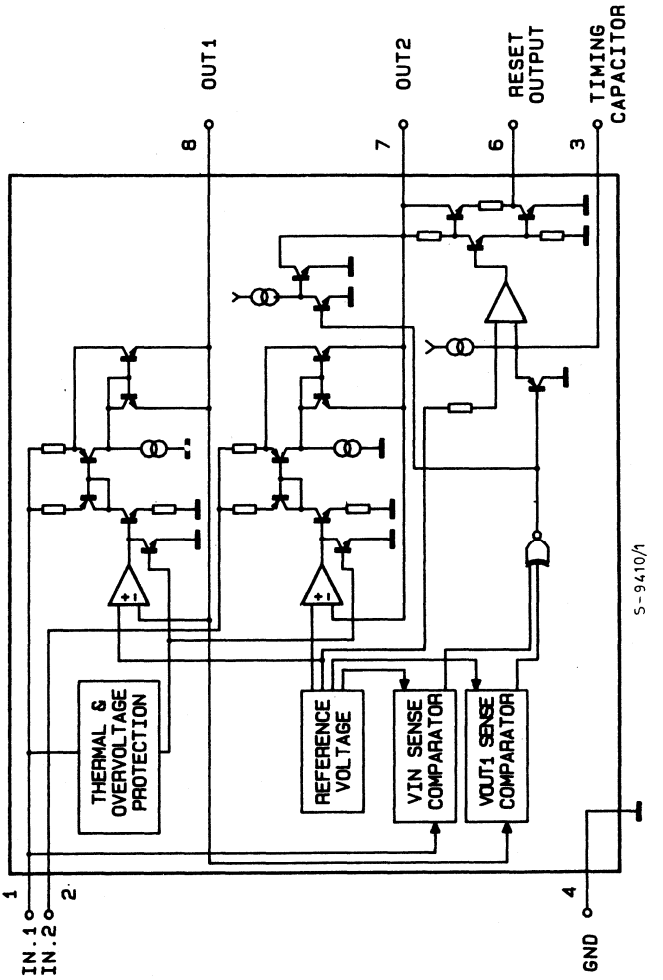
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_j	Storage and junction temperature	-40 to 150	°C

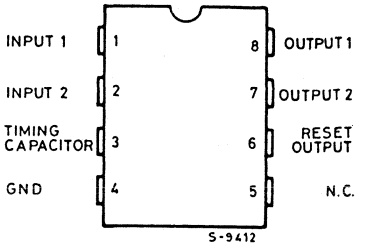
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



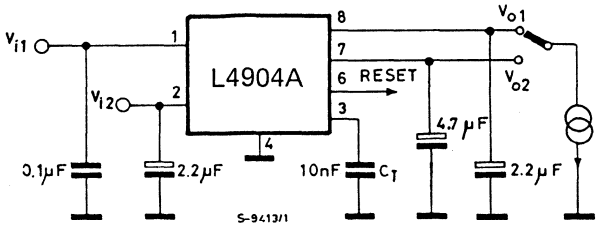
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

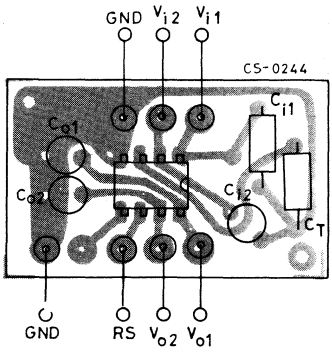
THERMAL DATA

$R_{th\,j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01} -0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	50			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	100			mA
V_{I01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01} +1.2	6.4	V_{01} +1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	
ΔV_{01}	Load regulation 1	V_{IN} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500µA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3		11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	µs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	50	84		dB
SVR2	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for µP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4904A makes it very easy to supply such equipments; it provides two voltage regulators (booth 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01} regulator also features low consumption (0.6mA

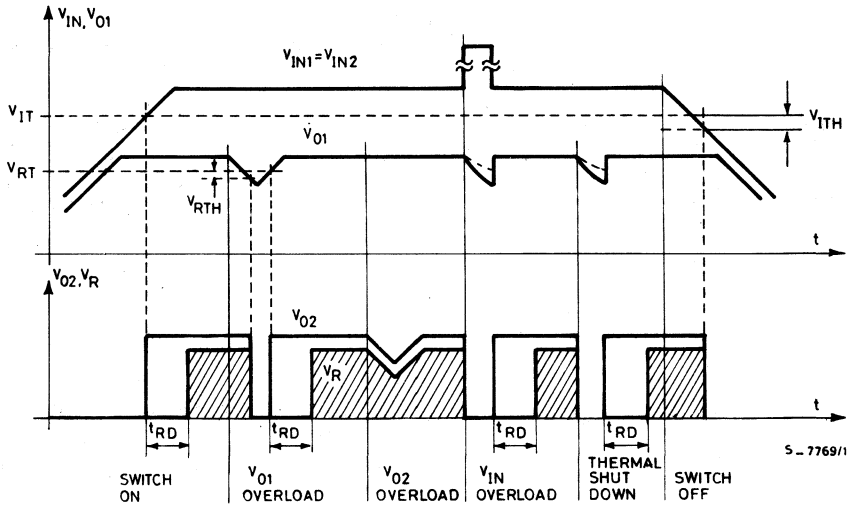
CIRCUIT OPERATION (continued)

typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a µP system.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 3 shows the L4904A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type C-MOS µP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTIONS (continued)

Application Circuits of a Microprocessor system (Fig. 2) or with data save battery (Fig. 3). The reset output provide delayed rising front at the turn-off of the regulator 2.

Fig. 2

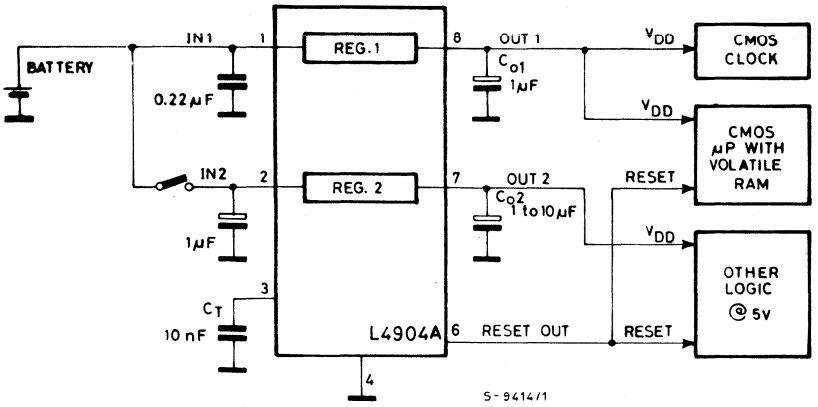
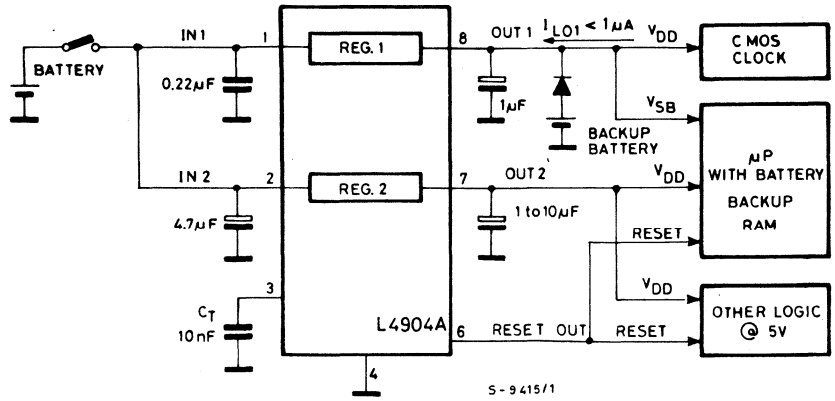


Fig. 3



APPLICATION SUGGESTIONS (continued)

Fig. 4 - Quiescent current (Reg. 1) vs. output current

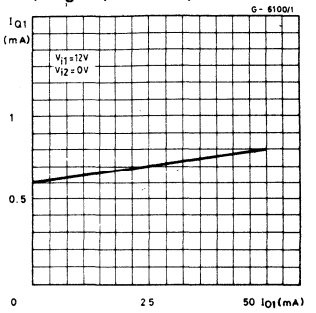


Fig. 5 - Quiescent current (Reg. 1) vs. input voltage

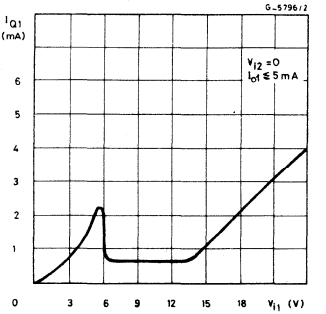


Fig. 6 - Total quiescent current vs. input voltage

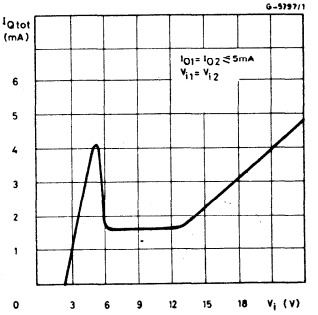
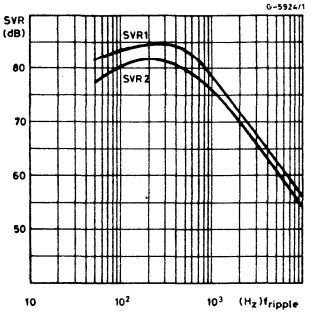


Fig. 7 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



SGS-THOMSON MICROELECTRONICS

L4905

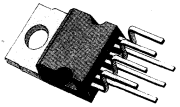
DUAL 5V REGULATOR WITH RESET

ADVANCE DATA

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: $I_{01} = 200mA$ $I_{02} = 300mA$
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 1%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCIENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4905 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



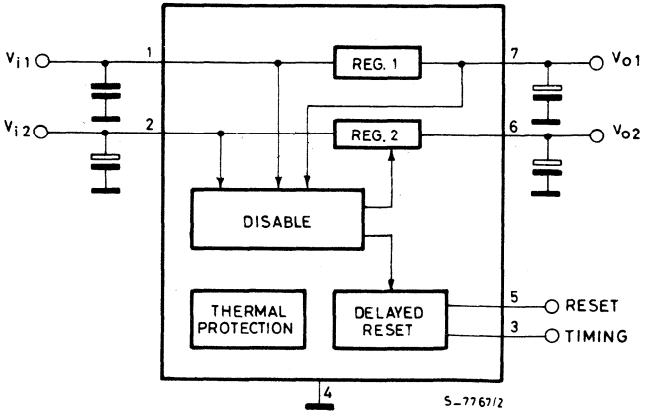
Heptawatt

ORDERING NUMBER: L4905

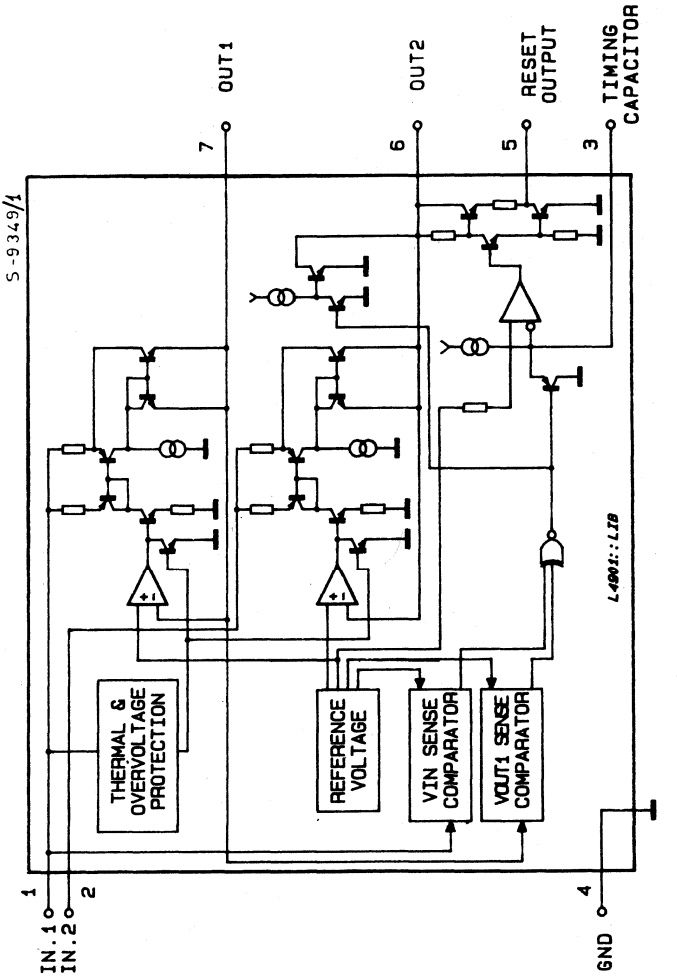
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

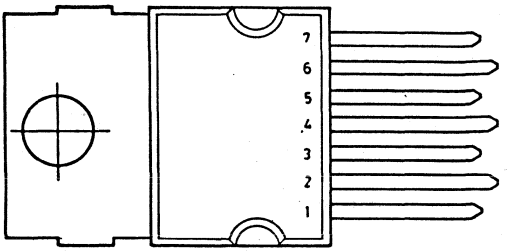
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



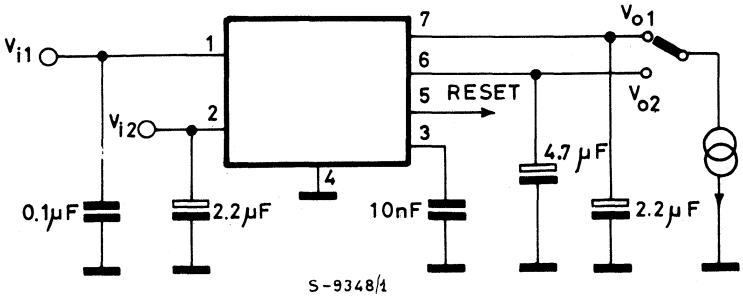
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 200mA regulator input.
2	INPUT 2	300mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A} \right)$; t_{RD} (ms) = C_t (nF)
6	OUTPUT 2	5V - 300mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{O2} capacitor is discharged.
7	OUTPUT 1	5V - 200mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_{IN1} = V_{IN2} = 14,4V$, $T_{amb} = 25°$ unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_I	DC operating input voltage				24	V
V_{01}	Output voltage 1	R load 1KΩ	5.0	5.05	5.1	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	200			mA
I_{LO1}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq 3V$			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	300			mA
V_{io1}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 200mA		0.7 0.8 1.05	0.8 1 1.3	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 24V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 200mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 300mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V $I_{02} = I_{01} \leq 5mA$		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq 5mA$ I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 - 0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 - 0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	54 50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4905 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;
- permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

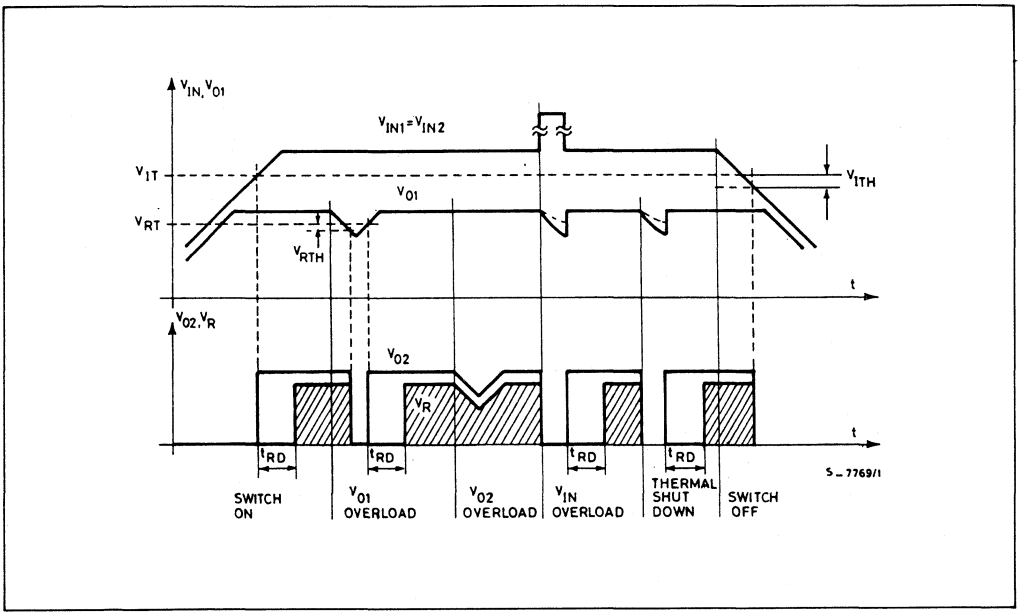
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4905 with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTION (continued)

Fig. 2

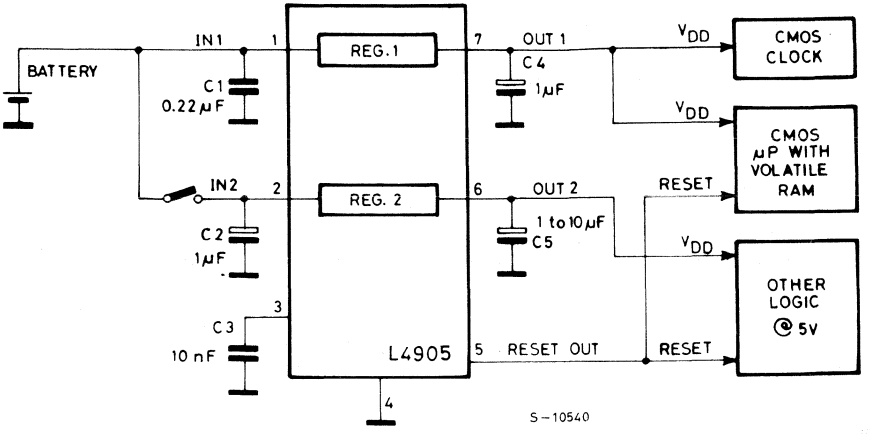
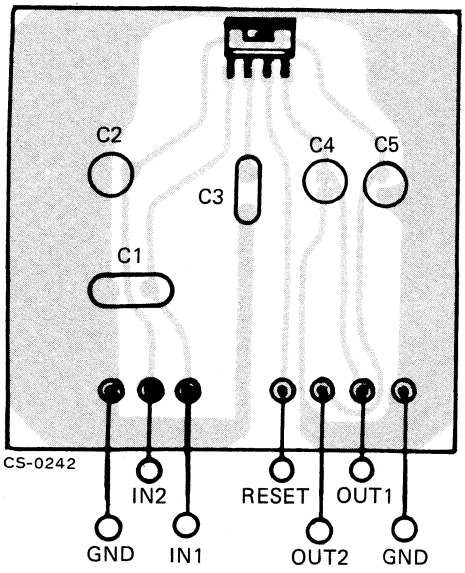


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

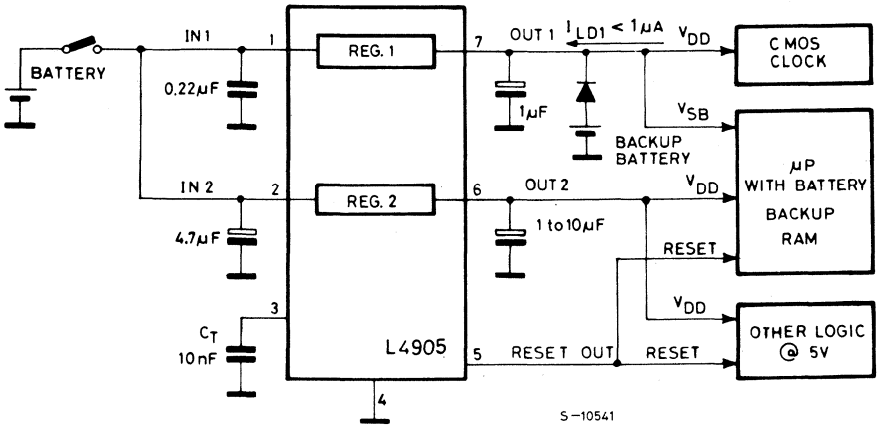


Fig. 5 - Quiescent current (Reg. 1) vs. output current

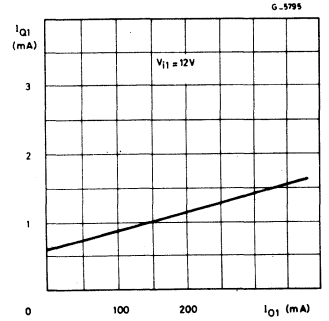


Fig. 6 - Quiescent current (Reg. 1) vs. input voltage

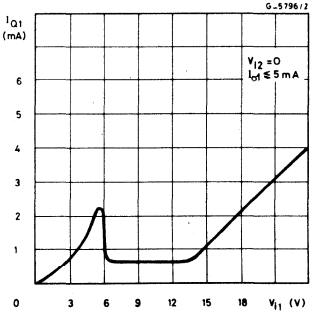
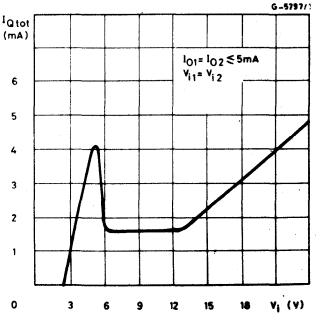


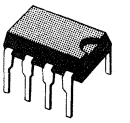
Fig. 7 - Total quiescent current vs. input voltage



VOLTAGE REGULATOR PLUS FILTER

PRELIMINARY DATA

- FIXED OUTPUT VOLTAGE 8.5 V
- 250 mA OUTPUT CURRENT
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION



POWER MINIDIP
(4 + 4)

ORDER CODE : L4916

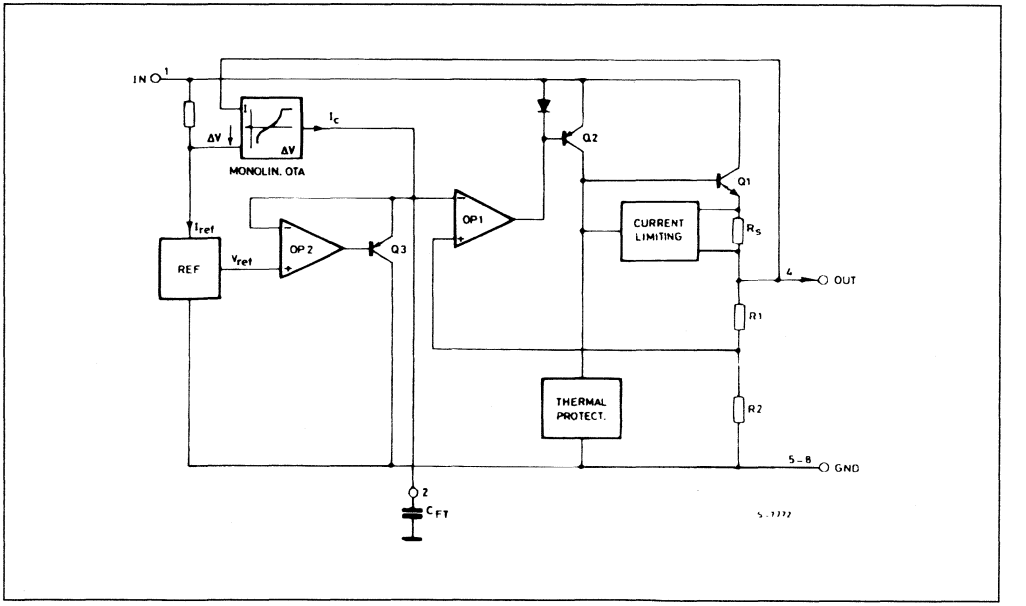
DESCRIPTION

This circuit combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wider input voltage range.

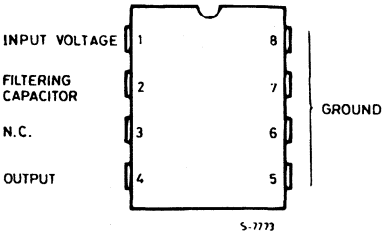
A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltages.

The non linear behaviour of this control circuitry allows a fast settling of the filter.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Peak Input Voltage (300 ms)	40	V
V_i	DC Input Voltage	28	V
I_O	Output Current	Internally Limited	
P_{tot}	Power Dissipation	Internally Limited	
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	20	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C; V_i = 13.5 V, test circuit of fig. 1, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Input Voltage				20	V
V_o	Output Voltage	V_i = 12 to 18 V I_o = 5 to 150 mA	8.1	8.5	8.9	V
$\Delta V_{I/O}$	Controlled Input-output Dropout Voltage	V_i = 5 to 10 V I_o = 5 to 150 mA		1.6	2.1	V
ΔV_o	Line Regulation	V_i = 12 to 18 V I_o = 10 mA		1	20	mV
ΔV_o	Load Regulation	I_o = 5 to 250 mA t_{on} = 30 µs t_{off} = ≥ 1 ms		50	100	mV
ΔV_O	Load Regulation (filter mode)	V_i = 8.5 V I_o = 5 to 150 mA t_{on} = 30 µs t_{off} = ≥ 1 ms		150	250	mV
I_q	Quiescent Current	I_o = 5 mA		1	2	mA
ΔI_q	Quiescent Current Change	V_i = 6 to 18 V I_o = 5 to 150 mA		0.05		mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 10 mA		1.2		mV/°C
SVR	Supply Voltage Rejection	V_{iac} = 1 V_{rms} f = 100 Hz I_o = 150 mA V_{IDC} = 12 to 18 V V_{IDC} = 6 to 11 V		 70 35(*)		 dB dB
I_{SC}	Short Circuit Current		250	300		mA
T_{on}	Switch On Time	I_o = 150 mA V_i = 5 to 11 V V_i = 11 to 18 V		 500(*) 300		 ms ms
T_J	Thermal Shutdown Junction Temperature			145		°C

(*) Depending of the C_{FT} capacitor.

Figure 1 : Test and Application Circuit.

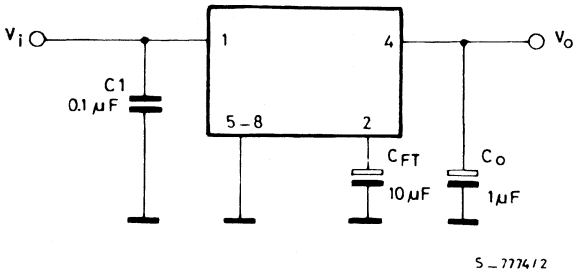
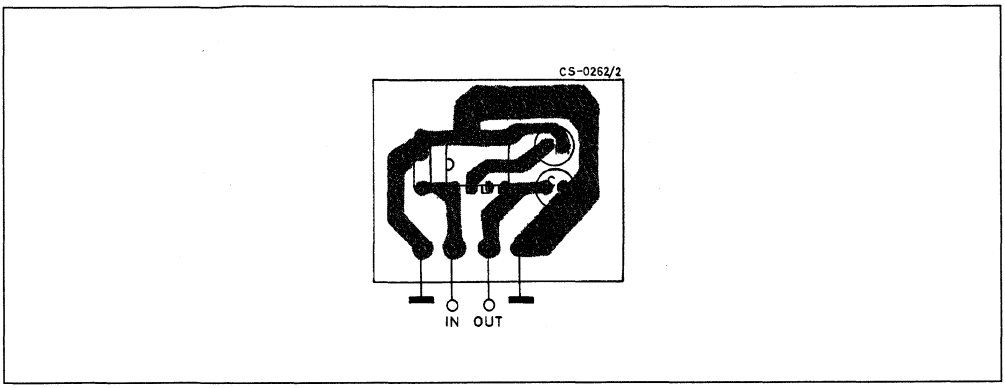


Figure 2 : P.C. Board and Component Layout of Fig. 1 (1 : 1 scale).



PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{I\,MIN} = V_{OUT\,NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.

The series pass element use a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from a REF through the OP2 and Q3, acting as an active zener diode of value V_{REF}.

In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig.3).

The output voltage is fixed to its nominal value:

$$V_{OUT\,NOM} = V_{REF}\left(1 + \frac{R1}{R2}\right) = V_{CFT}\left(1 + \frac{R1}{R2}\right)$$

$\frac{R1}{R2}$ = INTERNALLY FIXED RATIO = 2.4

The ripple rejection is quite high (70 dB) and independent from C_{FT} value.

On the usual voltage regulators, when the input voltage goes below the nominal value, the regulation transistors (series element) saturate bringing the system out of regulation making it very sensible to every variation of the input voltage. On the contrary, a control loop on the L4916 consents to avoid the saturation of the series element by regulating the value of the reference voltage (pin 2). In fact, whenever the input voltage decreases below $V_{I\,MIN}$ the supervisor loop, utilizing a non linear OTA, forces the reference voltage at pin 2 to decrease by discharging C_{FT}. So, during the static mode, when the input voltage goes below V_{MIN} the drop out is kept fixed to about 1.6V. In this condition the device works as a low pass filter in the range (2) of the OTA characteristic. The ripple rejection is externally adjustable acting on C_{FT} as follows :

$$SVR\,(jw) = \left|\frac{V_I\,(jw)}{V_{out}\,(jw)}\right| = \left|1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}}\left(1 + \frac{R1}{R2}\right)}\right|$$

Where:

$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

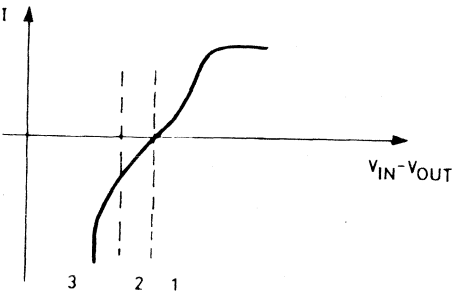
C_{FT} = value of capacitor in F

The reaction time of the supervisor loop is given by the transconductance of the OTA and by C_{FT}. When the value of the ripple voltage is so high and its negative peak is fast enough to determine an istantaneous decrease of the dropout till 1.2 V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharge the capacitor rapidously.

If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection ; the device's again working as a filter (fast transient range).

With C_{FT} = 10 µF; f = 100 Hz a SVR of 35 is obtained.

Figure 3 : Nonliner Transfer Characteristic of the Drop Control Unit.



S-961772

1) Normal operating range (high ripple rejection)
2) Drop controlled range (medium ripple rejection)
3) Fast discharge of C_{FT}

Figure 4 : Supply Voltage Rejection vs. Input Voltage.

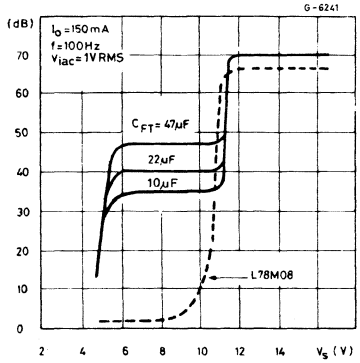


Figure 5 : Supply voltage Rejection vs. Frequency.

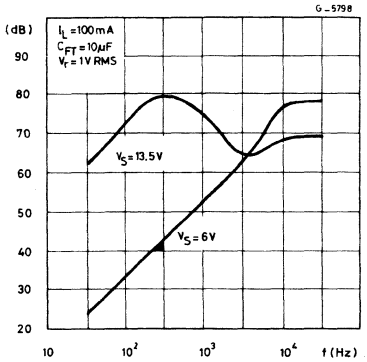


Figure 6 : V_O vs. Supply Voltage.

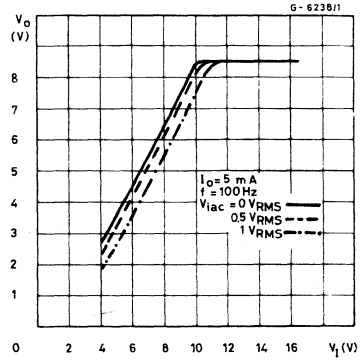


Figure 7 : Quiescent Current vs. Input Voltage.

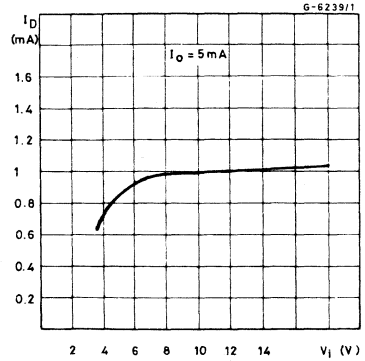


Figure 8 : Dropout vs. Load Current.

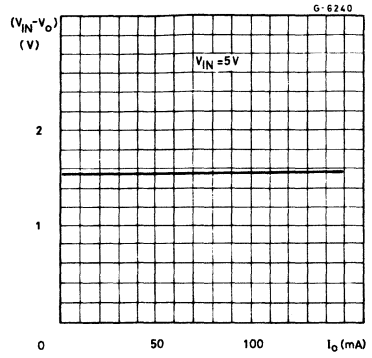
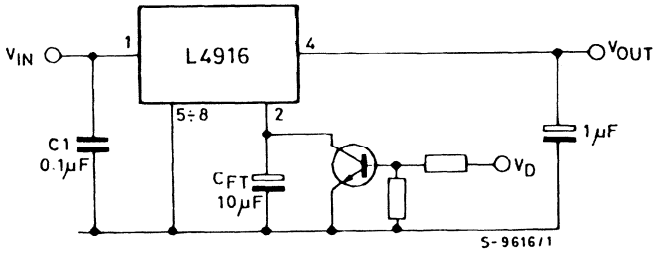


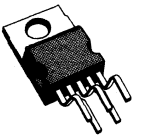
Figure 9 : Inhibit Function Realized on C_{FT} Pin.



VOLTAGE REGULATORS PLUS FILTER

PRELIMINARY DATA

- FIXED OUTPUT VOLTAGE 8.5V
- 250mA OUTPUT CURRENT
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION



PENTAWATT

ORDER CODE : L4918

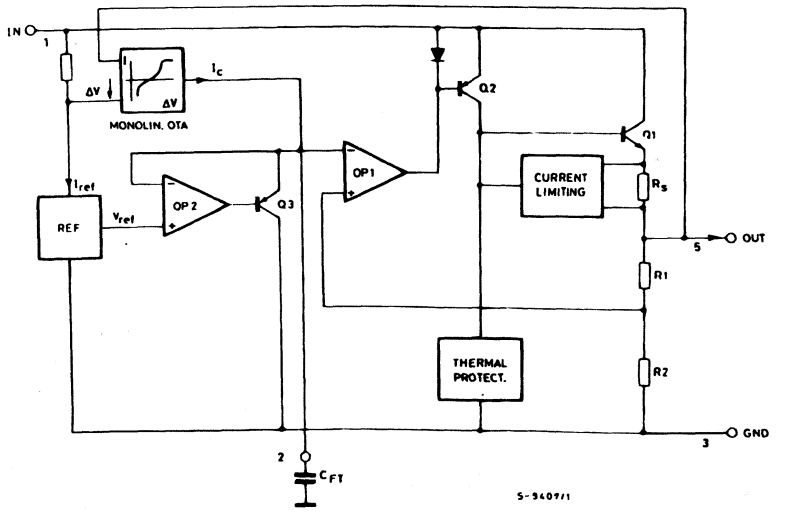
DESCRIPTION

The L4918 combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wider input voltage range.

A supervisor low-pass loop of the element prevents the output transistor from saturation at low input vol tages.

The non linear behaviour of this control circuitry allows a fast setting of the filter.

BLOCK DIAGRAM



PIN CONNECTION (top view)

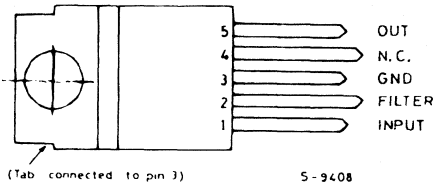
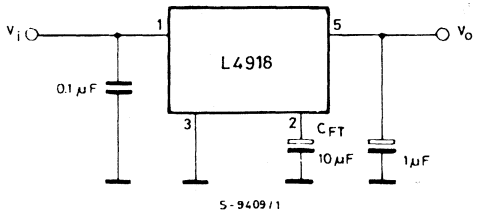


Figure 1 : Application and Test Circuit.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Peak Input Voltage (300ms)	40	V
V_S	DC Voltage	28	V
I_O	Output Current	Internally Limited	
P_{tot}	Power Dissipation	Internally Limited	
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C; V_i = 13.5 V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Input Voltage				20	V
V_O	Output Voltage	V_i = 12 to 18 V I_O = 5 to 150 mA	8.1	8.5	8.9	V
$\Delta V_{I/O}$	Controlled Input-output Dropout Voltage	V_i = 5 to 10 V I_O = 5 to 150 mA		1.6	2.1	V
ΔV_O	Line Regulation	V_i = 12 to 18 V I_O = 10 mA		1	20	mV
ΔV_O	Load Regulation	I_O = 5 to 250 mA t_{on} = 30 µs t_{off} = ≥ 1 ms			100	mV
ΔV_O	Load Regulation	V_i = 8.5 V I_O = 5 to 150 mA t_{on} = 30 µs t_{off} = ≥ 1 ms		100	250	mV
I_q	Quiescent Current	I_O = 5 mA		1.0	2	mA
ΔI_q	Quiescent Current Change	V_i = 6 to 18 V I_O = 5 to 150 mA		0.05		mA
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Drift	I_O = 10 mA		1.2		mV/°C
SVR	Supply Voltage Rejection	V_{iac} = 1 V_{rms} f = 100 Hz I_O = 150 mA V_{IDC} = 12 to 18 V V_{IDC} = 6 to 11 V		71 35(*)		dB dB
I_{SC}	Short Circuit Current		250	300		mA
t_{on}	Switch On Time	I_O = 150 mA V_i = 5 to 11 V V_i = 11 to 18 V		500(*) 300		ms ms
T_{JSD}	Thermal Shut Down			150		°C

(*) Depending of the C_{FT} capacitor

PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{I\,MIN} = V_{OUT\,NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.

The series pass element use a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from a REF through the OP2 and Q3, acting as an active zener diode of value V_{REF}.

In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig.2).

The output voltage is fixed to its nominal value:

$$V_{OUT\,NOM} = V_{REF}\left(1 + \frac{R1}{R2}\right) = V_{CFT}\left(1 + \frac{R1}{R2}\right)$$

$$\frac{R1}{R2} = \text{INTERNALLY FIXED RATIO} = 2.4$$

The ripple rejection is quite high (71 dB) and independent from C_{FT} value.

On the usual voltage regulators, when the input voltage goes below the nominal value, the regulation transistors (series element) saturate bringing the system out of regulation making it very sensible to every variation of the input voltage. Onthe contrary, a control loop on the L4918 consents to avoid the saturation of the series element by regulating the value of the reference voltage (pin 2). In fact, whenever the input voltage decreases below $V_{I\,MIN}$ the supervisor loop, utilizing a non linear OTA, forces the reference voltage at pin 2 to decrease by discharging C_{FT}. So, during the static mode, when the input voltage goes below V_{MIN} the drop out is kept fixed to about 1.6 V. In this condition the device works as a low pass filter in the range (2) of the OTA

characteristic. The ripple rejection is externally adjustable acting on C_{FT} as follows:

$$SVR(jw) = \left| \frac{V_I(jw)}{V_{out}(jw)} \right| = \left| 1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}} \left(1 + \frac{R1}{R_2}\right)} \right|$$

Where:

$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

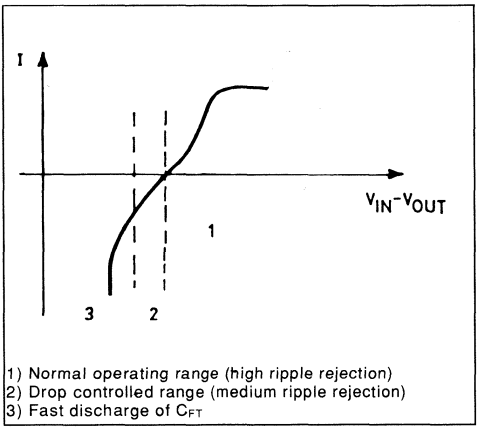
C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the transconductance of the OTA and by C_{FT}. When the value of the ripple voltage is so high and its negative peak is fast/enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharge the capacitor rapidously.

If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection; the device's again working as a filter (fast transient range).

With C_{FT} = 10 μF ; f = 100 Hz a SVR of 35 is obtained.

Figure 2 : Nonliner Transfer Characteristic of the Drop Control Unit.



1) Normal operating range (high ripple rejection)
2) Drop controlled range (medium ripple rejection)
3) Fast discharge of C_{FT}

Figure 3 : Supply Voltage Rejection vs. Frequen-

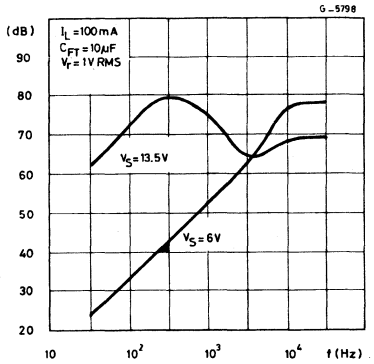


Figure 4 : Supply voltage Rejection vs. Input Voltage.

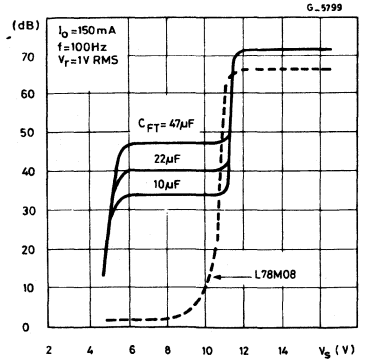
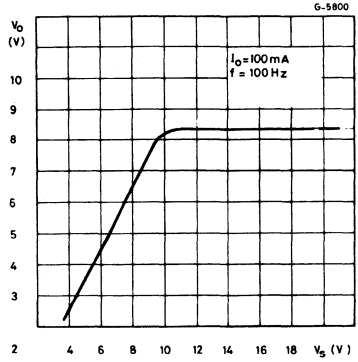


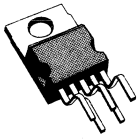
Figure 5 : Output Voltage vs. Input Voltage.



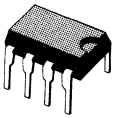
VERY LOW DROP ADJUSTABLE REGULATORS

ADVANCE DATA

- VERY LOW DROP VOLTAGE
- ADJUSTABLE OUTPUT VOLTAGE FROM 1.25V TO 20V
- 400mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- REVERSE VOLTAGE PROTECTION
- + 60/ – 60V TRANSIENT PEAK VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION WITH FOLD-BACK CHARACTERISTICS
- THERMAL SHUT-DOWN



Pentawatt



Minidip (4 + 4)

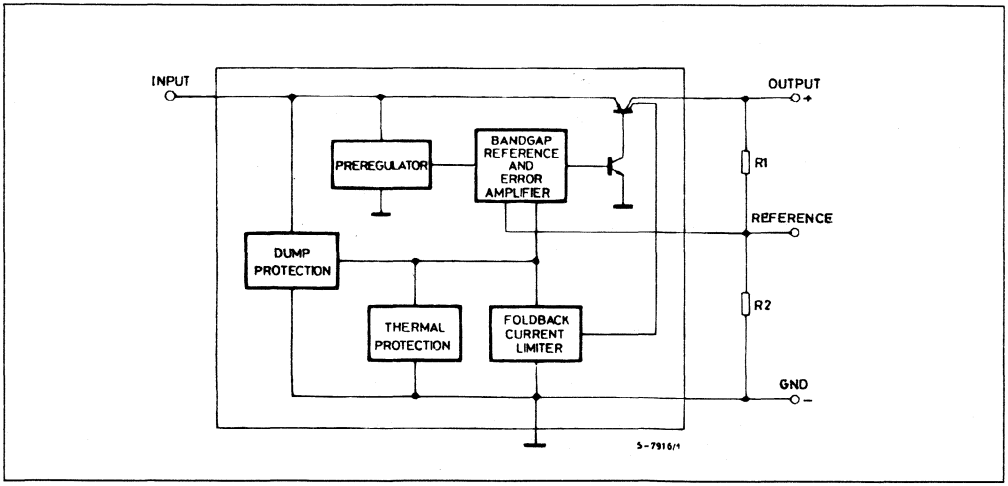
ORDER CODES : L4920 (Pentawatt)
L4921 (Minidip)

DESCRIPTION

The L4920 and L4921 are adjustable voltage regulators with a very low voltage drop (0.4V typ. at 0.4A T_j = 25°C), low quiescent current and comprehensive on-chip protection.
These devices are protected against load dump and field decay transients, polarity reversal and over heating.
A foldback current limiter protects against load short circuits.
The output voltage is adjustable through an external divider from 1.25V to 20V. The minimum operating input voltage is 5.2V (T_J = 25°C).

These regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.
In battery backup and standby applications the low consumption of these devices extends battery life.

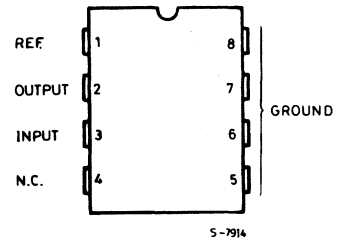
BLOCK DIAGRAM

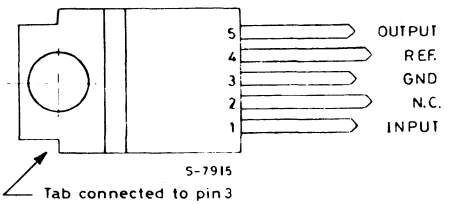


ABSOLUTE MAXIMUM RATINGS

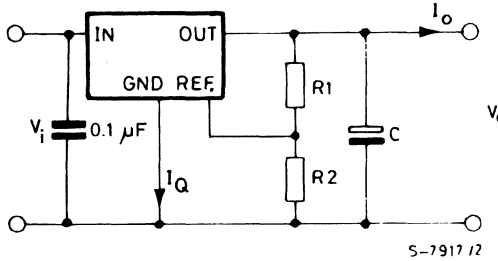
Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	35	
	DC Reverse Input Voltage	- 18	V
	Transient Input Overvoltages :	60	V
	Load Dump :		V
	5ms ≤ t_{rise} ≤ 10ms		
	τ_f Fall Time Constant = 100ms		
	R_{SOURCE} ≥ 0.5Ω		
	Field Decay :	- 60	V
	5ms ≤ t_{fall} ≤ 10ms, R_{SOURCE} ≥ 10Ω		
	τ_r Rise Time Constant = 33ms		
T_J, T_{STG}	Junction and Storage Temperature Range	- 55 to 150	°C

PIN CONNECTIONS (top view)





TEST AND APPLICATION CIRCUIT



C = 100µF is required for stability (ESR ≤ 3Ω over T range)
R2 = 6.2KΩ.

THERMAL DATA

			Minidip (4 + 4)	Pentawatt	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	60	°C/W
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	15		°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max		3.5	°C/W

ELECTRICAL CHARACTERISTICS (for V_I = 14.4V, T_j = 25°C, V_o = 5V, C_o = 100µF, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Operating Input Voltage	$V_o \geq 4.5V$ I_o = 400mA	V_o + 0.7		26	V
		$V_{REF} \leq V_o < 4.5V$ I_o = 400mA	5.2		26	V
V_{REF}	Reference Voltage	5.2V < V_i < 26V 5mA ≤ I_o ≤ 400mA (*)	1.20	1.25	1.30	V
ΔV_o	Line Regulation	V_o + 1V < V_i < 26V $V_o \geq 4.5V$ I_o = 5mA		1	10	mV/V
ΔV_o	Load Regulation	5mA ≤ I_o ≤ 400mA (*) $V_o \geq 4.5V$		3	15	mV/V
V_D	Dropout Voltage	I_o = 10mA I_o = 150mA I_o = 400mA		0.05 0.2 0.4	 0.4 0.7	V V V
I_Q	Quiescent Current	I_o = 0mA V_o + 1V < V_i < 26V		0.8	2	mA
		I_o = 400mA (*) V_o + 1V < V_i < 26V		65	90	mA
I_o	Maximal Output Current			800		mA
I_{OSC}	Short Circuit Output Current (*)			350	500	mA

(*) Foldback protection.

ELECTRICAL CHARACTERISTICS (for V_I = 14.4V ; – 40 ≤ T_j ≤ 125°C (note 1), V_o = 5V ; C_o = 100µF, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Operating Input Voltage	$V_o \geq 4.5V$ I_o = 400mA	V_o + 0.9		26	V
		$V_{REF} \leq V_o < 4.5V$ I_o = 400mA	5.4		26	V
V_{REF}	Reference Voltage	5.4V < V_i < 26V	1.17	1.25	1.33	V
ΔV_o	Line Regulation	V_o + 1.2V < V_i < 26V $V_o \geq 4.5V$ I_o = 5mA		2	15	mV/V
ΔV_o	Load Regulation	5mA ≤ I_o ≤ 400mA (*) $V_o \geq 4.5V$		5	25	mV/V
V_D	Dropout Voltage	 I_o = 150mA I_o = 400mA		 0.25 0.5	 0.5 0.9	V V V
I_Q	Quiescent Current	I_o = 0mA V_o + 1.2V < V_i < 26V		1.2	3	mA
		I_o = 400mA (*) V_o + 1.2V < V_i < 26V		80	140	mA
I_o	Maximal Output Current			870		mA
I_{OSC}	Short Circuit Output Current (*)			230		mA

(*) Foldback protection.

Note : 1. Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Figure 1 : Output Voltage vs. Temperature.

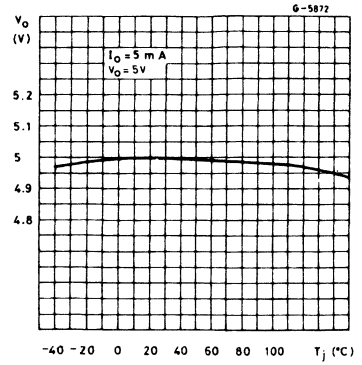


Figure 2 : Foldback Current Limiting.

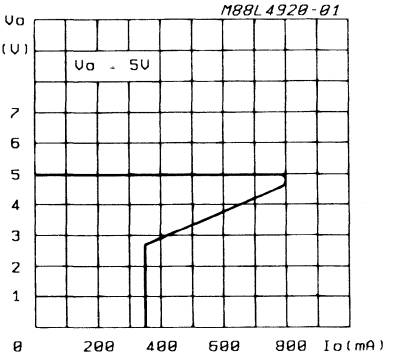
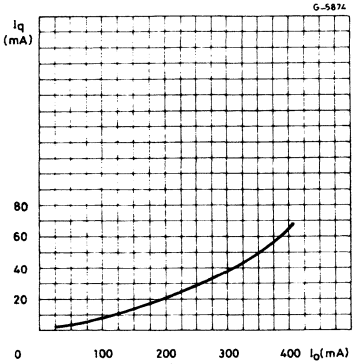


Figure 3 : Quiescent Current vs. Output Current (V_o = 5V).



APPLICATION INFORMATION

1) The L4920 and L4921 have $V_{REF} \cong 1.25V$. Then the output voltage can be set down to V_{REF} but V_i must be greater than 5.2V (T_j = 25°C).
2) As the regulator reference voltage source works in closed loop, the reference voltage may change in foldback condition.
3) For applications with high V_I, the total power dissipation of the device with respect to the thermal resistance of the package may be limiting . The total power dissipation is :

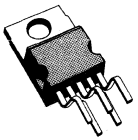
$$P_{tot} = V_i I_q + (V_i - V_o) I_o$$

A typical curve giving the quiescent current I_q as a function of the output current I_o is shown in fig. 3.

5V–1A VERY LOW DROP REGULATOR WITH RESET

ADVANCE DATA

- VERY LOW DROP (max. 0.9V at 1A) OVER FULL OPERATING TEMPERATURE RANGE ($-40 \leq T_J \leq 125°C$)
- LOW QUIESCENT CURRENT (max 70mA at 1A) OVER FULL T RANGE
- PRECISE OUTPUT VOLTAGE (5V ± 4%) OVER FULL T RANGE
- POWER ON-OFF INFORMATION WITH SET-TABLE DELAY
- LOAD DUMP AND REVERSE BATTERY PRO-TECTION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN



Pentawatt

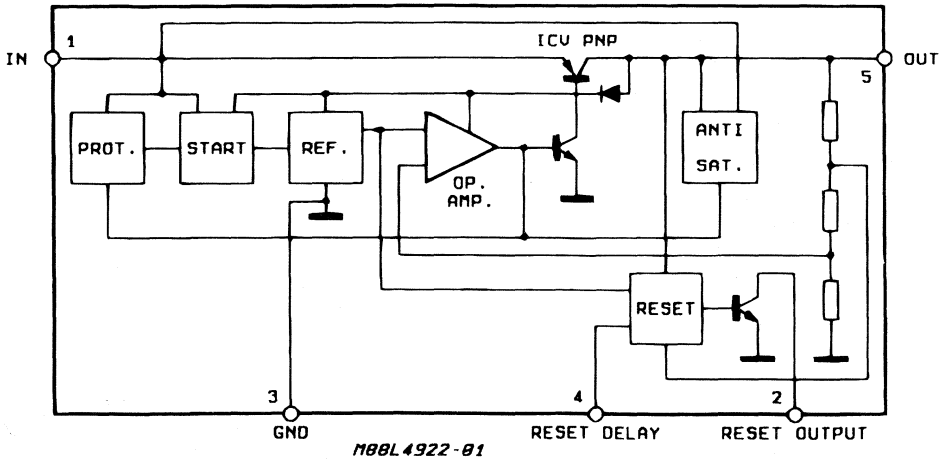
ORDER CODE : L4922

DESCRIPTION

The L4922 is a high current monolithic voltage regulator with very low voltage drop (0.70V max at 1A, $T_J = 25°C$).

The device is internally protected against load dumps transient of + 60V, reverse polarity, overheating and output short circuit : thanks to these features the L4922 is very suited for the automotive and industrial applications.

BLOCK DIAGRAM



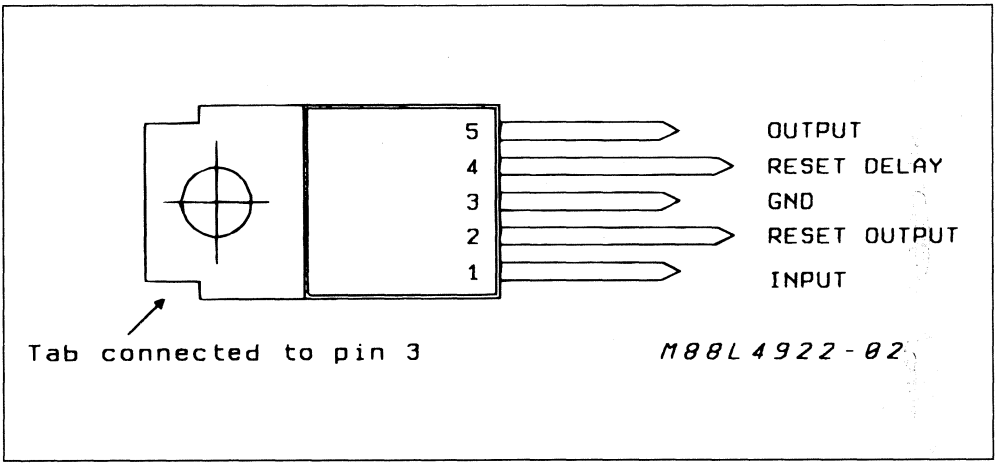
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage DC Reverse Voltage Transient Input Overvoltage : Load Dump : 5ms ≤ t_{rise} ≤ 10ms, τ_f Fall Time Constant = 100ms, R_{source} ≥ 0.5Ω	35 - 18 60	V V V
T_J, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3.5	°C/W

PIN CONNECTION (top view)



FUNCTIONAL DESCRIPTION

The operating principle of the voltage regulator is based on the reference, the error amplifier, the driver and the power PNP. This stage uses an Isolated Collector Vertical PNP transistor which allows to obtain very low dropout voltage (typ. 450mV) and low quiescent current (I_Q = 20mA typically at I_o = 1A).

Thanks to these features the device is particularly suited when the power dissipation must be limited as, for example, in automotive or industrial applications supplied by battery.

The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (Co_{min} = 47µF) to guarantee the global stability of the system.

The antisaturation circuit allows to reduce drastically the supply current peak which takes place during the start up.

The reset function is LOW when the output voltage level is lower than the reset threshold voltage V_{RthOFF} (typ. value : V_o – 150mV). When the output voltage is higher than V_{RthON} the reset becomes HIGH after a delay time settable with the external capacitor C_d. Typically t_d = 20ms, C_d = 0.1µF. The reset and delay threshold hysteresis improve the noise immunity allowing to avoid false switchings. The typical reset output waveform is shown in fig. 1.

ELECTRICAL CHARACTERISTICS (V_I = 14. 4V, – 40°C ≤ T_J ≤ + 125°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Operating Input Voltage	(*) note 1	6		26	V
V_O	Output Voltage	I_O = 10mA to 1A	4.8		5.2	V
ΔV_{Line}	Line Regulation	V_i = 6 to 26V		5	25	mV
SVR	Supply Voltage Rejection	I_O = 700mA f = 120Hz C_O = 47µF V_i = $12V_{dc}$ + $5V_{pp}$		55		dB
ΔV_{LOAD}	Load Regulation	I_O = 10mA to 1A		15	50	mV
$V_i - V_o$	Dropout Voltage	T_J = 25°C, I_O = 1A Over Full T, I_O = 1A		0.45	0.70 0.90	V V
I_q	Quiescent Current	I_O = 10mA I_O = 1A		7 25	12 70	mA mA
I_{SC}	Short Circuit Current			1.8		A
V_R	Reset Output Saturation Voltage	I_R = 16mA V_O ≤ 4.75V			0.8	V
I_R	Reset Output Leakage Current (high level)	V_O in Regul.			50	µA
t_D	Reset Pulse Delay Time	C_D = 100nF		20		ms
V_{RthOFF}	Power OFF V_O Threshold	V_O @ Reset out H to L Transition	4.75	V_O – 0.15		V
I_{CD}	Delay Capacitor Charging Current (current generator)	V_4 = 3V		20		µA
V_{RthON}	Power ON V_O Threshold	V_O @ Reset out L to H Transition		V_{RthOFF} + 0.03V	V_O – 0.04V	V
V_4	Delay Comparator Threshold	Reset out = "1" H to L Transition Reset out = "0" L to H Transition	3.2 3.7	 4	3.8 4.4	V V
V_{4H}	Delay Comparator Hysteresis			500		mV

(*) Note 1 : The device is not operating within the range : 26V < V_i < 35V.

Figure 1 : Typical Reset Output Waveform.

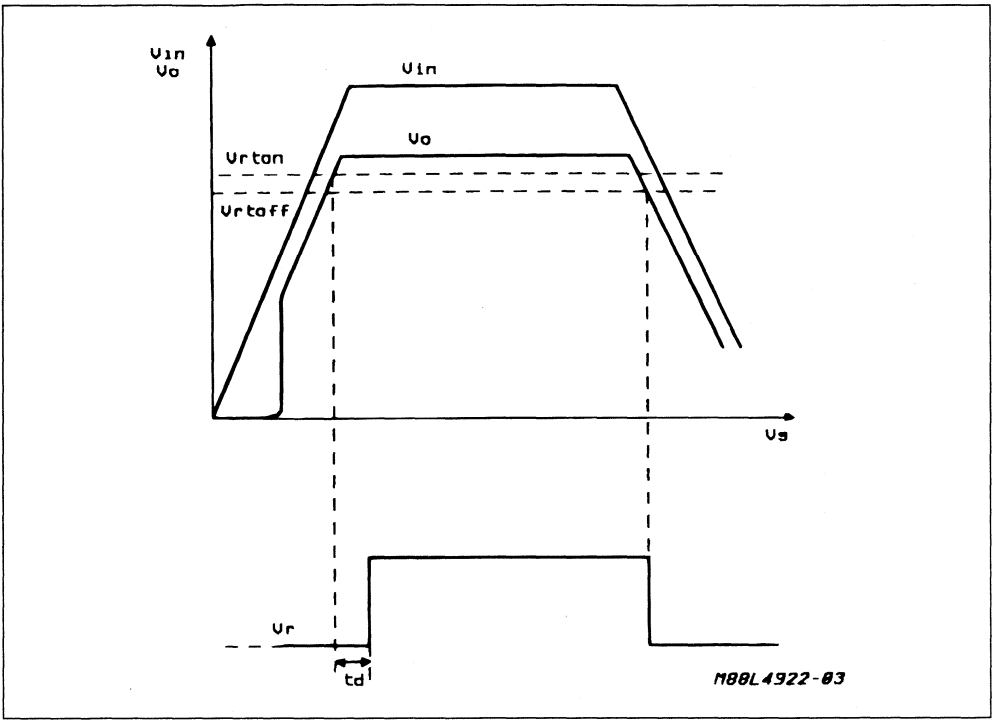
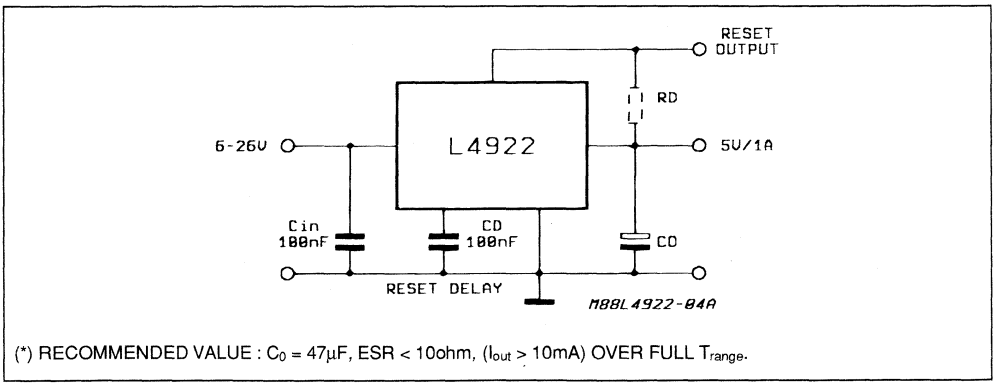


Figure 2 : Typical Application Circuit.



(*) RECOMMENDED VALUE : C_O = 47µF, ESR < 10ohm, (I_{out} > 10mA) OVER FULL T_{range}.

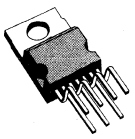
SGS-THOMSON MICROELECTRONICS

L4923

5V–1A VERY LOW DROP REGULATOR WITH RESET AND INHIBIT

ADVANCE DATA

- VERY LOW DROP (max. 0.9V at 1A) OVER FULL OPERATING TEMPERATURE RANGE ($-40 \leq T_J \leq 125°C$)
- LOW QUIESCENT CURRENT (max 70mA at 1A) OVER FULL T RANGE
- PRECISE OUTPUT VOLTAGE (5V ± 4%) OVER FULL T RANGE
- POWER ON-OFF INFORMATION WITH SETTABLE DELAY
- INHIBIT FOR REMOTE ON-OFF COMMAND (active high)
- LOW STANDBY CURRENT
- LOAD DUMP AND REVERSE BATTERY PROTECTION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN



Heptawatt

ORDER CODE : L4923

DESCRIPTION

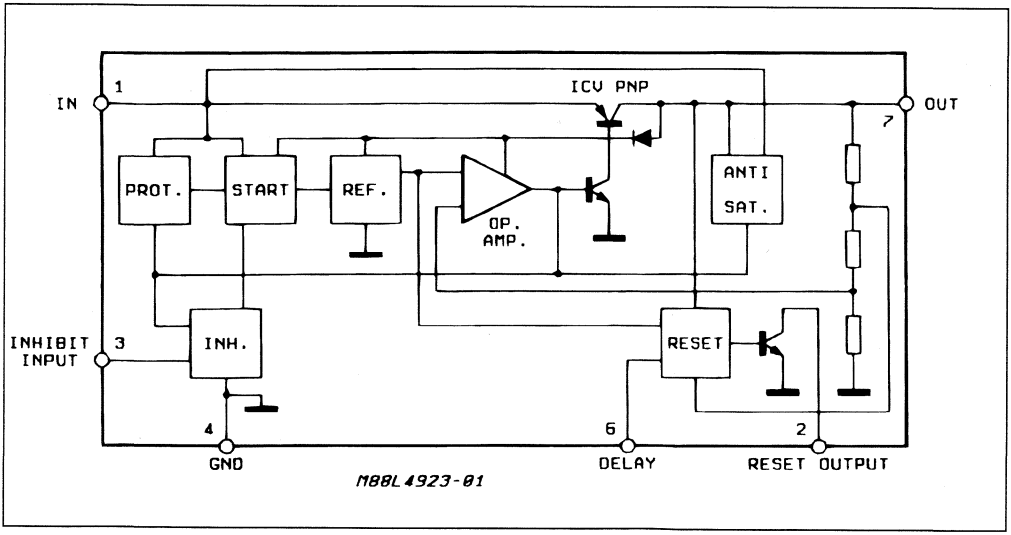
The L4923 is a high current monolithic voltage regulator with very low voltage drop (0.70V max at 1A, $T_J = 25°C$).

The device is internally protected against load dump transient of + 60V, reverse polarity, overheating and output short circuit : thanks to these features the L4923 is very suited for the automotive and industrial applications.

The reset function is very useful for power off and power on information when supplying a microprocessor.

The inhibit function reduces drastically the consumption when no load current is required : typically the standby current value is 300µA.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage DC Reverse Voltage Transient Input Overvoltage : Load Dump : 5ms ≤ trise ≤ 10ms, τ_f Fall Time Constant = 100ms, Rsource ≥ 0.5Ω	35 - 18 60	V V V
T_J, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3.5	°C/W

PIN CONNECTION (top view)

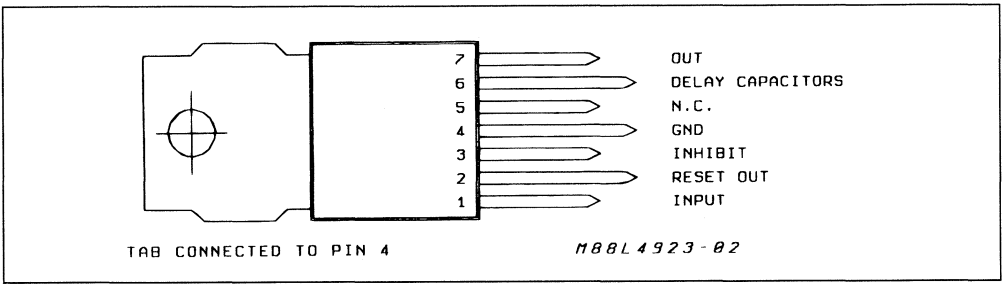
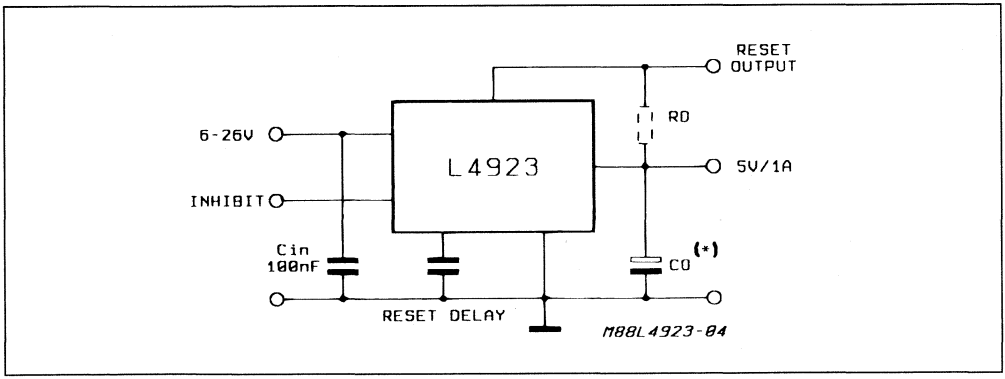


Figure 1 : Application Circuit.



(*) RECOMMENDED VALUE : C_O = 47µF, ESR < 10Ω, (I_{out} > 10mA) OVER FULL T_{range}.

ELECTRICAL CHARACTERISTICS (V_i = 14. 4V, – 40°C ≤ T_J ≤ + 125°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Operating Input Voltage	(*) Note 1	6		26	V
V_o	Output Voltage	I_o = 10mA to 1A	4.8		5.2	V
ΔV_{Line}	Line Regulation	V_i = 6 to 26V		5	25	mV
SVR	Supply Voltage Rejection	I_o = 700mA f = 120Hz C_o = 47µF $V_i = 12V_{dc} + 5V_{pp}$		55		dB
ΔV_{LOAD}	Load Regulation	I_o = 10mA to 1A		15	50	mV
$V_i - V_o$	Dropout Voltage	T_J = 25°C, I_O = 1A		0.45	0.70	V
		Over Full T, I_o = 1A			0.90	V
I_q	Quiescent Current	I_o = 10mA I_o = 1A Active High Inhibit		7 25 0.30	12 70 0.65	mA mA mA
I_{SC}	Short Circuit Current			1.8		A
V_R	Reset Output Saturation Voltage	I_R = 16mA $V_o \leq$ 4.75V			0.8	V
I_R	Reset Output Leakage Current (high level)	V_o in Regul.			50	µA
t_D	Reset Pulse Delay Time	C_D = 100nF		20		ms
V_{RthOFF}	Power OFF V_o Threshold	V_o @ Reset out H to L Transition	4.75	V_o – 0.15		V
I_{C6}	Delay Capacitor Charging Current (current generator)	V_6 = 3V		20		µA
V_{RthON}	Power ON V_o Threshold	V_o @ Reset out L to H Transition		V_{rthOFF} + 0.03V	V_o – 0.04V	V
V_6	Delay Comparator Threshold	Reset out = "1" H to L Transition	3.2		3.8	V
		Reset out = "0" L to H Transition	3.7	4	4.4	V
V_{6H}	Delay Comparator Hysteresis			500		mV
V_{InhL}	Low Inhibit Voltage				0.8	V
V_{InhH}	High Inhibit Voltage		2.0			V
I_{InhL}	Low Level Inhibit Current	$V_{Inh\ L}$ = 0.4V	– 40	– 10		µA
I_{InhH}	High Level Inhibit Current	$V_{Inh\ H}$ = 2.4V		6	20	µA

(*) Note 1 : The device is not operating within the range : 26V < V_i < 35V.

FUNCTIONAL DESCRIPTION

The operating principle of the voltage regulator is based on the reference, the error amplifier, the driver and the power PNP. This stage uses an Isolated Collector Vertical PNP transistor which allows to obtain very low dropout voltage (typ. 450mV) and low quiescent current (I_Q = 20mA typically at I_O = 1A).

Thanks to these features the device is particularly suited when the power dissipation must be limited as, for example, in automotive or industrial applications supplied by battery.

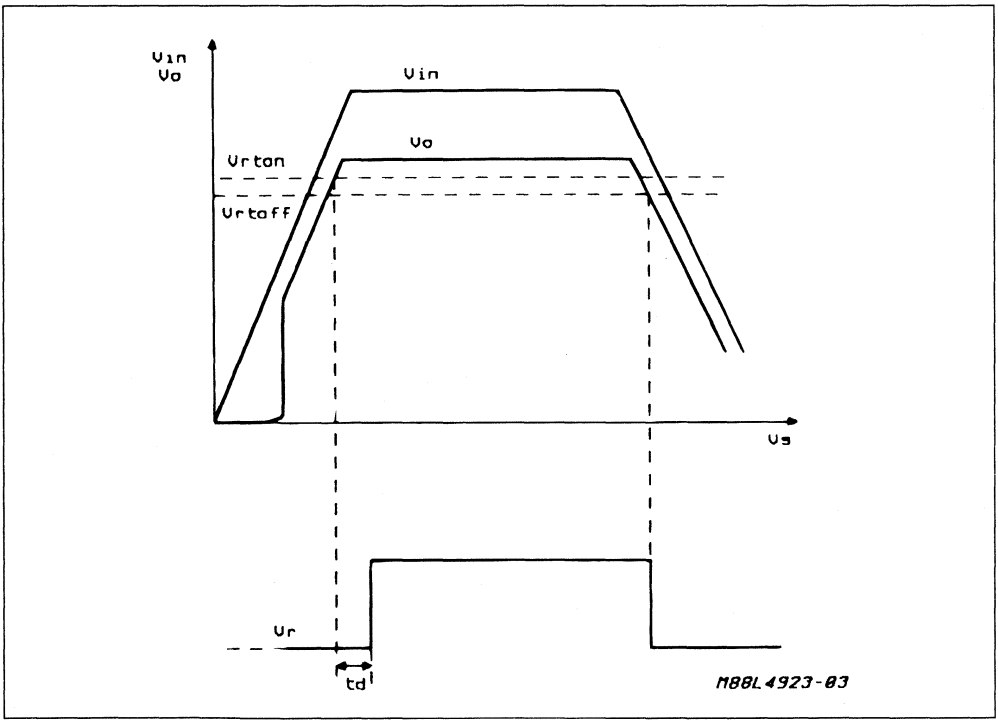
The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (C_O = 47µF) to guarantee the global stability of the system.

The antisaturation circuit allows to reduce drastically the supply current peak which takes place during the start up.

The reset function is LOW when the output voltage level is lower than the reset threshold voltage V_{RthOFF} (typ. value : V_O - 150mV). When the output voltage is higher than V_{RthON} the reset becomes HIGH after a delay time settable with the external capacitor C_d. Typically t_d = 20ms, C_d = 0.1µF. The reset and delay threshold hysteresis improve the noise immunity allowing to avoid false switchings. The typical reset output waveform is shown in fig. 2.

The inhibit circuit accepts standard TTL input levels : this block switches off the voltage regulator when the input signal is HIGH and switches on it when the input signal is LOW. Thanks to inhibit function the consumption is drastically reduced (650µA max) when no load current is required.

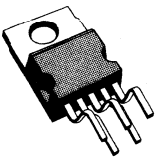
Figure 2 : Typical Reset Output Waveform.



5V VERY LOW DROP VOLTAGE REGULATOR

ADVANCE DATA

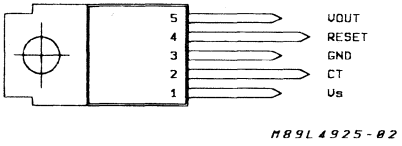
- OUTPUT VOLTAGE PRECISION 5V ± 2%
- VERY LOW QUIESCENT CURRENT, LESS THAN 250µA
- OUTPUT CURRENT : I_O = 500mA
- VERY LOW DROPOUT (max 0.6V)
- OPERATING TRANSIENT SUPPLY VOLTAGE UP TO 40V
- POWER-ON RESET CIRCUIT SENSING THE OUTPUT VOLTAGE
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS



PENTAWATT

ORDER CODES : L4925H (Horizontal version)
L4925 (Vertical version)

PIN CONNECTION



DESCRIPTION

The L4925 is a monolithic integrated voltage regulator with a very low dropout output and additional functions such as power-on reset and programmable reset delay-time. It is designed for supplying microcomputer controlled systems specially in automotive applications.

ABSOLUTE MAXIMUM RATINGS

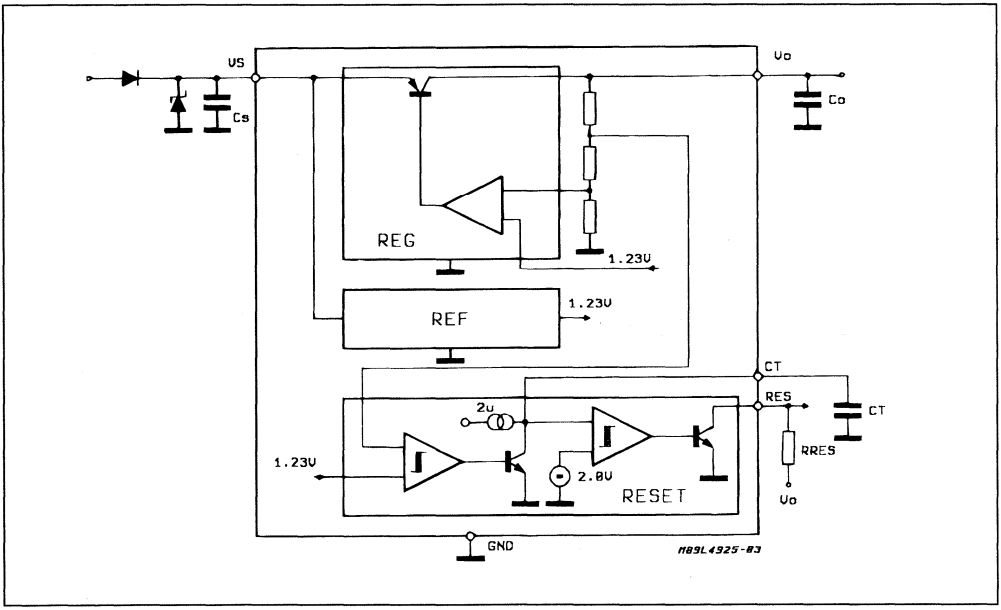
Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage Transient Supply Overvoltages : Load Dump : 5ms ≤ t_{rise} ≤ 10ms τ_f Fall Time Constant = 100ms R_{SOURCE} ≥ 0.5Ω	28 40	V V
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to + 150	°C
V_{RES}	Reset Voltage	20	V
I_{RES}	Reset Current	5	mA

Note : The circuit is ESD protected according to MIL-STD-883C.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3.5	°C/W

APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS(V_S = 14V ; – 40°C ≤ T_j 125°C unless otherwise specified).

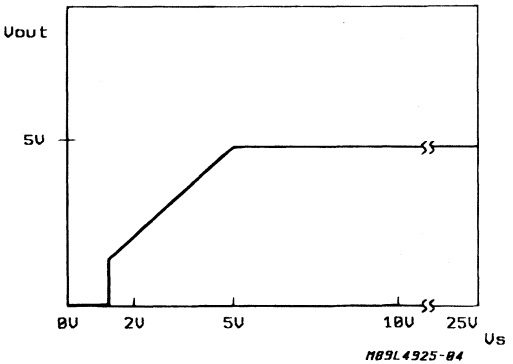
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_j = 25°C ; I_O = 1mA	4.95	5.00	5.05	V
V_O	Output Voltage	6V < V_{IN} < 25V 1mA < I_O < 500mA	4.90	5.00	5.10	V
V_{DP}	Dropout Voltage	I_O = 100mA I_O = 500mA		0.2 0.3	0.3 0.6	V V
V_{IO}	Input to Output Voltage Difference in Undervoltage Condition	V_{IN} = 4V, I_O = 350mA			0.6	V
V_{OL}	Line Regulation	6V < V_{IN} < 25V I_O = 1mA			20	mV
V_{OLO}	Load Regulation	5mA < I_O < 500mA			50	mV
I_{LIM}	Current Limit	V_O = 4.5V (note 1)	550	1000	1500	mA
I_{QSB}	Quiescent Current	I_O = 0.3mA ; T_j < 100°C		140	250	µA
I_Q	Quiescent Current	I_O = 500mA			20	mA

RESET

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset Threshold Voltage		4.5	4.7	4.9	V
V_{RTH}	Reset Threshold Hysteresis		50	100	200	mV
t_{RD}	Reset Pulse Delay	C_T = 100nF ; t_R > 100µs	60	100	140	ms
t_{RR}	Reset Reaction Time	C_T = 100nF	1	10	50	µs
V_{RL}	Reset Output LOW Voltage	R_{RES} = 10KΩ to V_O V_S ≥ 2V			0.4	V
$I_{L\,RES}$	Reset Output HIGH Leakage	V_{RES} = 5V			1	µA
V_{CTth}	Delay Comparator Threshold			2.0		V
$V_{CTth,\,hy}$	Delay Comparator Threshold Hysteresis			100		mV

Note : 1. Foldback characteristic.

Figure 1 : Output Voltage vs. Input Voltage.



FUNCTIONAL DESCRIPTION

The L4925 is based on the SGS-THOMSON Microelectronics modular voltage regulator approach. Several outstanding features and auxiliary functions are provided to meet the requirements of supplying the microprocessor systems used in automotive applications.

OUTPUT VOLTAGE REGULATOR

The output voltage regulator uses an Isolated Collector Vertical PNP transistor as a regulating element. This structure allows a very low dropout voltage at currents up to 500mA. The dropout operation of the output regulator is maintained down to 2V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. This feature avoids functional interruptions which could be generated by overvoltage pulses.

The typical curve of this output voltage as a function of the input supply voltage is shown in fig. 1.

The current consumption of the device (quiescent current) is less than 250µA. The dropout voltage is controlled to reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region.

The quiescent current is shown in fig. 2 as a function of the supply input voltage.

RESET CIRCUIT

The block circuit diagram of the reset circuit is shown in fig. 3. The reset circuit supervises the output voltage. The reset threshold of 4.7V is defined by the internal reference voltage.

The reset pulse delay time t_{RD}, is defined by the charge time of an external capacitor C_T :

$$t_{RD} = \frac{C_T - 2V}{2\mu A}$$

The reaction time of the reset circuit depends on the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T.

The reaction time of the reset circuit increases the noise immunity.

In fact, if the standby output voltage drops below the reset threshold for a time shorter than the reaction time t_{RR}, no reset output variation occurs. The nominal reset delay is generated for standby output voltage drops longer than the time necessary for the complete discharging of the capacitor C_T. This time is typically equal to 50µs if C_T = 100nF. The typical reset output waveforms are shown in fig. 4.

Figure 2 : Quiescent Current vs. Supply Voltage.

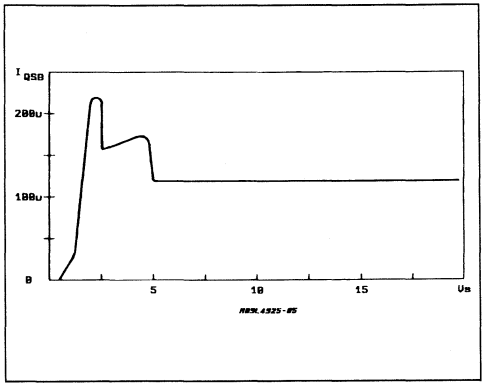


Figure 3 : Block Diagram of the Reset Circuit.

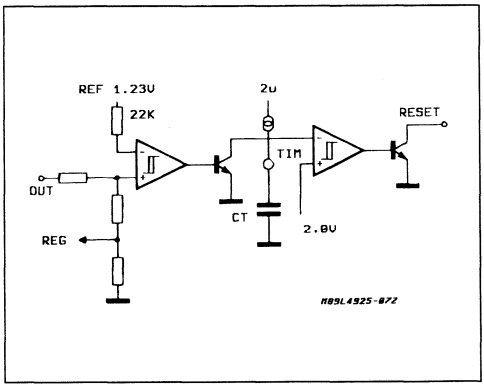
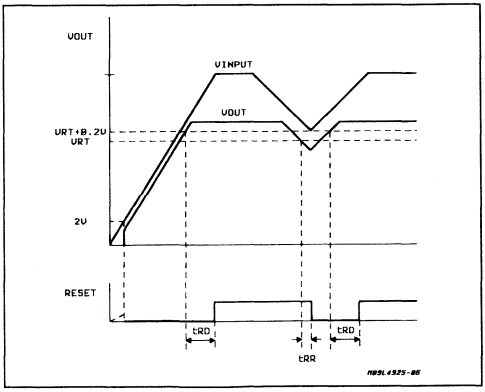


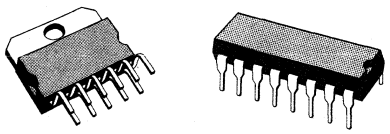
Figure 4 : Typical Reset Output Waveforms.



DUAL MULTIFUNCTION VOLTAGE REGULATOR

ADVANCE DATA

- STANDBY OUTPUT VOLTAGE PRECISION 5V ± 2%
- OUTPUT 2 TRACKED TO THE STANDBY OUTPUT
- OUTPUT 2 DISABLE FUNCTION FOR STANDBY MODE
- VERY LOW QUIESCENT CURRENT, LESS THAN 250μA, IN STANDBY MODE
- OUTPUT 2 VOLTAGE SETTABLE FROM 5 TO 20V
- OUTPUT CURRENTS : I_{O1} = 50mA, I_{O2} = 500mA
- VERY LOW DROPOUT (max 0.4V/0.6V)
- OPERATING TRANSIENT SUPPLY VOLTAGE UP TO 40V
- PROGRAMMABLE RESET THRESHOLD
- POWER-ON RESET CIRCUIT SENSING THE STANDBY OUTPUT VOLTAGE
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- EARLY WARNING OUTPUT FOR SUPPLY UNDERVOLTAGE
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS



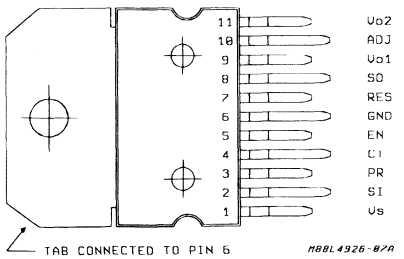
Multiwatt 11 **Powerdip** (12+2+2)

ORDER CODES : L4926 (Multiwatt–11)
L4928 (Powerdip 12+2+2)

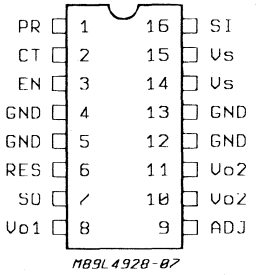
DESCRIPTION

The L4926/28 are monolithic integrated dual voltage regulators with two very low dropout outputs and additional functions such as power-on reset and input voltage sense. They are designed for supplying microcomputer controlled systems specially in automotive applications.

PIN CONNECTIONS (top view)

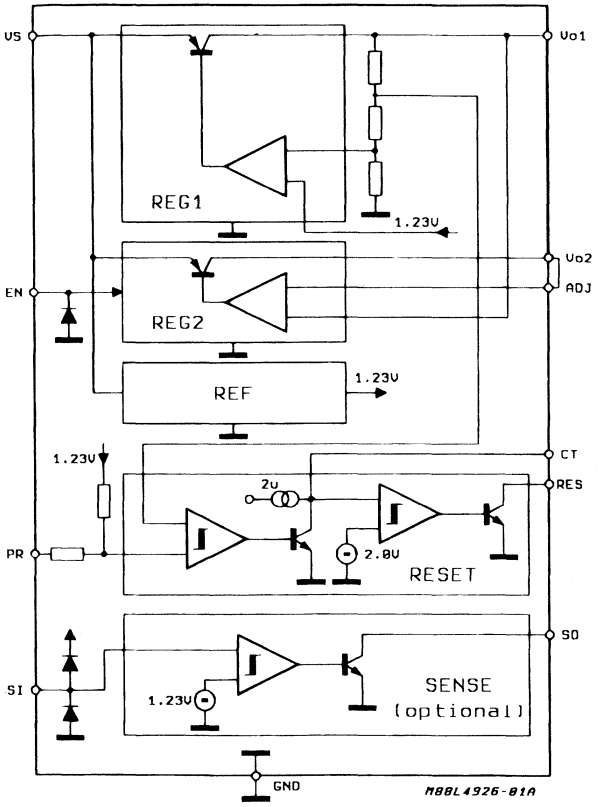


(Multiwatt–11)



(Powerdip 12+2+2)

BLOCK DIAGRAM



THERMAL DATA

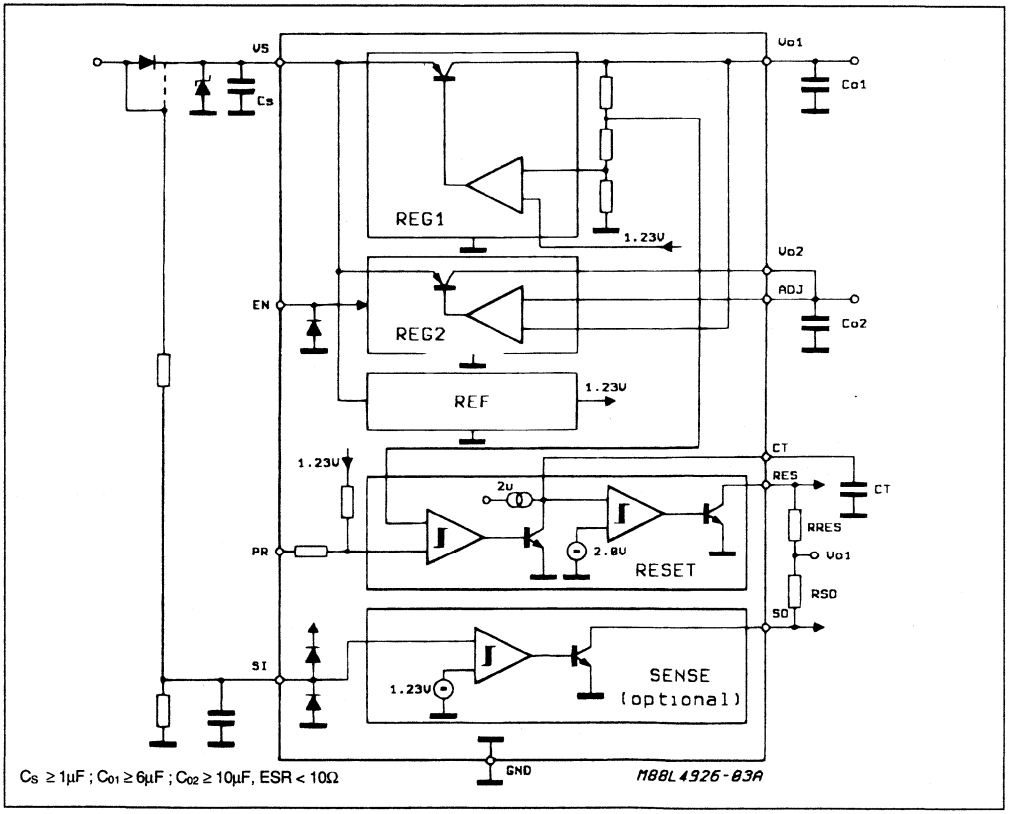
$R_{th\ j\text{-}c}$	Thermal Resistance Junction - case (MW11)	Max	3	°C/W
$R_{th\ J\text{-}A}$	Thermal Resistance Junction Ambient (power DIP 12 + 2 + 2)		80	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	DC Supply Voltage Transient Supply Overvoltages : Load Dump : 5ms ≤ t_{rise} ≤ 10ms τ_f Fall Time Constant = 100ms R_{SOURCE} ≥ 0.5Ω	28 40	V V
I_{SI}	Sense Input Current (V_{SI} < – 0.3V or V_{SI} > V_s	± 1	mA
I_{EN}	Enable Input Current (V_{EN} < – 0.3V)	– 1	mA
V_{EN}	Enable Input Voltage	V_s	mA
V_{RES}, V_{SO}	Reset and Sense Output Voltage	20	V
I_{RES}, I_{SO}	Reset and Sense Output Current	5	mA
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C
P_D	Power Dissipation (T_A = 80°C, $T_{th\ heatsink}$ = 90°C/W) MW11 Power DIP 12 + 2 + 2	5 875	W mW

Note : The circuit is ESD protected according to MIL–STD–883C.

APPLICATION CIRCUIT



C_S ≥ 1µF ; C_{O1} ≥ 6µF ; C_{O2} ≥ 10µF, ESR < 10Ω

ELECTRICAL CHARACTERISTICS (V_S = 14V ; – 40°C ≤ T_J ≤ 125°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage				25	V
V_{O1}	Standby Output Voltage	T_J = 25°C ; I_{O1} = 1mA	4.95	5.00	5.05	V
V_{O1}	Standby Output Voltage	6V ≤ V_S ≤ 25V 1mA ≤ I_{O1} ≤ 50mA	4.90	5.00	5.10	V
V_{O2} - V_{O1}	Output Voltage 2 Tracking Error (note 1)	6V ≤ V_S≤ 25V 5mA ≤ I_{O2} ≤ 500mA Enable = LOW	– 25		+ 25	mV
I_{ADJ}	ADJ Input Current	I_{O1} = 1mA ; I_{O2} = 5mA	– 1	0.1	1	µA
V_{DP1}	Dropout Voltage 1	I_{O1} = 10mA I_{O1} = 50mA		0.1 0.2	0.2 0.4	V V
V_{IO1}	Input to Output Voltage Difference in Undervoltage Condition	V_S = 4V, I_{O1} = 35mA			0.4	V
V_{DP2}	Dropout Voltage 2	I_{O2} = 100mA I_{O2} = 500mA		0.2 0.3	0.3 0.6	V V
V_{IO2}	Input to Output Voltage Difference in Undervoltage Condition	V_S = 4V, I_{O2} = 350mA			0.6	V
$V_{OL\ 1.2}$	Line Regulation	6V ≤ V_S ≤ 25V I_{O1} = 1mA, I_{O2} = 5mA			20	mV
V_{OLO1}	Load Regulation 1	1mA ≤ I_{O1} ≤ 50mA			25	mV
V_{OLO2}	Load Regulation 2	5mA ≤ I_{O2} ≤ 500mA			50	mV
I_{LIM1}	Current Limit 1	V_{O1} = 4.5V V_{O1} = 0V (note 2)	55 20	100 40	200 80	mA mA
I_{LIM2}	Current Limit 2	V_{O2} = 0V	550	1000	1500	mA
I_{QSB}	Quiescent Current Standby Mode (output 2 disabled)	I_{O1} = 0.3mA ; T_J < 100°C V_{EN} ≥ 2.4V PR Open PR Grounded		 140 155	 250 280	 µA µA
I_Q	Quiescent Current	I_{O1} = 50mA I_{O2} = 500mA			20	mA

ENABLE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ENL}	Enable Input LOW Voltage (output 2 active)		– 0.3		1.5	V
V_{ENH}	Enable Input HIGH Voltage		2.4		7	V
V_{ENhyst}	Enable Hysteresis		30	75	200	mV
I_{EN}	Enable Input Current	0V < V_{EN} < 1.2V 2.5V < V_{EN} < 7V	– 10 – 1	– 1.5 0	– 0.5 + 1	µA µA

RESET

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Rt}	Reset Threshold Voltage (note 3)	PR Open PR Grounded	4.5 3.1	4.7 3.3	4.9 3.5	V V
V_{Rth}	Reset Threshold Hysteresis		50	100	200	mV
t_{RD}	Reset Pulse Delay	C_T = 100nF ; t_R > 100µs	60	100	140	ms
t_{RR}	Reset Reaction Time	C_T = 100nF	1	10	50	µs
V_{RL}	Reset Output LOW Voltage	R_{RES} = 10KΩ to V_{O1} $V_S \geq 2V$			0.4	V
I_{LRES}	Reset Output HIGH Leakage	V_{RES} = 5V			1	µA
V_{CTth}	Delay Comparator Threshold			2.0		V
$V_{CTth, hyst}$	Delay Comparator Threshold Hysteresis			100		mV

SENSE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SIth}	Sense Threshold Voltage		1.16	1.23	1.30	V
$V_{SIth,hyst}$	Sense Threshold Hysteresis		50	100	200	mV
V_{SOL}	Sense Output LOW Voltage	$V_{SI} \leq 1.16V$; $V_S \geq 3V$ R_{SO} = 10KΩ to V_{O1}			0.4	V
I_{LSO}	Sense Output Leakage	V_{SO} = 5V ; $V_{SI} \geq 1.5V$			1	µA
I_{SI}	Sense Input Current		– 1	0.1	1	µA

Note : 1 : V_{O2} connected to ADJ.V_{O2} can be set to higher values by inserting an external resistor divider.
2 : Foldback characteristic
3 : The reset threshold can be varied continuously from 3.3V to 4.7V by connecting an external resistor from pin PR to GND.

FUNCTIONAL DESCRIPTION

The L4926/8 are based on the SGS-THOMSON Microelectronics modular voltage regulator approach. Several out-standing features and auxiliary functions are provided to meet the requirements of supplying the microprocessor systems used in automotive applications.

Furthermore the device is suitable also in other applications requiring two stabilized voltages.

The modular approach allows other features and functions to be realized easily when required.

STANDBY REGULATOR

The standby regulator uses an Isolated Collector Vertical PNP transistor as the regulating element. This structure allows a very low dropout voltage at currents up to 50mA. The dropout operation of the standby regulator is maintained down to 2V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. This feature avoids functional interruptions which could be generated by overvoltage pulses.

The typical curve of the standby output voltage as a function of the input supply voltage is shown in fig. 1.

The current consumption of the device (quiescent current) is less than 250µA when output 2 is disabled (standby mode). The dropout voltage is controlled to reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region.

The quiescent current is shown in fig. 2 as a function of the supply input voltage 2.

OUTPUT 2 VOLTAGE

The output 2 regulator uses the same output structure as the standby regulator, but rated for an output current of 500mA.

The output 2 regulator works in tracking mode with the standby output voltage as a reference voltage when the output 2 programming pin ADJ is connected to V_{O2}. By connecting a resistor divider R_1, R_2 to the pin ADJ as shown in fig. 3, the output voltage 2 can be programmed to the value :

$$V_{O2} = V_{O1} (1 + R_1/R_2)$$

The output 2 regulator can be switched off via the Enable input.

Figure 1 : Output Voltage vs. Input Voltage.

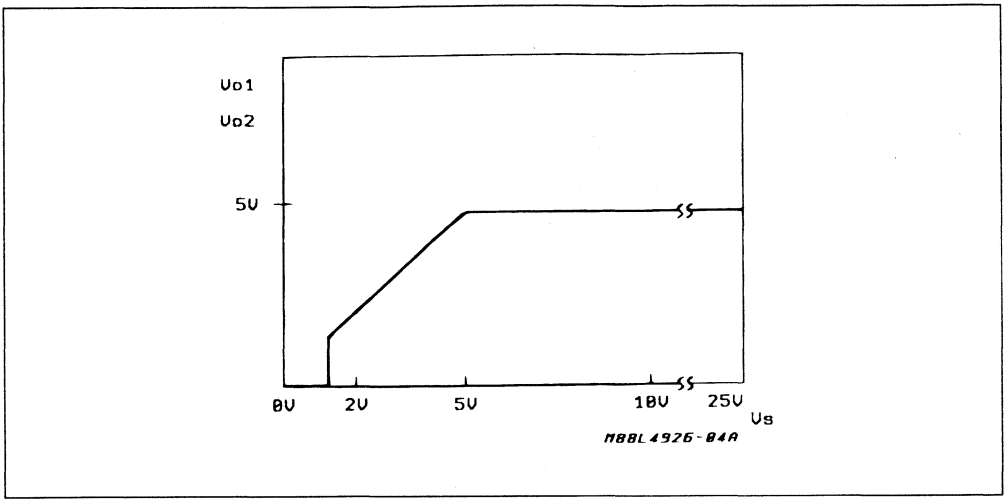


Figure 2 : Quiescent Current vs. Supply Voltage.

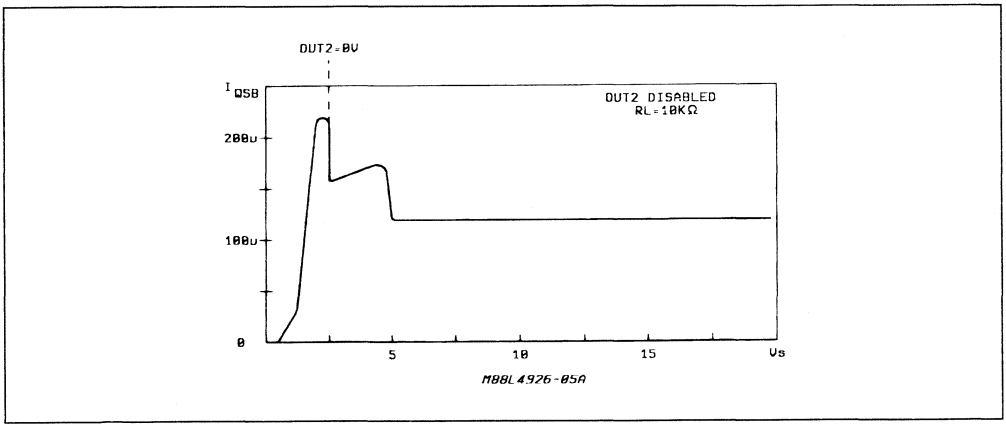
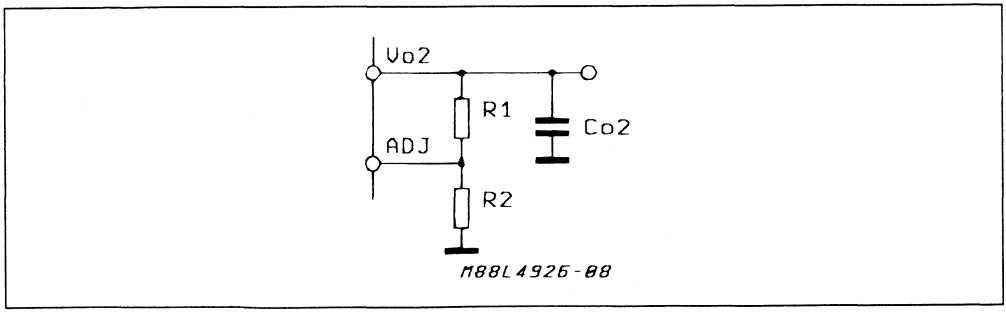


Figure 3 : Programmable Output 2 Voltage with External Resistors.



RESET CIRCUIT

The block circuit diagram of the reset circuit is shown in fig. 4. The reset circuit supervises the standby output voltage. The reset threshold of 4.7V is defined by the internal reference voltage and the standby output divider, when the pin PR is left open. The reset threshold can be programmed in the range 3.3V - 4.7V by connecting an external resistor R_{PR} from PR to GND. R_{PR} value can be calculated by :

$$R_{PR} = \frac{22K}{\frac{4.7V}{V_{Rt}} - 1} - 51.9K,\ 3.3V < V_{RT} < 4.7V$$

The reset pulse delay time t_{RD}, is defined by the charge time of an external capacitor C_T :

$$t_{RD} = \frac{C_T \times 2V}{2\mu A}$$

The reaction time of the reset circuit depends on the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T.

The reaction time of the reset circuit increases the noise immunity. In fact, if the standby output voltage drops below the reset threshold for a time shorter than the reaction time t_{RR}, no reset output variation occurs. The nominal reset delay is generated for standby output voltage drops longer than the time necessary for the complete discharging of the capacitor C_T. This time is typically equal to 50µs if C_T = 100nF. The typical reset output waveforms are shown in fig. 5.

SENSE COMPARATOR

This circuit compares an input signal with an internal voltage reference of typically 1.23V. The use of an external voltage divider makes the comparator very flexible in the application. This function can be used to supervise the input voltage - either before or after the protection diode - and to give additional information to the microprocessor such as low voltage warnings.

Figure 4 : Block Diagram of the Reset Circuit.

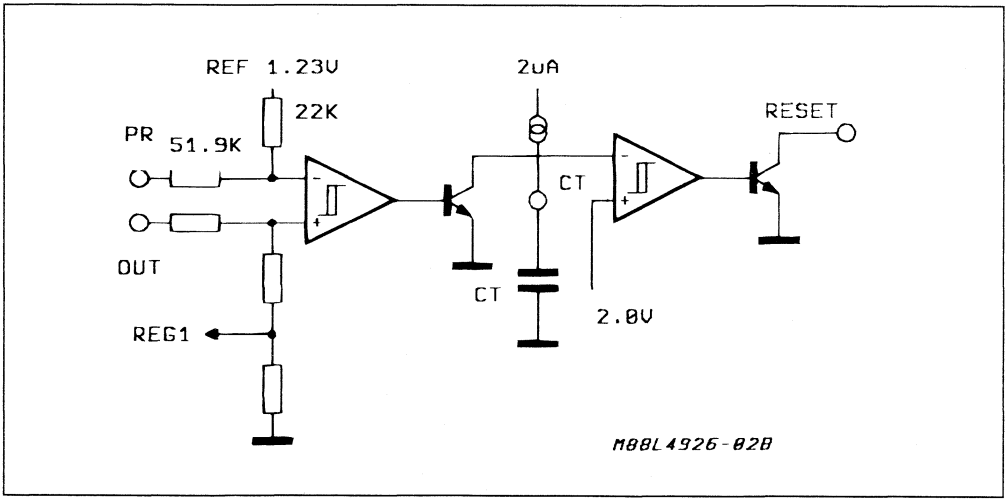
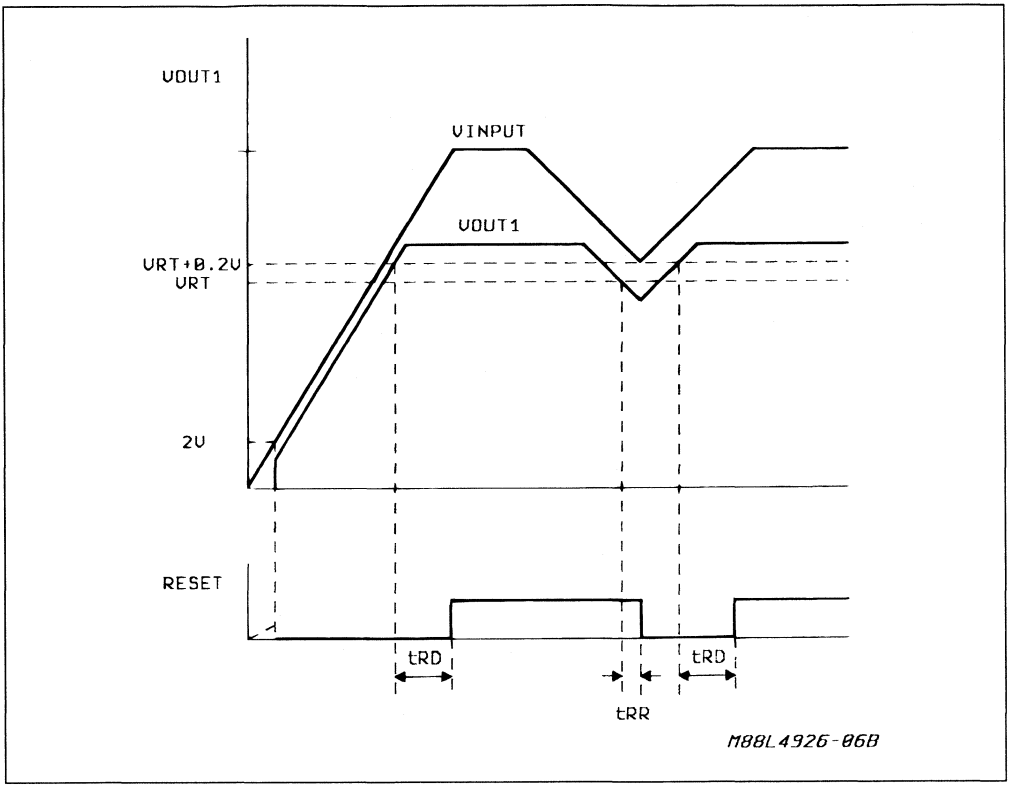


Figure 5 : Typical Reset Output Waveforms.



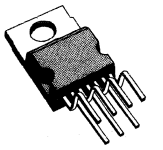
SGS-THOMSON MICROELECTRONICS

L4927

DUAL MULTIFUNCTION VOLTAGE REGULATOR

ADVANCE DATA

- STANDBY OUTPUT VOLTAGE PRECISION 5V ± 2%
- OUTPUT 2 TRACKED TO THE STANDBY OUTPUT
- OUTPUT 2 DISABLE FUNCTION FOR STANDBY MODE
- VERY LOW QUIESCENT CURRENT, LESS THAN 250µA, IN STANDBY MODE
- OUTPUT CURRENTS : I_{O1} = 50mA, I_{O2} = 500mA
- VERY LOW DROPOUT (max 0.4V/0.6V)
- OPERATING TRANSIENT SUPPLY VOLTAGE UP TO 40V
- POWER-ON RESET CIRCUIT SENSING THE STANDBY OUTPUT VOLTAGE
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS



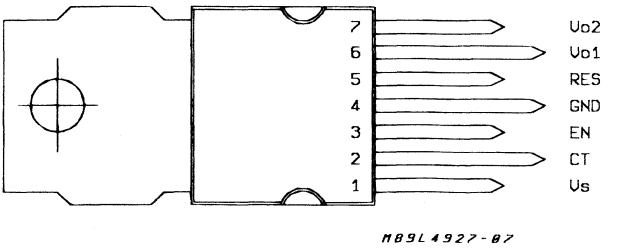
Heptawatt

ORDER CODE : L4927

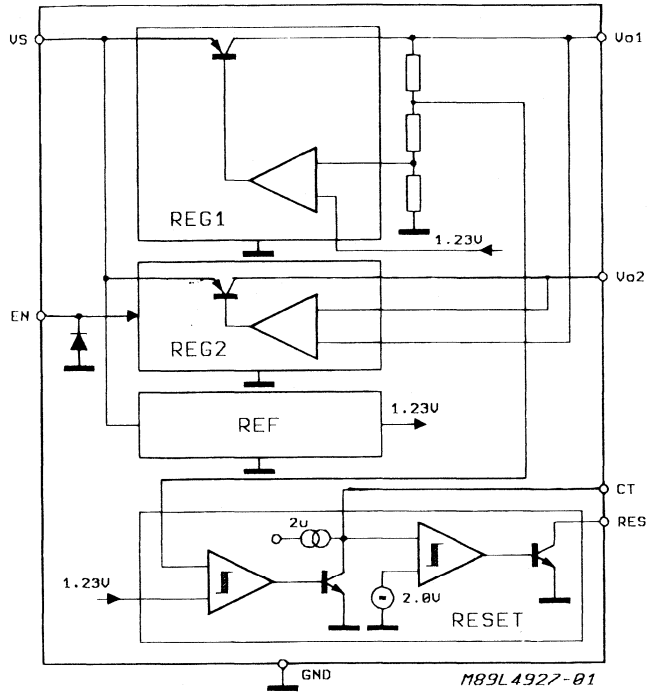
DESCRIPTION

The L4927 is a monolithic integrated dual voltage regulators with two very low dropout outputs and additional functions such as power-on reset and input voltage sense. It is designed for supplying microcomputer controlled systems specially in automotive applications.

PIN CONNECTION (top view)



BLOCK DIAGRAM



THERMAL DATA

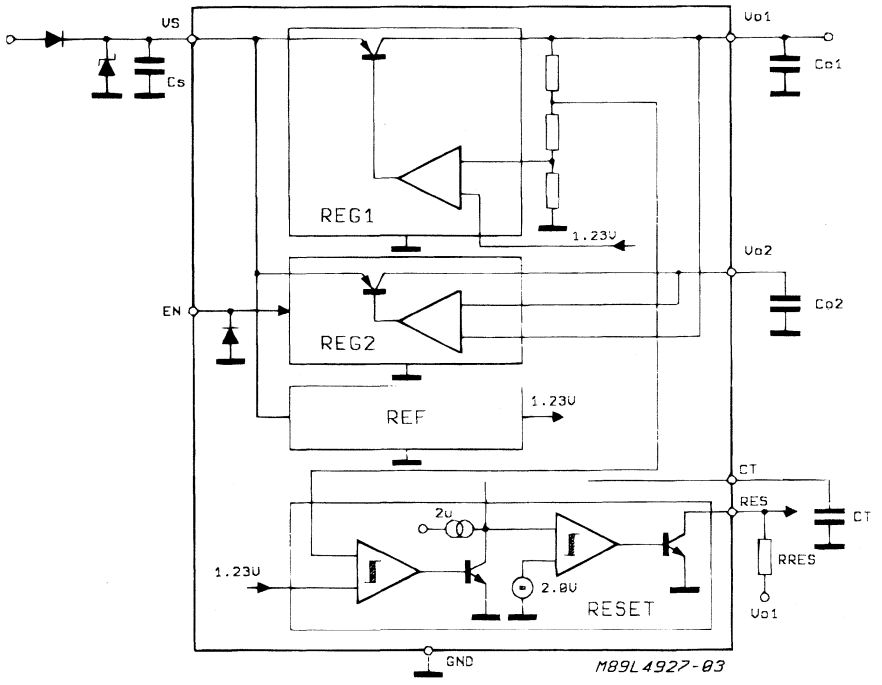
$R_{th\ j\text{-}c}$	Thermal Resistance Junction-case	Max	3	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	D.C. Supply Voltage Transient Supply Voltage (T < 1s)	28 40	V V
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C
I_{EN}	Enable Input Current (V_{EN} < – 0.3V)	– 1	mA
V_{EN}	Enable Input Voltage	V_s	V
V_{RES}	Reset Output Voltage	20	V
I_{RES}	Reset Output Current	5	mA
P_D	Power Dissipation (T_A = 80°C, $R_{th\ heatsink}$ = 90°C/W)	5	W

Note : The circuit is ESD protected according to MIL–STD–883C.

APPLICATION CIRCUIT



$C_S \geq 1\mu F$; $C_{O1} \geq 6\mu F$; $C_{O2} \geq 10\mu F$, ESR < 10Ω

ELECTRICAL CHARACTERISTICS (V_S = 14V ; – 40°C ≤ T_j ≤ 125°C unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage				25	V
V_{O1}	Standby Output Voltage	T_j = 25°C ; I_{O1} = 1mA	4.95	5.00	5.05	V
V_{O1}	Standby Output Voltage	6V ≤ V_S ≤ 25V 1mA ≤ I_{O1} ≤ 50mA	4.90	5.00	5.10	V
V_{O2}-V_{O1}	Output Voltage 2 Tracking Error (note1)	6V ≤ V_S ≤ 25V 5mA ≤ I_{O2} ≤ 500mA Enable = LOW	– 25		+ 25	mV
V_{DP1}	Dropout Voltage 1	I_{O1} = 10mA I_{O1} = 50mA		0.1 0.2	0.2 0.4	V V
V_{IO1}	Input to output Voltage Difference in Undervoltage Condition	V_S = 4V, I_{O1} = 35mA			0.4	V
V_{DP2}	Dropout Voltage 2	I_{O2} = 100mA I_{O2} = 500mA		0.2 0.3	0.3 0.6	V V
V_{IO2}	Input to output Voltage Difference in Undervoltage Condition	V_S = 4V, I_{O2} = 350mA			0.6	V
$V_{OL1.2}$	Line Regulation	6V ≤ V_S ≤ 25V I_{O1} = 1mA, I_{O2} = 5mA			20	mV
V_{OLIO1}	Load Regulation 1	1mA ≤ I_{O1} ≤ 50mA			25	mV
V_{OLO2}	Load Regulation 2	5mA ≤ I_{O2} ≤ 500mA			50	mV
I_{LIM1}	Current Limit 1	V_{O1} = 4.5V V_{O1} = 0V (note2)	55 20	100 40	200 80	mA mA
I_{LIM2}	Current Limit 2	V_{O2} = 0V	550	1000	1500	mA
I_{QSB}	Quiescent Current Standby Mode (output 2 disabled)	I_{O1} = 0.3mA ; T_j < 100°C V_{EN} ≥ 2.4V PR Open PR Grounded		 140 155	 250 280	 µA µA
I_Q	Quiescent Current	I_{O1} = 50mA I_{O2} = 500mA			20	mA

ENABLE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ENL}	Enable Input LOW Voltage (output 2 active)		– 0.3		1.5	V
V_{ENH}	Enable Input HIGH Voltage		2.4		7	V
V_{ENhyst}	Enable Hysteresis		30	75	200	mV
I_{EN}	Enable Input Current	0V < V_{EN} < 1.2V 25V < V_{EN} < 7V	– 10 – 1	– 1.5 0	– 0.5 + 1	µA µA

RESET

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Rt}	Reset Threshold Voltage (note3)	PR Open PR Grounded	4.5 3.1	4.7 3.3	4.9 3.5	V V
V_{Rth}	Reset Threshold Hysteresis		50	100	200	mV
t_{RD}	Reset Pulse Delay	C_T = 100nF ; t_R > 100µs	60	100	140	ms
t_{RR}	Reset Reaction Time	C_T = 100nF	1	10	50	µs
V_{RL}	Reset Output LOW Voltage	R_{RES} = 10KΩ to V_{O1} $V_S \geq 2V$			0.4	V
I_{LRES}	Reset Output HIGH Leakage	V_{RES} = 5V			1	µA
V_{CTth}	Delay Comparator Threshold			2.0		V
$V_{CTth,\,hyst}$	Delay Comparator Threshold Hysteresis			100		mV

Note : 1 : V_{O2} connected to ADJ.V_{O2} can be set to higher values by inserting an external resistor divider.
2 : Foldback characteristic

FUNCTIONAL DESCRIPTION

The L4927 is based on the SGS-THOMSON Microelectronics modular voltage regulator approach. Several out-standing features and auxiliary functions are provided to meet the requirements of supplying the microprocessor systems used in automotive applications.

Furthermore the device is suitable also in other applications requiring two stabilized voltages.

The modular approach allows other features and functions to be realized easily when required.

STANDBY REGULATOR

The standby regulator uses an Isolated Collector Vertical PNP transistor as the regulating element. This structure allows a very low dropout voltage at currents up to 50mA. The dropout operation of the standby regulator is maintained down to 2V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. This feature avoids functional interruptions which could be generated by overvoltage pulses.

The typical curve of the standby output voltage as a function of the input supply voltage is shown in fig. 1.

The current consumption of the device (quiescent current) is less than 250µA when output 2 is disabled (standby mode). The dropout voltage is controlled to reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region.

The quiescent current is shown in fig. 2 as a function of the supply input voltage 2.

OUTPUT 2 VOLTAGE

The output 2 regulator uses the same output structure as the standby regulator, but rated for an output current of 500mA.

The output 2 regulator works in tracking mode with the standby output voltage as a reference voltage.

The output 2 regulator can be switched off via the Enable input.

Figure 1 : Output Voltage vs. Input Voltage.

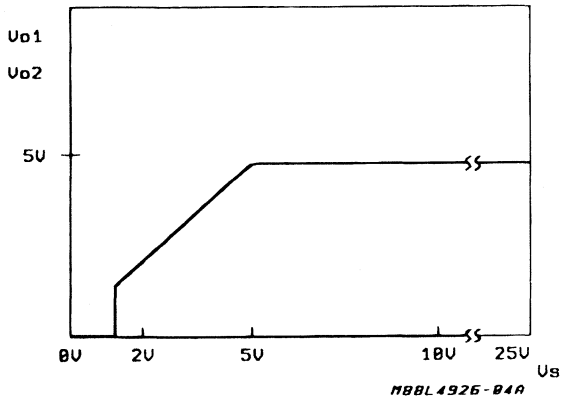
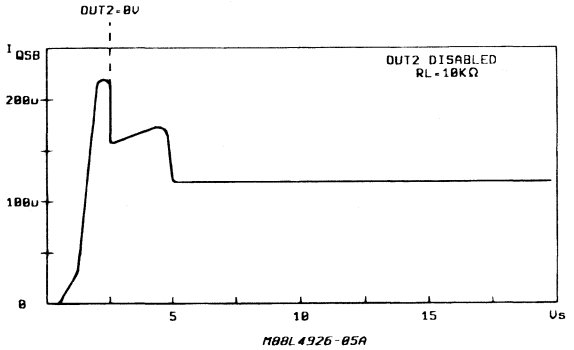


Figure 2 : Quiescent Current vs. Supply Voltage.



RESET CIRCUIT

The block circuit diagram of the reset circuit is shown in fig. 3. The reset circuit supervises the standby output voltage. The reset threshold of 4.7V is defined by the internal reference voltage and the standby output divider.

The reset pulse delay time t_{RD}, is defined by the charge time of an external capacitor C_T :

$$t_{RD} = \frac{C_T \times 2V}{2\mu A}$$

The reaction time of the reset circuit depends on the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T.

The reaction time of the reset circuit increases the noise immunity. In fact, if the standby output voltage drops below the reset threshold for a time shorter than the reaction time t_{RR}, no reset output variation occurs. The nominal reset delay is generated for standby output voltage drops longer than the time necessary for the complete discharging of the capacitor C_T. This time is typically equal to 50µs if C_T = 100nF. The typical reset output waveforms are shown in fig.

Figure 3 : Block Diagram of the Reset Circuit.

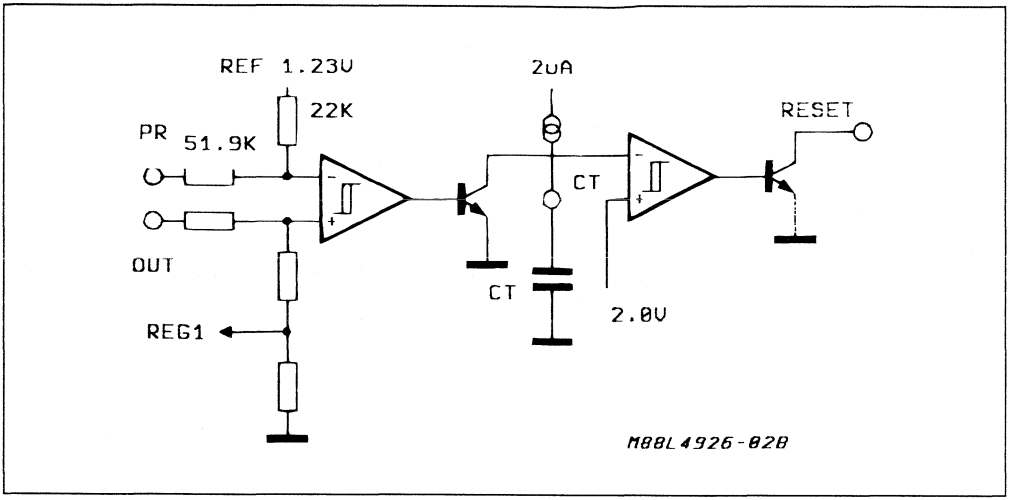
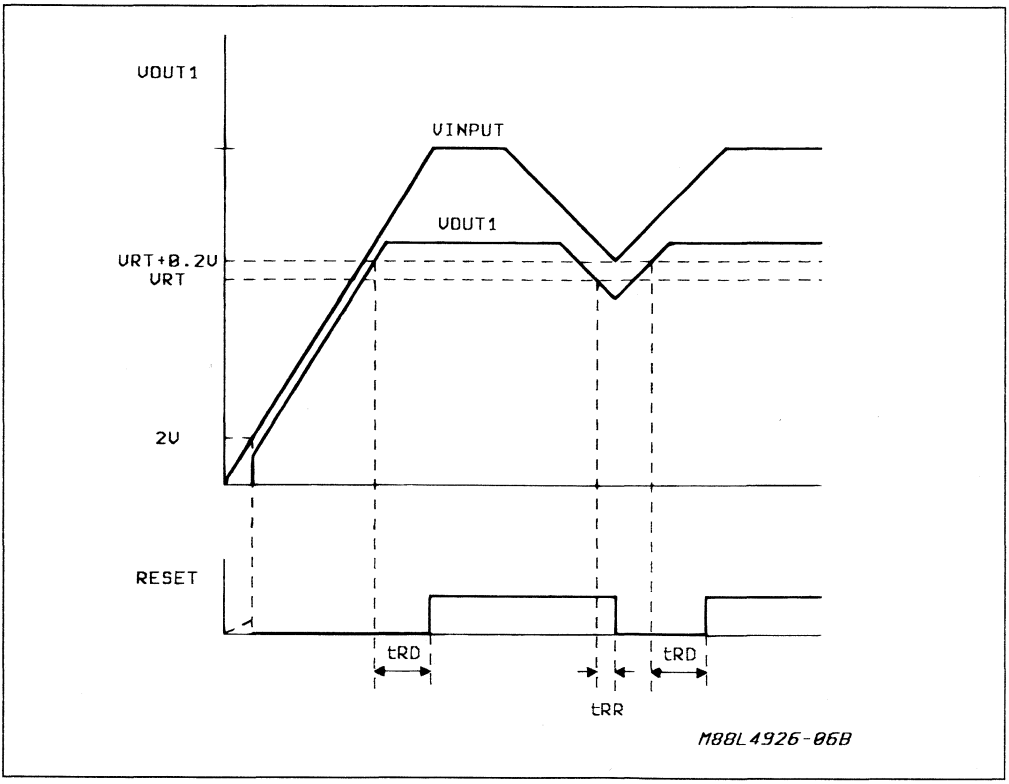


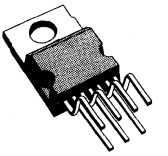
Figure 4 : Typical Reset Output Waveforms.



DUAL VERY LOW DROP VOLTAGE REGULATOR

ADVANCE DATA

- OUTPUT VOLTAGES 5V AND 9.5V
- OPERATING DC SUPPLY VOLTAGE RANGE 5V – 25V
- OPERATING TRANSIENT SUPPLY VOLTAGE UP TO 40V
- EXTREMELY LOW QUIESCENT CURRENT IN STANDBY MODE
- OUTPUT 2 DISABLE FUNCTION FOR STAND-BY MODE
- OUTPUT CURRENT CAPABILITY 100mA AND 500mA
- VERY LOW DROPOUT VOLTAGES LESS THAN 0.4V/0.6V
- RESET CIRCUIT SENSING THE STANDBY OUTPUT VOLTAGE
- PROGRAMMABLE RESET PULSE DELAY WITH EXTERNAL CAPACITOR
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS



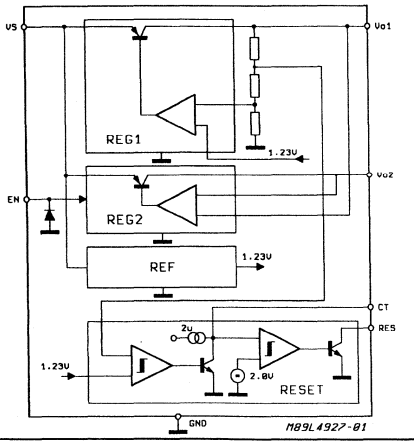
HEPTAWATT

ORDER CODE : L4930

DESCRIPTION

The L4930 is a monolithic integrated dual voltage regulator with two very low dropout outputs and power-on reset. It is designed especially for car radio applications with very low quiescent current in standby mode.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

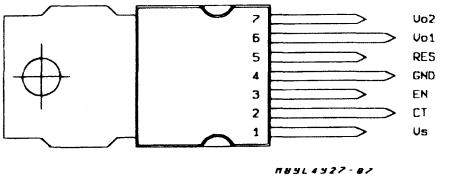
Symbol	Parameter	Value	Unit
V_S	D.C. Supply Voltage Transient Supply Voltage (T < 1s)	28 40	V V
I_O	Output Currents	Internally Limited	
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to + 150	°C
I_{EN}	Enable Input Current	± 1	mA
V_{RES}	Output Voltage	20	V
I_{RES}	Output Current	5	mA

Note : The circuit is ESD protected accorcing to MIL-STD-883C.

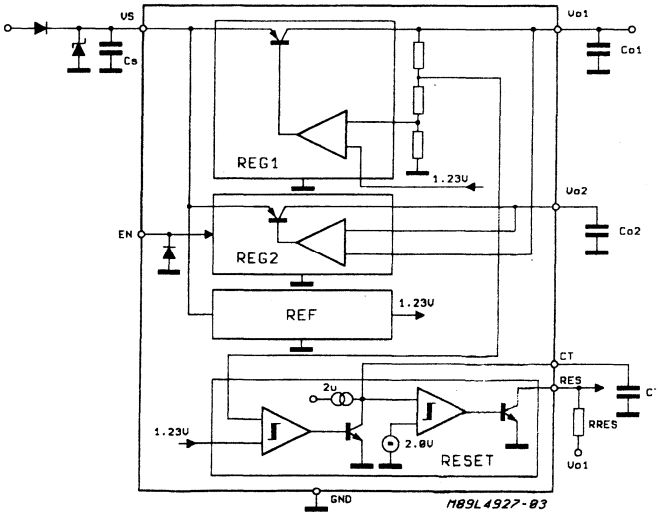
THERMAL DATA

$R_{th\ j\text{-}c}$	Thermal Resistance Junction-case	Max	3.5	°C/W

PIN CONNECTION (top view)



APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS (V_S = 14V ; – 25°C ≤ T_A ≤ 85°C unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Standby Output Voltage	T_j = 25°C ; I_{OUT} = 1mA	4.90	5	5.1	V
V_{O1}	Standby Output Voltage	6V < V_{IN} < 20V 1mA < I_{O1} < 100V	4.85	5	5.15	V
V_{O2}	Output Voltage 2	10.2V ≤ V_{IN} ≤ 20V 5mA < I_{O2} < 500mA	9.2	9.5	9.7	V
V_{DP1}	Dropout Voltage 1	I_{OUT1} = 10mA I_{OUT1} = 50mA		0.1 0.2	0.2 0.4	V V
V_{DP2}	Dropout Voltage 2	I_{OUT2} = 100mA I_{OUT2} = 500mA		0.15 0.25	0.3 0.5	V V
$V_{OL11.2}$	Line Regulation	6V < V_{IN} < 20V I_{O1} = 1mA, I_{O2} = 5mA		1	20	mV
V_{OL01}	Load Regulation 1	1mA < I_{OUT1} < 100mA		5	25	mV
V_{OL02}	Load Regulation 2	5mA < I_{OUT2} < 500mA		5	50	mV
I_{LIM1}	Current Limit 1	V_{O1} = 4.5V	100	150		mA
I_{LIM2}	Current Limit 2	V_{O2} = 0V	550	750	1500	mA
I_{QSB}	Quiescent Current in Standby Mode	V_{EN} ≤ 1.5V (output 2 disabled) I_{O1} = 0.3mA	130	200	250	µA
I_Q	Quiescent Current	I_{OUT1} = 100mA ; I_{OUT2} = 500mA			25	mA

ENABLE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ENL}	Enable Input LOW Voltage (output 2 disabled)		– 0.3		1.5	V
V_{ENH}	Enable Input HIGH Voltage		2.4		7	V
V_{ENhyst}	Enable Hysteresis		30	75	200	mV
I_{EN}	Enable Input Current	0V < V_{EN} < 1.2V 25V < V_{EN} < 7V	– 10 – 1	– 1.5 0	– 0.5 + 1	µA µA

RESET

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Rt}	Reset Threshold Voltage		4.5	4.7	4.9	V
V_{Rth}	Reset Threshold Hysteresis		50	100	200	mV
t_{RD}	Reset Pulse Delay	C_T = 68nF ; t_R ≥ 100µs	60	100	140	ms
t_{RR}	Reset Reaction Time	C_T = 68nF	1	10	50	µs
V_{RL}	Reset Output LOW Voltage	R_{RES} = 10KΩ to V_{OUT1} V_{IN} ≥ 2V			0.4	V
I_{LRES}	Reset Output HIGH Leakage Current	V_{RES} = 5V			1	µA

FUNCTIONAL DESCRIPTION

STANDBY REGULATOR

The standby regulator uses an Isolated Collector Vertical PNP transistor as the regulating element. This structure allows a very low dropout voltage at currents up to 50mA. The dropout operation of the standby regulator is maintained down to 2V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. This feature avoids functional interruptions which could be generated by overvoltage pulses.

The current consumption of the device (quiescent current) is less than 250µA when output 2 is disabled. (standby mode). The dropout voltage is controlled to reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region.

The quiescent current is shown in fig. 2 as a function of the supply input voltage 2.

OUTPUT 2 VOLTAGE

The output 2 regulator uses the same output structure as the standby regulator, but rated for an output current of 500mA and the output regulated voltage = 9.5V.

The output 2 regulator can be switched off via the Enable input.

RESET CIRCUIT

The block circuit diagram of the reset circuit is shown in fig. 3. The reset circuit supervises the standby output voltage. The reset threshold of 4.7V is defined by the internal reference voltage and the standby output divider.

The reset pulse delay time t_{RD}, is defined by the charge time of an external capacitor C_T :

$$t_{RD} = \frac{C_T \times 2V}{2\mu A}$$

The reaction time of the reset circuit depends on the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T.

The reaction time of the reset circuit increases the noise immunity.

In fact, if the standby output voltage drops below the reset threshold for a time shorter than the reaction time t_{RR}, no reset output variation occurs. The nominal reset delay is generated for standby output voltage drops longer than the time necessary for the complete discharging of the capacitor C_T. The typical reset output waveforms are shown in fig. 5.

Figure 2 : Quiescent Current vs. Supply Voltage.

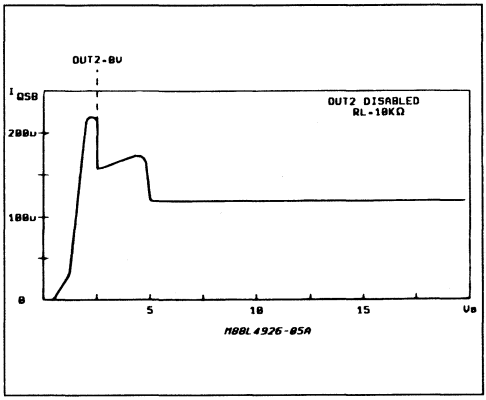


Figure 3 : Block Diagram of the Reset Circuit.

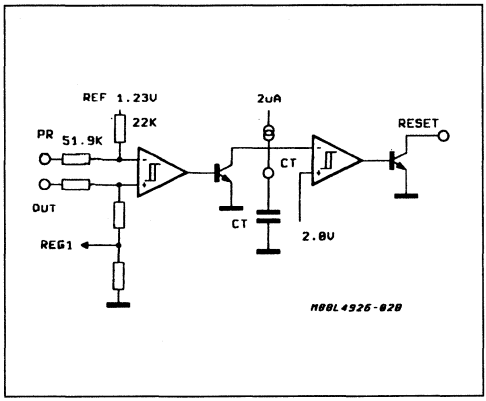
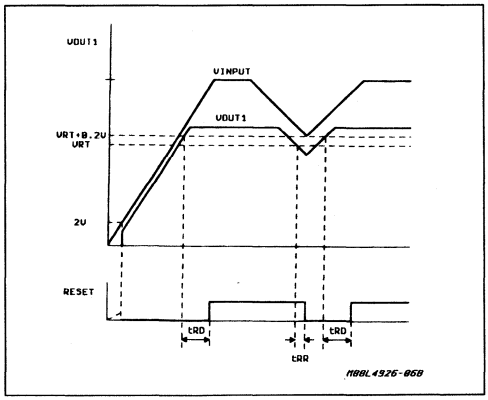


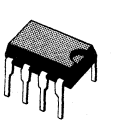
Figure 4 : Typical Reset Output Waveforms.

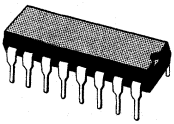


DUAL 5V REGULATOR WITH RESET ENABLE AND AUXILIARY CURRENT SINK OUTPUT

ADVANCE DATA

- VERY LOW DROPOUT VOLTAGE FOR BOTH OUTPUTS (max 0.6V, $-40 \leq T_J \leq +125°C$)
- VERY LOW QUIESCENT CURRENT
- OUTPUT VOLTAGE PRECISION 5V 4% OVER FULL T RANGE
- OUTPUT CURRENTS : $I_{01} = 50mA$, $I_{02} = 100mA$
- POWER-ON RESET CIRCUIT SENSING THE STANDBY OUTPUT VOLTAGE
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- CURRENT SINK OUTPUT FOR AUXILIARY FUNCTIONS
- ENABLE FUNCTION FOR THE ENABLE REGULATOR AND THE CURRENT SINK OUTPUT
- OVERVOLTAGE, SHORT CIRCUIT, REVERSE BATTERY AND THERMAL PROTECTIONS





MINIDIP **POWERDIP** (12 + 2 + 2 lead)

ORDER CODES : L4934 (Minidip)
L4935 (Powerdip)

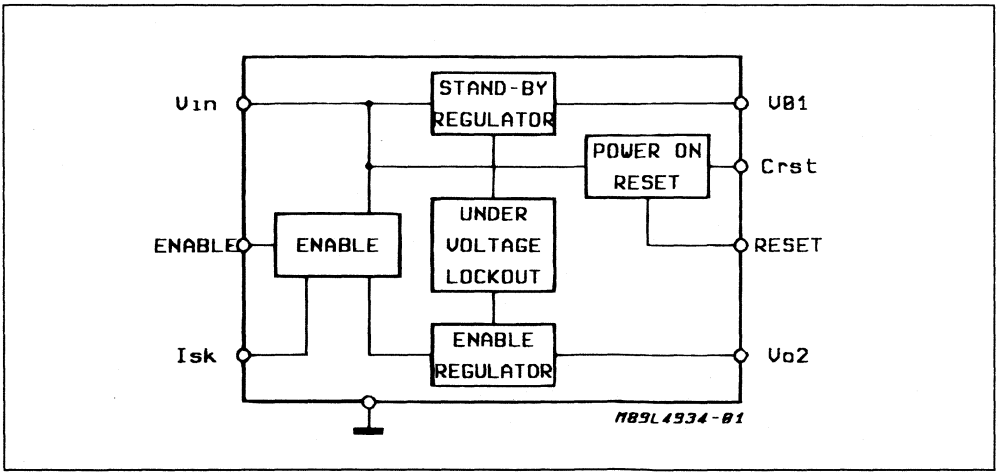
DESCRIPTION

The L4934/5 is a monolithic very low drop voltage regulator intended primarily for applications with microprocessors operating in low power standby conditions.

The device provides two 5V regulated outputs. The first output (V_{01}) delivers up to 50mA. The second output (V_{02}) supplies 100mA and is controlled by the ENABLE function which also controls the current sink output. In addition the device provides the RESET function for the microprocessor.

The L4934/5 is mounted in two different packages : 8-lead plastic minidip for L4934, 12 + 2 + 2 Powerdip for L4935.

BLOCK DIAGRAM



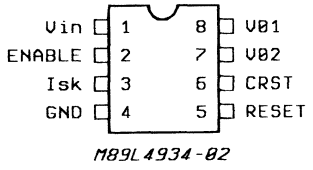
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{in}	D.C. Supply Voltage Transient Supply Overvoltage : Load Dump : 5ms ≤ trise ≤ 10ms, τf = 100ms, $R_{SOURCE} \geq 0.5\Omega$ Reverse Supply Voltage	+ 24 + 50 − 16	V V V
T_j, T_{stg}	Junction and Storage Temperature Range	− 55 to 150	°C
I_{01}, I_{02}	Standby Regulator Current Enabled Regulator Current	Internally Limited	
I_{SK}	Sinking Capability Current Sourcing Capability Current	Internally Limited 100	 mA
V_{EAB}	DC Input Voltage Range (E_{AB}, C_{RST})	− 0.3 V_{01} + 0.3	V
I_{RST}	Output Current	− 20	mA

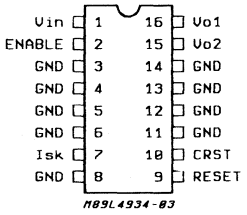
THERMAL DATA

			MINIDIP 8	POWERDIP 12+2+2	
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	70	°C/W
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins 4	Max	70	15	°C/W

PIN CONNECTIONS (top view)



MINIDIP



POWERDIP

PINS FUNCTIONS

N°	Name	Function
1	V_{in}	Supply Voltage Input
2	ENABLE	Enable Input Voltage : a high level on this pin enables V_{02} and I_{SK} outputs driver output.
3	I_{SK}	100mA open collector current sink driving external circuitry.
4	GND	Ground
5	RESET	Reset
6	CRST	External timing capacitor setting the power-on reset delay.
7	V_{02}	5V Output Controlled by the ENABLE Function
8	V_{01}	Standby 5V Output

ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V ; $-40°C \leq T_j \leq +125°C$; C_{out1} = 33µF ; C_{out2} = 33µF unless otherwise noted).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_Q	Quiescent Current	5.85V < V_{IN} < 16V I_{01} = 10mA $V_{(EAB)} = V_{EABL}$ $T_j = -40°C$ $-40 \leq T_j \leq 125°C$			 1 2.5	 mA mA

STANDBY REGULATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{01}	Output Voltage	5.85V < V_{IN} < 16V 10µA < I_{01} < 50mA	4.80		5.20	V
I_{01SC}	Short Circuit Current	V_{01} shorted to GND.	75			mA
V_{01DP}	Drop Out Voltage	I_{01} = 10mA I_{01} = 50mA			0.35 0.6	V V
C_{V01}	Output Capacitor Capacitance Output Capacitor Equivalent Series Resistance		33		 6	µF Ω
V_{O01SVR}	Supply Voltage Rejection	$V_{ripple} = 2V_{pp}$; f = 120Hz		50		dB

ENABLE REGULATOR ($V_{(EAB)} > V_{EABH}$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{02}	Output Voltage	5.85V < V_{IN} < 16V 10µA < I_{01} < 100mA	4.80		5.20	V
I_{01SC}	Short Circuit Current	V_{02} shorted to GND.	125			mA
V_{02DP}	Drop Out Voltage	I_{02} = 100mA			0.6	V
C_{V02}	Output Capacitor Capacitance Output Capacitor Equivalent Series Resistance		33		 6	µF Ω
V_{02SVR}	Supply Voltage Rejection	V_{ripple} = 2Vp-p ; f = 120Hz		50		dB

ENABLE INPUT BUFFER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{EABH}	Enable Input High Voltage		2.4			V
V_{EABL}	Enable Input Low Voltage				0.8	V
I_{EAB}	Enable Input Current	0 < V_{EAB} < 5V	–20		20	µA

ENABLE SINK OUTPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SKSC}	Enable Sink Current	$V_{(ISK)}$ > 2V	125			mA
I_{SKSAT}	Enable Sink Output on Voltage	$I_{(ISK)} = -100mA$			0.5	V
I_{SKLK}	Enable Sink Leakage	$V_{EAB} = V_{EABL}$			25	µA

ELECTRICAL CHARACTERISTICS (continued)

RESET FUNCTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RST}	Reset Threshold Voltage	Measured at V_{01} pin.	4.0		4.5	V
V_{RSTL}	Reset Output on Voltage	$V_{(CRST)} = 3.9$, $I_{(RST)} = -16mA$			0.8	V
V_{LVR}	Low Voltage Reset	$1V < V_{IN} < 16V$, V(CRST) = 0V, 1K resistor connected between R_{ST} and V_{01}.			0.8	V
T_{RST}	Reset Delay Time	$C_{RST} = 0.47\mu F$, V_{IN} stepped 0-14.4V.	100		200	msec

FUNCTIONAL DESCRIPTION

The L4934/5 dual voltage regulator contains four functional blocks. There are two 5 volt low drop regulators, a current sink output driver and a reset timing module. The circuit as a whole can withstand reverse battery voltage on the input and also contains an overtemperature shutdown, which disables both regulators, the current sink driver and pulls the reset output low.

Additionally, if the input voltage exceeds (V_{INSD}), both regulators shut down, the current sink output disables and the reset output goes low. The circuit is capable of handling + 50 volt load dump transients. The four major modules function as follows :

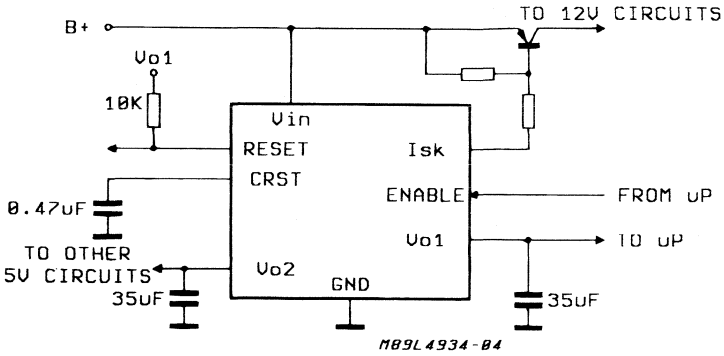
Standby Regulator (V_{D1}) - This regulator is always active and is intended for 5 volt loads of up to 75mA maximum. The regulator exhibits a very low dropout voltage and is self protected against overcurrent conditions. The standby output (V_{01}) requires a 33 microfarad capacitor to ground for stability. The circuit does not discharge the output capacitor if the input supply voltage is lost, granting some immunity to input supply transients. During power up, the V_{01} output stays low for input voltages less than 3.5 volts and then tracks the input until regulation is achieved. It is guaranteed that the R_{ST} output is low until the V_{01} output exceeds V_{RST} as specified in the Electrical Characteristics.

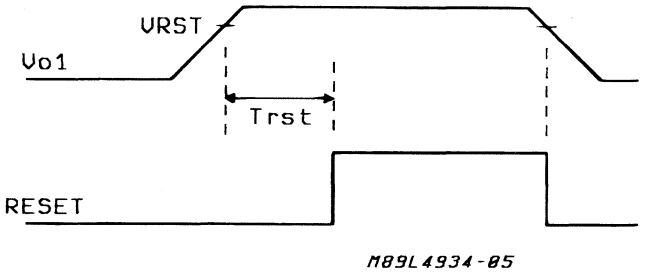
Enable Regulator (V02) - This regulator is activated only when the Enable pin voltage is more positive than V_{EABH} and V_{01} has exceeded V_{RST} (see Electrical Characteristics). Whenever V_{01} is less than V_{RST}, it has precedence over the state of the enable input. The V_{02} output is intended for loads of up to 125mA maximum. This regulator also exhibits a very low dropout voltage and is self protected against overcurrent conditions. The recommended output capacitor for the V_{02} output is 33 microfarads to ground. This circuit does not discharge the capacitor if the input supply is lost. If the Enable pin is held low, the V_{02} output will stay off for all values of V_{IN}.

Current Sink Output Driver (I_{SK}) - The I_{SK} output is an NPN open collector driver intended for actuating an external pass transistor used as a high side power switch. Figure 1 shows an example of an external PNP transistor used for this function. The I_{SK} output becomes active low if the E_{AB} input pin is more positive than V_{EABH} and if V_{CC} is greater than V_{RST}. The I_{SK} output is always off otherwise. The output is capable of sinking 150mA maximum, but is internally protected against overcurrent conditions.

Reset Module (C_{RST} and RESET) - The RESET output is active low and provides a reset signal for microprocessor systems at power up. The RESET output is low whenever the voltage on the C_{RST} pin is less than 1.25 volts nominally. Normally, a 0.47 microfarad capacitor should be connected between the C_{RST} pin and ground. If the V_{CC} output voltage drops below V_{RST} the capacitor is discharged by an internal pull-down. Once V_{CC} goes above V_{RST}, an internal charging current pulls the capacitor up. The nominal reset pulse duration is 150msec with a 0.47 microfarad reset capacitor.

Figure 1 : Typical Application Circuit.





5 V VERY LOW DROP VOLTAGE REGULATOR

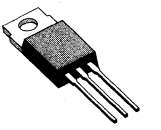
ADVANCE DATA

- PRECISE OUTPUT VOLTAGE (5 V ± 4 %) OVER FULL TEMPERATURE RANGE (–40/125°C)
- VERY LOW VOLTAGE DROP (0.75 Vmax) OVER FULL TEMP. RANGE
- OUTPUT CURRENT UP TO 500 mA
- + 80/- 80 V LOAD DUMP PROTECTION
- OVERVOLTAGE AND REVERSE VOLTAGE PROTECTIONS
- SHORT CIRCUIT PROTECTION AND THERMAL SHUT-DOWN (with hysteresis)
- LOW START UP CURRENT

DESCRIPTION

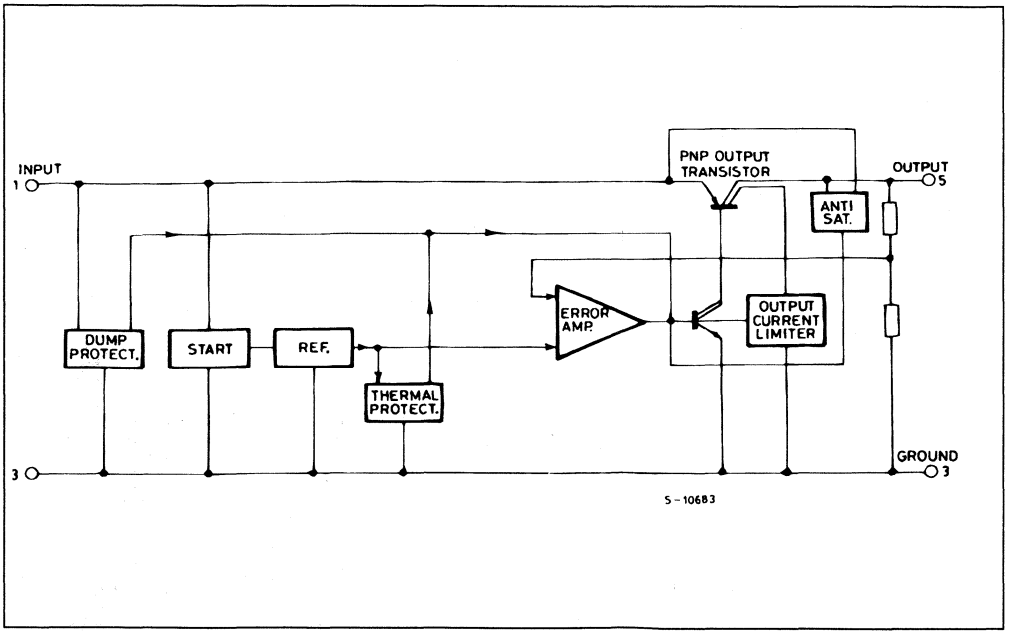
The L4945 is a monolithic integrated circuit in Versawatt package specially designed to provide a stabilized supply voltage for automotive and industrial electronic systems. Thanks to its very low voltage drop, in automotive applications the L4945 can work correctly even during the cranking phase, when the battery voltage could fall as low as 6 V. Furthermore, it incorporates a complete range of protection circuits against the dangerous overvoltages always present on the battery rail of the car.

TO220



ORDER CODE : L4945

BLOCK DIAGRAM



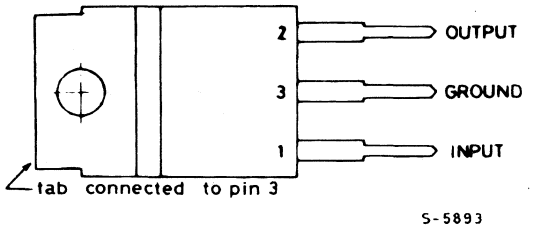
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Forward Input Voltage	35	V
V_i	Reverse Input Voltage Positive Transient Peak Voltage (t = 300 ms) Negative Transient Peak Voltage (t = 100 ms)	– 18 80 – 80	V V V
T_J	Junction Temperature Range	– 40 to 150	°C
T_{OP}	Operating Temperature Range	– 40 to 125	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

PIN CONNECTION (top view)

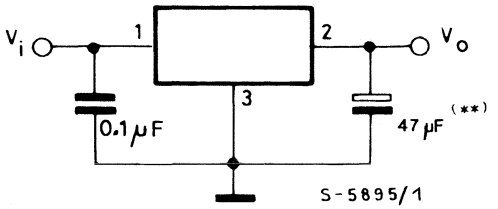


ELECTRICAL CHARACTERISITCS (refer to the test circuit, V_i = 14. 4 V, C_o = 47/µF, ESR < 10 Ω, – 40 °C < T_J < 125 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage Range	I_o = 5 mA to 500 mA Over Full T Range T_J = 25 °C	4.80 4.90	5.00 5.00	5.20 5.10	V V
V_i	Operating Input Voltage	I_o = 5 mA to (*) 500 mA	6		26	V
ΔV_o	Line Regulation	V_i = 6 V to 26 V ; I_o = 5 mA		5	50	mV
ΔV_o	Load Regulation	I_o = 5 mA to 500 mA		15	60	mV
V_d	Dropout Voltage	I_o = 500 mA, T_J = 25 °C Over Full T Range		0.40	0.55 0.75	V V
I_Q	Quiescent Current	I_o = 0 mA, T_J = 25 °C I_o = 0 mA Over Full T I_o = 500 mA Over Full T		5 6.5 110	10 13 180	mA mA mA
$\frac{\Delta V_o}{T}$	Temperature Output Voltage Drift			– 0.5		mV/°C
SVR	Supply Volt. Rej.	I_o = 350 mA ; f = 120 Hz C_o = 100 µF ; V_i = 12 V ± 5 V_{pp}	50	60		dB
I_{sc}	Output Short Circuit Current		0.50	0.80	1.50	A

(*) For a DC voltage 26 < V_i < 35 V the device is not operating.

TEST CIRCUIT



(**) Min 20 / µF, ESR < 10 Ω over full temperature range.

FUNCTIONAL DESCRIPTION

The block diagram shows the basic structure of the device : the reference, the error amplifier, the driver, the power PNP, the protection functions.

The power stage is a Lateral PNP transistor which allows a very low dropout voltage (typ. 400 mV at T_J = 25 °C, max. 750 mV over the full temperature range @ I_O = 500 mA). The typical curve of the dropout voltage as a function of the junction temperature is shown in Fig. 1 : that is the worst case, where I_O = 500 mA.

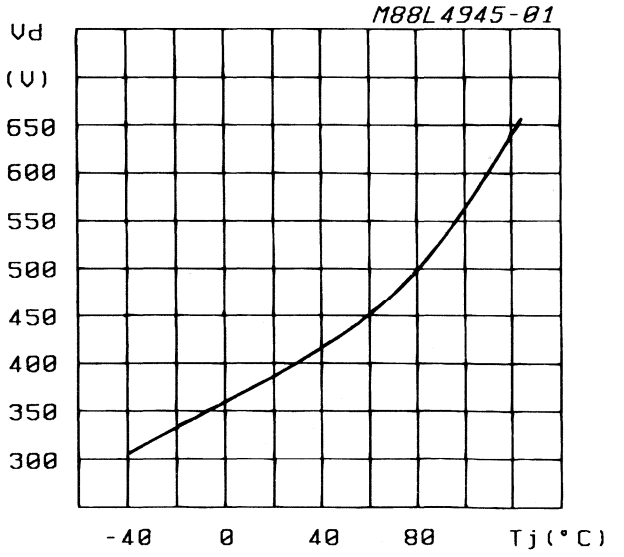
The current consumption of the device (quiescent current) is maximum 10 mA - over full T - when no load current is required.

The internal antisaturation circuit allows a drastic reduction in the current peak which takes place during the start up.

The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (C_{Omin} = 20 µF) to guarantee the global stability of the system.

Load dump protection (± 80 V, t = 300 ms), reverse voltage (- 18 V) and short circuit protection, thermal shutdown are the main features that make the L4945 specially suitable for applications in the automotive enviroment.

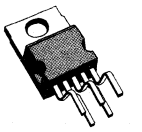
Figure 1 : Typical Dropout Voltage vs. T_j (I_O = 500 mA).



5V-0.5A VERY LOW DROP REGULATOR WITH RESET

ADVANCE DATA

- PRECISE OUTPUT VOLTAGE (5V ± 4%) OVER FULL TEMPERATURE RANGE (– 40 / 125 °C)
- VERY LOW VOLTAGE DROP (0.75Vmax) OVER FULL T RANGE
- OUTPUT CURRENT UP TO 500mA
- RESET FUNCTION
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- + 80V LOAD DUMP PROTECTION
- – 80V LOAD DUMP PROTECTION
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION AND THERMAL SHUT-DOWN (with hysteresis)
- LOW START UP CURRENT



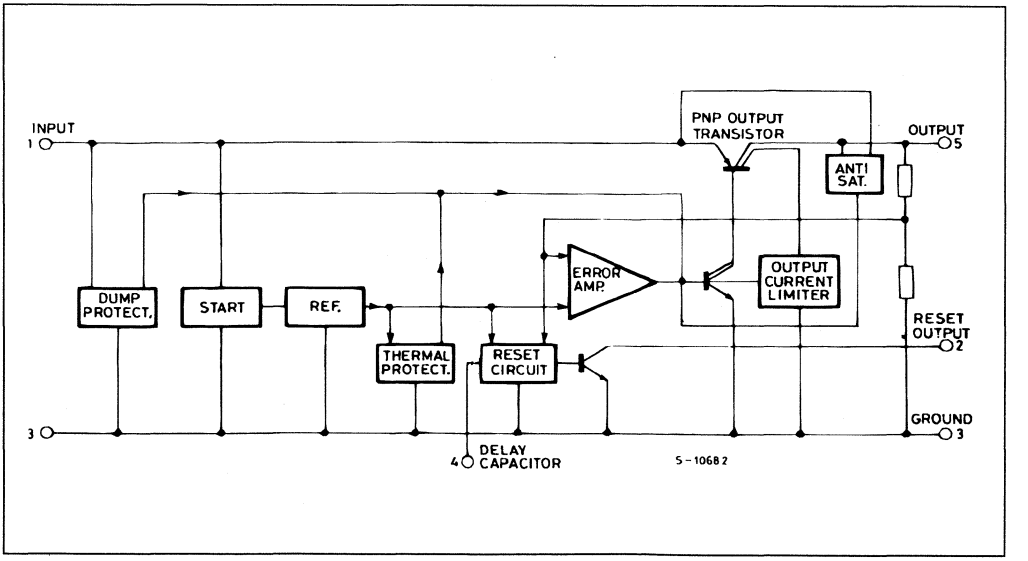
Pentawatt

ORDER CODE : L4947

DESCRIPTION

The L4947 is a monolithic integrated circuit in Pentawatt package specially designed to provide a stabilized supply voltage for automotive and industrial electronic systems. Thanks to its very low voltage drop, in automotive applications the L4947 can work correctly even during the cranking phase, when the battery voltage could fall as low as 6V. Furthermore, it incorporates a complete range of protection circuits against the dangerous overvoltages always present on the battery rail of the car. The reset function makes the device particularly suited to supply microprocessor based systems : a signal is available (after an externally programmable delay) to reset the microprocessor at power-on phase ; at power-off, this signal becomes low inhibiting the microprocessor.

BLOCK DIAGRAM



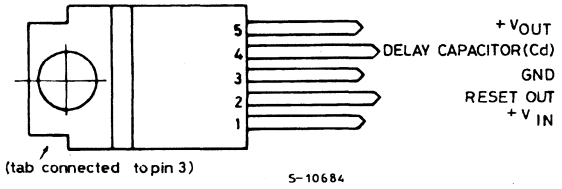
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	35	V
	DC Reverse Input Voltage	— 18	V
	Transient Input Overvoltages :		
	Load Dump :	80	V
	5ms ≤ t_{rise} ≤ 10ms		
	τ_f Fall Time Constant = 100ms		
	R_{SOURCE} ≥ 0.5Ω		
	Field Decay :	− 80	V
	5ms ≤ t_{fall} ≤ 10ms, R_{SOURCE} ≥ 10Ω		
	τ_r Rise Time Constant = 33ms		
	Low Energy Spike :	± 100	V
	t_{rise} = 1µs, t_{fall} = 500µs, R_{SOURCE} ≥ 10Ω		
	f_r Repetition Frequency = 5Hz		
V_R	Reset Output Voltage	35	V
T_J, T_{stg}	Junction and Storage Temperature Range	− 55 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3.5	°C/W

PIN CONNECTION (top view)



ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_i = 14. 4V, C_o = 47µF, ESR < 10Ω, R_p = 1KΩ, R_L = 1KΩ, − 40°C ≤ T_J ≤ 125°C, unless otherwise specified)

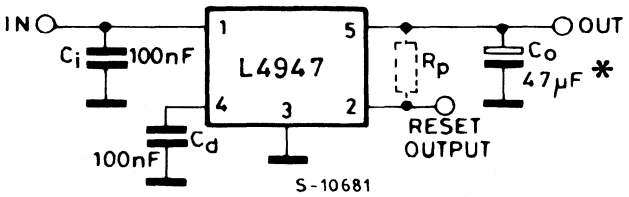
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 5mA to 500mA	4.80	5.00	5.20	V
		Over Full T Range				
		T_J = 25°C	4.90	5.00	5.10	V
V_i	Operating Input Voltage	I_o = 5mA to (*) 500mA	6		26	V
ΔV_o	Line Regulation	V_i = 6V to 26V ; I_o = 5mA		5	50	mV
ΔV_o	Load Regulation	I_o = 5mA to 500mA		15	60	mV
$V_i - V_o$	Dropout Voltage	I_o = 500mA, T_J = 25°C		0.40	0.55	V
		Over Full T Range			0.75	V
I_q	Quiescent Current	I_o = 0mA, T_J = 25°C		5	10	mA
		I_o = 0mA Over Full T		6.5	13	mA
		I_o = 500mA Over Full T		110	180	mA
$\frac{\Delta V_o}{T}$	Temperature Output Voltage Drift			− 0.5		mV/°C

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SVR	Supply Volt. Rej.	I_o = 350mA ; f = 120Hz C_o = 100µF ; V_i = 12V ± $5V_{pp}$	50	60		dB
I_{sc}	Output Short Circuit Current		0.50	0.80	1.50	A
V_R	Reset Output Saturation Voltage	1.5V < V_o < $V_{RT\ (off)}$, I_R = 1.6mA 3.0 < V < V_o < $V_{RT\ (off)}$, I_R = 8mA			0.40 0.40	V V
I_R	Reset Output Leakage Current	V_O in Regulation, V_R = 5V			50	µA
$V_{RT\ peak}$	Power On-Off Reset out Peak Voltage	1KΩ Reset Pull-up to V_o		0.65	1.0	V
$V_{RT\ (off)}$	Power OFF V_o Threshold	V_o @ Reset Out H to L Transition	4.75	V_o – 0.15		V
$V_{RT\ (on)}$	Power ON V_o Threshold	V_o @ Reset Out L to H Transition		$V_{RT\ (off)}$ + 0.05	V_o – 0.04	V
V_{Hyst}	Power ON-Off Hysteresis	$V_{RT\ (on)}$ – $V_{RT\ (off)}$		0.05		V
V_d	Delay Comparator Threshold	V_d @ Reset Out L to H Transition	3.65	4.00	4.35	V
		V_d @ Reset Out H to L Transition	3.20	3.55	3.90	V
V_{dH}	Delay Comparator Hysteresis			0.45		V
I_d	Delay Capacitor Charging Current	V_d = 3V, T_J = 25°C		20		µA
V_{disch}	Delay Capacitor Discharge Voltage	V_o < $V_{RT\ (off)}$		0.55	1.20	V
T_d	Power on Reset Delay Time	C_d = 100nF, T_J = 25°C	10	20	30	ms

(*) For a DC voltage 26 < V_i < 35V the device is not operating.

TEST CIRCUIT



(*) Min 20µF, ESR < 10Ω over full temperature range
R_P (pull up resistor) and R_L (load) are both equal to 1kΩ.

FUNCTIONAL DESCRIPTION

The L4947 is a very low drop 5V/0.5A voltage regulator provided with a reset function and therefore particularly suited to meet the requirements of supplying the microprocessor systems used in automotive and industrial applications.

The block diagram shows the basic structure of the device : the reference, the error amplifier, the driver, the power PNP, the protection and reset functions.

The power stage is a Lateral PNP transistor which allows a very low dropout voltage (typ. 400mV at T_J = 25°C, max. 750mV over the full temperature range @ I_O = 500mA). The typical curve of the dropout voltage as a function of the junction temperature is shown in Fig. 1 : that is the worst case, where I_O = 500mA.

The current consumption of the device (quiescent current) is maximum 13mA - over full T - when no load current is required.

The internal antisaturation circuit allows a drastic reduction in the current peak which takes place during the start up.

The reset function supervises the regulator output voltage inhibiting the microprocessor when the device is out of regulation and resetting it at the power-on after a settable delay. The reset is LOW when the output voltage value is lower than the reset threshold voltage. At the power-on phase the output voltage increases (see Fig. 2) and - when it reaches the power-on V_O threshold V_{RT} (On) - the reset output becomes HIGH after a delay time set by the external capacitor C_d. At the power-off the output voltage decreases : at the $V_{RT(Off)}$ threshold value (V_O-0.15V typ. value) the reset output instantaneously goes down (LOW status) inhibiting the microprocessor. The typical power on-off hysteresis is 50mV.

The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (C_{omin} = 20µF) to guarantee the global stability of the system.

Load dump and field decay protections (± 80V), reverse voltage (– 18V) and short circuit protection, thermal shutdown are the main features that make the L4947 specially suitable for applications in the automotive enviroment.

Figure 1 : Typical Dropout Voltage vs. T_j (I_o = 500mA).

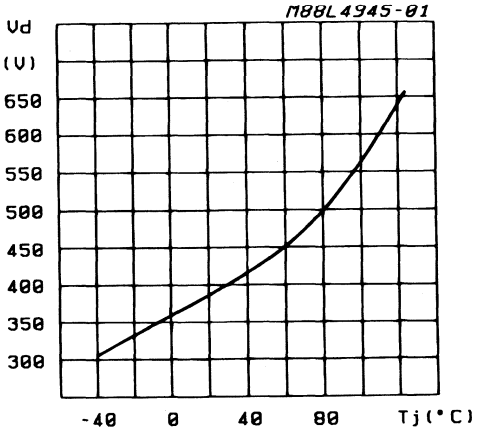
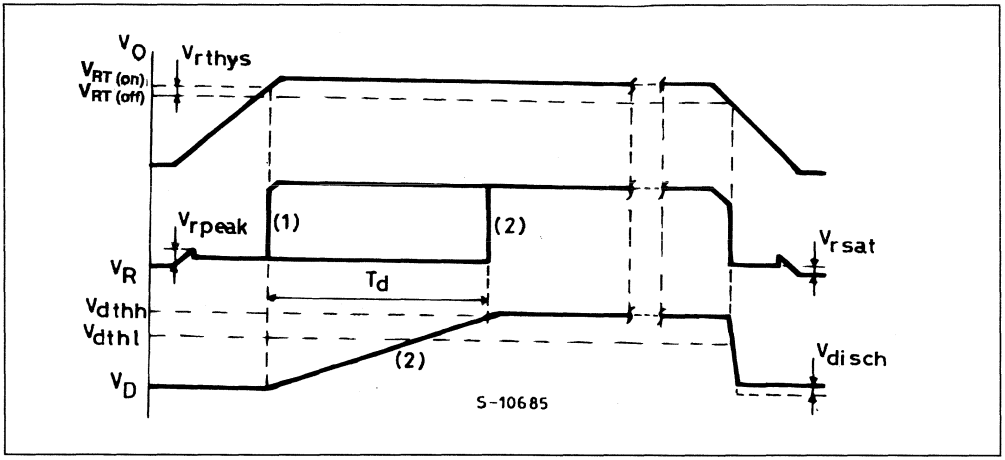
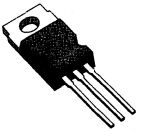


Figure 2 : Reset Waveforms : (1) Without External Capacitor C_d.
(2) With External Capacitor C_d.



VERY LOW DROP VOLTAGE REGULATOR

- OUPUT CURRENT IN EXCESS OF 400mA
- INPUT/OUTPUT DROP TYP. 0.25V at 150mA OVER FULL TEMPERATURE RANGE
- OVERVOLTAGE PROTECTION (± 40V)
- REVERSE POLARITY PROTECTION
- FOLDBACK CURRENT LIMITING
- THERMAL SHUTDOWN
- VERY LOW QUIESCENT CURRENT



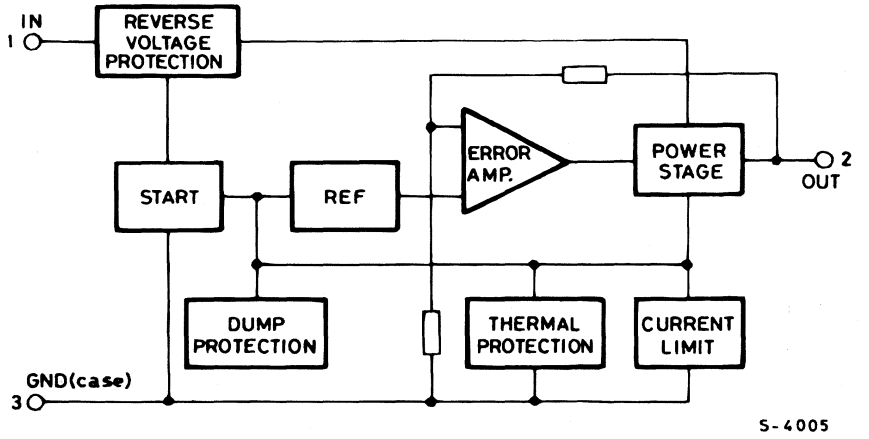
TO 220

ORDER CODE : LM2930A

DESCRIPTION

The LM2930A is an improved version of the LM2930 5V voltage regulator which features an output current rating of 400mA with a dropout voltage of 0.4V typ. (T_j = 25°C). At 150mA the dropout voltage falls to 0.2V. Moreover, the LM2930A includes ± 40V input overvoltage protections plus reverse polarity protection, thermal shutdown and foldback current limiting. Designed primarily for automotive applications, the LM2930A protects both itself and the load from load dump field decays transients and incorrect battery connection. The low voltage drop of this device allows correct operation even during starting when the battery voltage can fall below 6V. The LM2930A is available in a T0-220 plastic power package.

BLOCK DIAGRAM



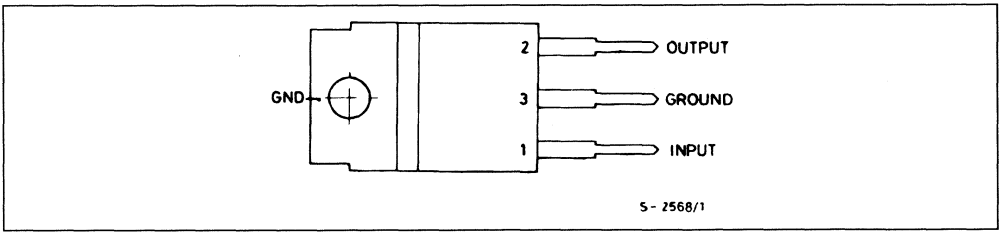
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage	35	V
	DC Input Reverse Voltage	– 18	V
	Transient Input Overvoltage : Load Dump : 5ms ≤ T_{rise} ≤ 10ms, τ_f Fall Time Constant = 100ms, R_{source} ≥ 0.5Ω	+ 40	V
	Field Decay : 5ms ≤ t_{fall} ≤ 10ms t_r Rise Time Constant = 33ms, R_{source} ≤ 10Ω	– 40	V
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W

PIN CONNECTION (top view)

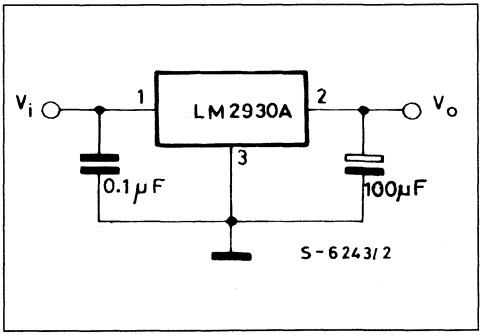


TEST AND APPLICATION CIRCUIT

The output capacitor is required for stability. Though the 100 µF shown is the minimum recommended value, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperature expected in the system. Many aluminum type electrolytics will freeze at temperatures less than – 30 °C, reducing their effective capacitance to zero. To maintain regulator stability down to – 40 °C, capacitors rated at that temperature (such as tantalums) must be used.



ELECTRICAL CHARACTERISTICS (V_i = 14.4 V, Co = 100 µF, T_j = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	6 V ≤ V_i ≤ 26 V (*), 5 mA ≤ I_o ≤ 400 mA	4.80	5.00	5.20	V
ΔV_o	Line Regulation	6 V ≤ V_i ≤ 26 V, I_o = 5 mA		5	50	mV
ΔV_o	Load Regulation	5 mA ≤ I_o ≤ 400 mA		15	75	mV
R_o	Output Impedance	100 mA_{DC} & 10 mArms, 100 Hz – 10 KHz		200		mΩ
I_d	Quiescent Current	I_o = 5 mA I_o = 150 mA		0.8 22	2 40	mA mA
e_N	Output Noise Voltage	10 Hz – 100 KHz		140		µVrms
LTS	Long Term Stability			20		mV/1000 hr
SVR	Supply Voltage Rejection	f_o = 120 Hz $V_i = V_o$ + 3 V + 2 V_{PP} Co = 100 µF		60		dB
I_o	Current Limit			800		mA
$V_i - V_o$	Dropout Voltage	I_o = 150 mA I_o = 400 mA		0.2 0.4	0.4 0.7	V V
I_{SC}	Output Short Circuit Current (foldback condition)			350	500	mA

⊗ **Note :** For a DC voltage 26 V < Vi < 35 V the device is not operating

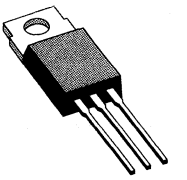
ELECTRICAL CHARACTERISTICS (V_i = 14.4 V, C_O = 100 µF, – 40 ≤ T_j ≤ 125 °C (see note1) unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	6.5 V ≤ Vi ≤ 26 V, 5 mA ≤ I_o ≤ 400 mA	4.70	5.00	5.30	V
ΔV_o	Line Regulation	6.5 V ≤ V_i ≤ 26 V, I_o = 5 mA		10	75	mV
ΔV_o	Load Regulation	5 mA ≤ I_o ≤ 400 mA		22	110	mV
I_d	Quiescent Current	I_o = 5 mA I_o = 150 mA		1.2 40	3 70	mA mA
I_o	Current Limit			870		mA
$V_i - V_o$	Dropout Voltage	I_o = 150 mA I_o = 400 mA		0.25 0.5	0.5 0.9	V V
I_{sc}	Output Short Circuit Current (foldback condition)			230		mA

Note : 1. Design limits are guaranteed by statistical control on production samples over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

VERY LOW DROP VOLTAGE REGULATOR

- OUTPUT CURRENT IN EXCESS OF 400mA
- INPUT/OUTPUT DROP TYP. 0.2 V AT 150mA
- OVERVOLTAGE PROTECTION (± 60 V)
- REVERSE POLARITY PROTECTION
- FOLDBACK CURRENT LIMITING
- THERMAL SHUTDOWN
- VERY LOW QUIESCENT CURRENT



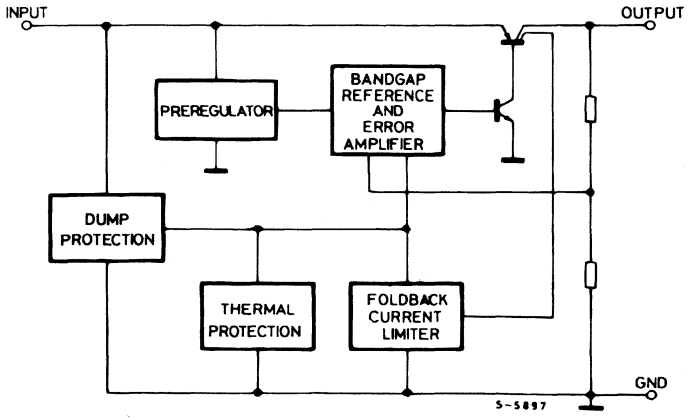
TO-220

ORDER CODE : LM2931A

DESCRIPTION

The LM2931A is an improved version of the LM2931 5 V voltage regulator which features an output current rating of 400mA with a dropout voltage of 0.4V typ. (T_j = 25 °C). At 150mA the dropout voltage falls to 0.2V. A special feature of this device is the low quiescent current of 2mA at 10mA output current which makes it ideal for standby and backup applications. Designed for automotive applications, the LM2931A protects itself and the load from ± 60V load dump and field decay transients and battery reversal. It also includes a thermal shutdown circuit and a foldback current limiter. The low voltage drop of the LM2931A allows correct operation of 5V automotive equipment during starting when the battery voltage can fall below 6V. The LM2931A is available in a TO-220 plastic power package.

BLOCK DIAGRAM



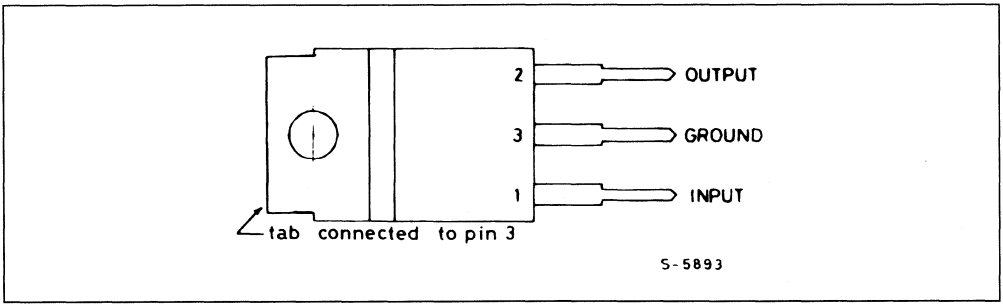
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage	35	V
	DC Input Reverse Voltage	– 18	V
	Transient Input Overvoltage : Load Dump : 5ms ≤ T_{rise} ≤ 10ms, τ_f Fall Time Constant = 100ms, R_{source} ≥ 0.5Ω	+ 60	V
	Field Decay : 5ms ≤ t_{fall} ≤ 10ms t_r Rise Time Constant = 33ms, R_{source} ≤ 10Ω	– 60	V
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

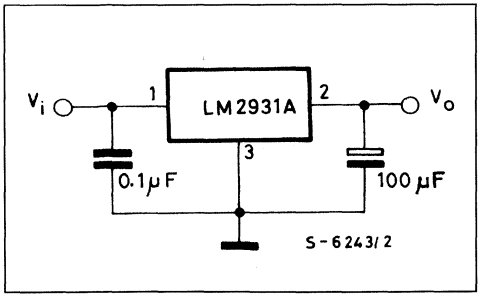
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	4	°C/W

PIN CONNECTIONS (top view)



TEST AND APPLICATION CIRCUIT



The output capacitor is required for stability. Though the 100 µF shown is the minimum recommended value, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperature expected in the system. Many aluminum type electrolytics will freeze at temperatures less than – 30°C, reducing their effective capacitance to zero. To maintain regulator stability down to – 40°C, capacitors rated at that temperature (such as tantalums) must be used.

ELECTRICAL CHARACTERISTICS (V_I = 14.4V, C_O = 100µF, T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	6V ≤ V_i ≤ 26V, 5mA ≤ I_o ≤ 400mA	4.80	5.00	5.20	V
ΔV_o	Line Regulation	6V ≤ V_I ≤ 26V, I_o = 5mA		5	50	mV
ΔV_o	Load Regulation	5mA ≤ I_o ≤ 400mA		15	75	mV
R_o	Output Impedance	100mA$_{DC}$ & 10mArms, 100Hz - 10KHz		 200		 mΩ
I_d	Quiescent Current	I_o = 5mA I_o = 150mA		0.8 22	2 40	mA mA
e_N	Output Noise Voltage	10Hz - 100KHz		140		µVrms
LTS	Long Term Stability			20		mV/ 1000 hr
SVR	Supply Voltage Rejection	f_o = 120Hz, V_i = V_o + 3V + 2V_{PP} C_o =100µF		60		dB
I_o	Current Limit			800		mA
V_i-V_o	Dropout Voltage	I_o = 150mA I_o = 400mA		0.2 0.4	0.4 0.7	V V
I_{sc}	Output Short Circuit Current (foldback condition)			350	500	mA

ELECTRICAL CHARACTERISTICS (V_I = 14.4V, C_O = 100µF, 40 ≤ T_j ≤ 125°C (see note 1) unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	6.5V ≤ V_i ≤ 26V,(see note 2), 5mA ≤ I_o ≤ 400mA	4.70	5.00	5.30	V
ΔV_o	Line Regulation	6.5V ≤ V_I ≤ 26V, I_o = 5mA		10	75	mV
ΔV_o	Load Regulation	5mA ≤ I_o ≤ 400mA		22	110	mV
I_d	Quiescent Current	I_o = 5mA I_o = 150mA		1.2 40	3 70	mA mA
I_o	Current Limit			870		mA
V_i-V_o	Dropout Voltage	I_o = 150mA I_o = 400mA		0.25 0.5	0.5 0.9	V V
I_{sc}	Output Short Circuit Current (foldback condition)			230		mA

Notes : 1. Design limits are guaranteed by statistical control on production samples over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.
2. For a DC voltage 26V < Vi < 35V the device is not operating.

SGS-THOMSON MICROELECTRONICS

SGSD93E
SGSD93F
SGSD93G

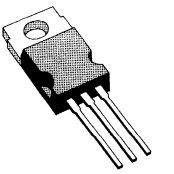
EPITAXIAL PLANAR NPN

ADVANCE DATA

- DAMPER DIODE

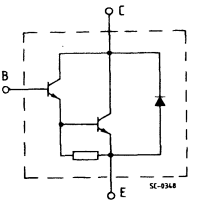
AUTOMOTIVE

- SWITCHING APPLICATION



TO-220

INTERNAL SCHEMATIC DIAGRAM



DESCRIPTION

The SGSD93E/93F/93G are silicon epitaxial planar NPN transistors in Darlington configuration mounted in Jedec TO-220 plastic package.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		SGSD93E	SGSD93F	SGSD93G	
V_{CBO}	Collector-base Voltage (I_E = 0)	160	180	200	V
V_{CES}	Collector-emitter Voltage (V_{BE} = 0)	140	160	180	V
V_{CEO}	Collector-emitter Voltage (I_B = 0)	140	160	180	V
V_{EBO}	Emitter-base Voltage (I_C = 0)	5			V
I_C	Collector Current	12			A
I_{CM}	Collector Peak Current	15			A
I_B	Base Current	0.2			A
P_{tot}	Total Dissipation at T_c < 25 °C	80			W
T_{stg}	Storage Temperature	– 65 to 150			°C
T_j	Max. Operating Junction Temperature	150			°C

THERMAL DATA

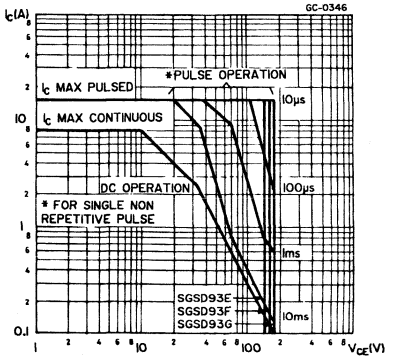
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.56	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

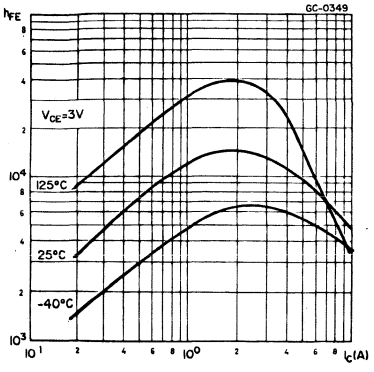
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cutoff Current (I_E = 0)	V_{CB} = 160 V for **SGSD93E** V_{CB} = 180 V for **SGSD93F** V_{CB} = 200 V for **SGSD93G**			50 50 50	µA µA µA
		V_{CB} = 160 V for **SGSD93E** V_{CB} = 180 V for **SGSD93F** V_{CB} = 200 V for **SGSD93G** T_c = 150 °C			2 2 2	mA mA mA
I_{CEO}	Collector Cutoff Current (I_B = 0)	V_{CE} = 140 V for **SGSD93E** V_{CE} = 160 V for **SGSD93F** V_{CE} = 180 V for **SGSD93G**			0.5 0.5 0.5	mA mA mA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{BE} = – 5 V			0.1	mA
$V_{CEO(sus)}$*	Collector-emitter Sustaining Voltage	I_C = 0.1 A for **SGSD93E** for **SGSD93F** for **SGSD93G**	140 160 180			V V V
$V_{CE(sat)}$*	Collector-emitter Saturation Voltage	I_C = 5 A I_B = 5 mA I_C = 10 A I_B = 20 mA I_C = 5 A I_B = 5 mA T_c = 150 °C I_C = 10 A I_B = 20 mA T_c = 150 °C I_C = 5 A I_B = 5 mA T_c = – 40 °C			1.4 2.0 1.4 2.2 1.6	V V V V V
$V_{BE(sat)}$*	Base-emitter Saturation Voltage	I_C = 5 A I_B = 5 mA I_C = 10 A I_B = 20 mA I_C = 5 A I_B = 5 mA T_c = 150 °C I_C = 5 A I_B = 5 mA T_c = – 40 °C			2.0 2.8 2.0 2.2	V V V V
h_{FE}*	DC Current Gain	I_C = 150 mA V_{CE} = 1 V I_C = 3 A V_{CE} = 3 V I_C = 5 A V_{CE} = 3 V I_C = 10 A V_{CE} = 3 V	500 1000 1000 750		 20000 	
V_F*	Diode Forward Voltage	I_F = 5 A I_F = 10 A			1.8 3.0	V V
h_{fe}	Small Signal Current Gain	I_C = 1 A V_{CE} = 5 V f = 5 MHz		25		
	RESISTIVE LOAD					
t_{on} t_s t_f	Turn-on Time Storage Time Fall Time	I_C = 6 A I_{B1} = – I_{B2} = 24 mA V_{CC} = 30 V	500 1.4 1.5	700 3.2 2.5	1100 5.0 4.5	ns µs µs

* Pulsed : pulsed duration = 300 µs, duty cycle = 1.5 %.

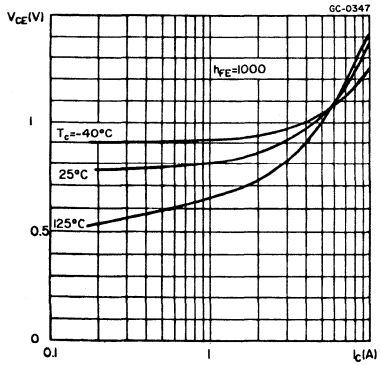
Safe Operating Areas.



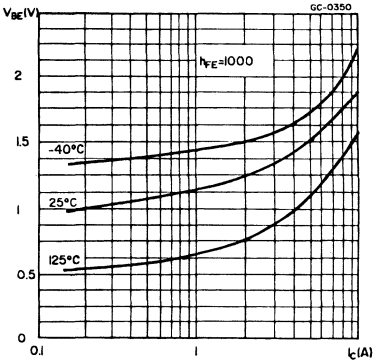
DC Current Gain.



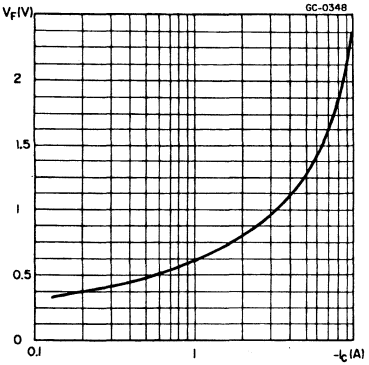
Collector-emitter Saturation Voltage.



Base-emitter Saturation Voltage.



Emitter-collector Voltage.



SUPPLY VOLTAGE SUPERVISORS

- POWER-ON RESET GENERATOR
- AUTOMATIC RESET GENERATION AFTER VOLTAGE DROP
- WIDE SUPPLY VOLTAGE RANGE ... 3 V TO 18 V
- PRECISION VOLTAGE SENSOR
- TEMPERATURE-COMPENSATED VOLTAGE REFERENCE
- TRUE AND COMPLEMENT RESET OUTPUTS
- EXTERNALLY ADJUSTABLE PULSE WIDTH

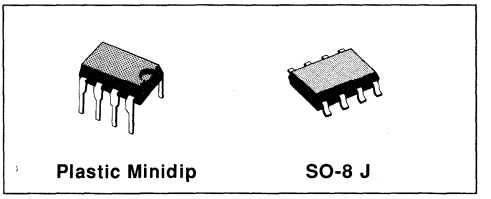
DESCRIPTION

The TL7700A series are monolithic integrated circuit supply voltage supervisors specifically designed for use as reset controllers in microcomputer and microprocessor systems. During power-up the device tests the supply voltage and keeps the RESET and $\overline{\text{RESET}}$ outputs active (high and low, respectively) as long as the supply voltage has not reached its nominal voltage value. Taking $\overline{\text{RESIN}}$ low has the same effect. To ensure that the microcomputer system has reset, the TL7700A then initiates an internal time delay that delays the return of the reset outputs to their inactive states. Since the time delay for most microcomputers and microprocessors is in the order of several machine cycles, the device internal time delay is determined by an external time delay is determined by an external capacitor connected to the C_T input (pin 3).

$t_d = 1.3 \times 10^4 \times C_T$

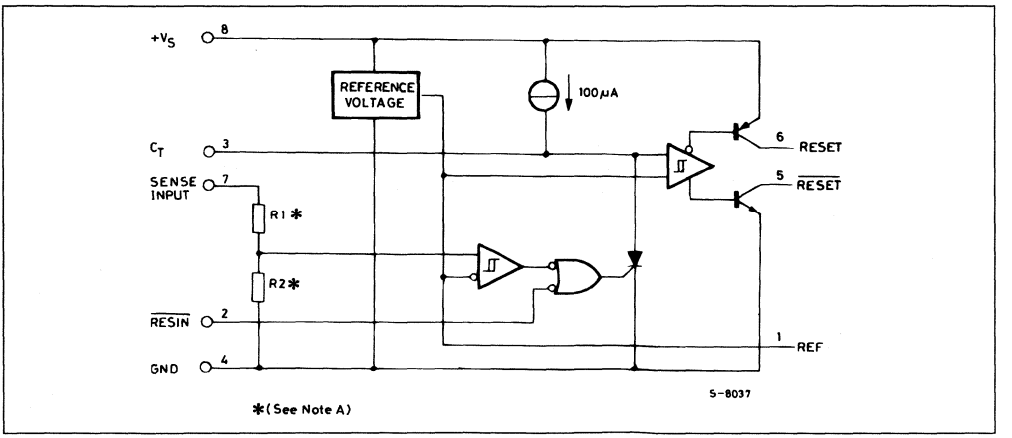
Where : C_T is in farads (F) and t_d in seconds (s). In addition, when the supply voltage drops below the nominal value, the outputs will be active until the supply voltage returns to the nominal value. An external capacitor (typically 0.1 µF) must be connected to the REF output (pin 1) to reduce the influence of fast transients in the supply voltage.

The TL7700AI series is characterized for operation from – 25°C to 85°C ; the TL7700AC series is characterized from 0°C to 70°C.



Plastic Minidip **SO-8 J**

BLOCK DIAGRAM



* TL7702A R1 = 0Ω, R2 = open ; TL7705A R1 = 7.8 KΩ, R2 = 10 KΩ ; TL7709A R1 = 19.7 KΩ, R2 = 10 KΩ ; TL7712A R1 = 32.7 KΩ, R2 = 10 KΩ ; TL7715A R1 = 43.4 KΩ, R2 = 10 KΩ.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage, V_{CC} (see note 1)	20	V
V_i	Input Voltage Range at $\overline{RESIN}$	– 0.3 to 20	V
V_i	Input Voltage at SENSE : TL7702A (see note 2)	– 0.3 to 6	V
	TL7705A	– 0.3 to 10	V
	TL7709A	– 0.3 to 15	V
	TL7712A	– 0.3 to 20	V
	TL7715A	– 0.3 to 20	V
I_{OH}	High-level Output Current at RESET	– 30	mA
I_{OL}	Low-level Output Current at $\overline{RESET}$	30	mA
T_{amb}	Operating Free-air Temperature Range : TL77XXAI	– 25 to 85	°C
	TL77XXAC	0 to 70	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

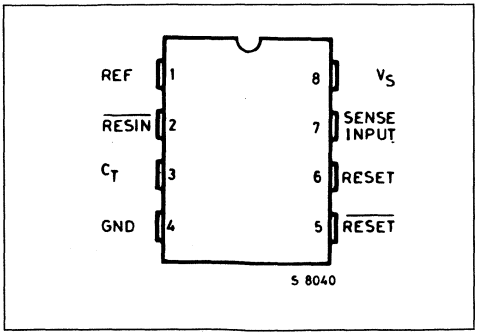
Notes : 1. All voltage values are with respect to the network ground terminal.
2. For the TL7700A, the voltage applied to the SENSE terminal must never exceed V_S.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min.	Max.	Unit
V_S	Supply Voltage		3.6	18	V
V_{IH}	High-level Input Voltage at RESIN		2		V
V_{IL}	Low-level Input Voltage at RESIN			0.6	V
V_i	Voltage at Sense Input	TL7702A	0	See Note 3	V
		TL7705A	0	10	
		TL7709A	0	15	
		TL7712A	0	20	
		TL7715A	0	20	
I_{OH}	High-level Output Current at RESET			– 16	mA
I_{OL}	Low-level Output Current at $\overline{RESET}$			16	mA
T_{amb}	Operating Free-air Temperature Range	TL77 - AI	– 25	85	°C
		TL77 - AC	0	70	

Note : 3. For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_S – 1 V or 6 V, whichever is less.

CONNECTION DIAGRAM AND ORDER CODE



Temperature Range	Plastic Minidip	SO-8
Commercial 0 to 70 °C	TL77XXACP	TL77XXACD
Industrial – 40 to 85 °C	TL77XXAIP	TL77XXAID

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	120	°C/W

ELECTRICAL CHARACTERISTICS these specifications unless otherwise specified, apply for : T_{amb} = – 25 to 85 °C (TLXXAI) ; T_{amb} = 0 to 70 °C (TL77XXAC)

Symbol	Parameter		Test Conditions (1)	Min.	Typ.	Max.	Unit
V_{OH}	High-level Output Voltage at $\overline{RESET}$		I_{OH} = – 16 mA	V_S–1.5			V
V_{OL}	Low-Level Output Voltage at $\overline{RESET}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference Voltage		T_{amb} = 25 °C	2.48	2.53	2.58	V
V_T	Threshold Voltage at SENSE Input	TL7702A	V_S = 3.6 V to 18 V T_{amb} = 25 °C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11.0	
		TL7715A		13.2	13.5	13.8	
V_T	Threshold Voltage at SENSE Input	TL7702A	V_S = 3.6 V to 18 V	2.45	2.53	2.58	V
		TL7705A		4.45	4.55	4.6	
		TL7709A		7.4	7.6	7.7	
		TL7712A		10.4	10.8	11.0	
		TL7715A		13.0	13.5	13.8	
V_{T+}, V_{T-}	Hysteresis (2) at SENSE Input	TL7702A	V_S = 3.6 V to 18 V T_{amb} = 25 °C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input Current at $\overline{RESIN}$ Input		V_i = 2.4 V to V_S			20	µA
			V_I = 0.4 V			– 100	
I_I	Input Current at SENSE Input	TL7702A	$V_{ref} < V_i < V_S$ –1.5 V		0.5	2	
I_{OH}	High-level Output Current at $\overline{RESET}$		V_O = 18 V			50	
I_{OL}	Low-level Output Current at RESET		V_O = 0 V			– 50	
I_S	Supply Current		All Inputs and out. open		1.8	3.3	mA

Notes : 1. All characteristics are measured with C = 0.1 µF from Pin 1 to GND, and with C = 0.1 µF from Pin 3 to GND.
2. Hysteresis is the difference between the positive going input threshold voltage. V_{T+}, and the negative going input threshold voltage, V_{T-}.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{pi}	Pulse Width at SENSE Input	$V_{ih} = V_{ityp} + 0.04 \times V_i$ $V_{iL} = V_{ityp} - 0.04 \times V_i$	0.9			µs
t_{pi}	Pulse Width at $\overline{RESIN}$ Input		0.4			µs
t_{po}	Pulse Width at Output	$C_f = 0.1$ µF	0.65	1.3	2.6	ms
t_{pdHL}	Propagation Delay Time from $\overline{RESIN}$ to $\overline{RESET}$	$C_L = 100$ pF $V_S = 5$ V $R_L = 4.7$ KΩ			1	µs
$t_{r/f}$	Rise/Falltime at $\overline{RESET}$ and $\overline{RESET}$	$C_L = 10$ pF $V_S = 5$ V $R_L = 4.7$ KΩ			1	µs

Figure 1 : Multiple Power Supply System Reset Generation.

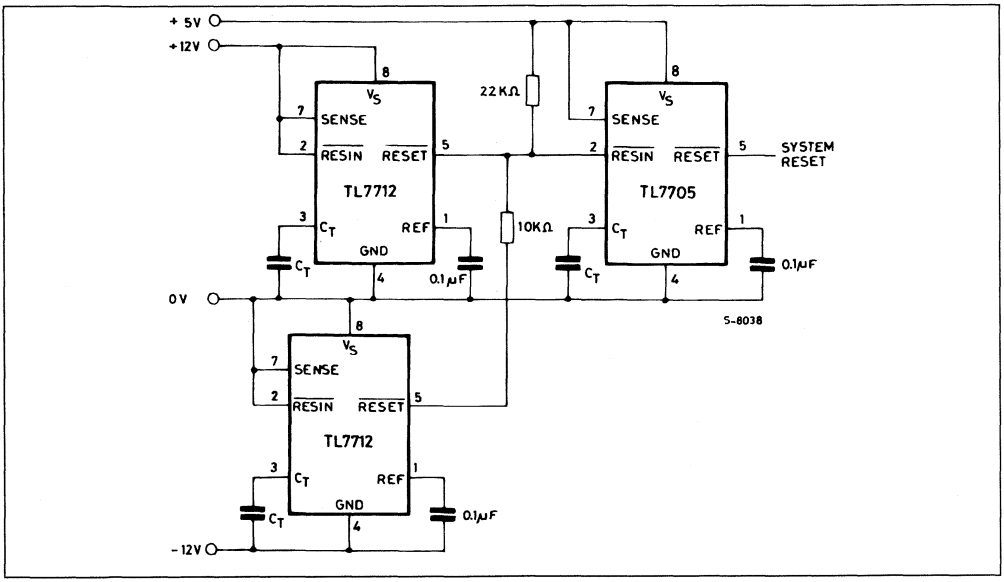
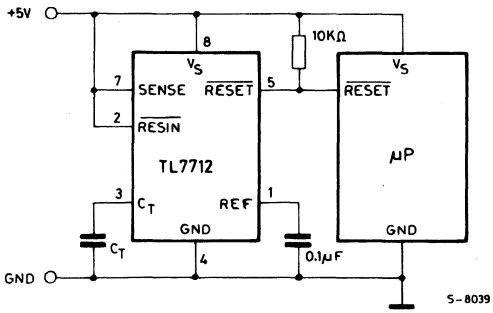


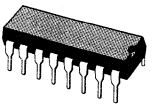
Figure 2 : Reset Controller for µP.



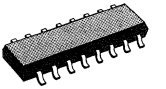
CAR ALTERNATOR REGULATOR

PRELIMINARY DATA

- ALTERNATOR VOLTAGE CONTROL
- COMPLETE FAULT DIAGNOSTICS
- INTERNAL DRIVER FOR 3W LAMP
- LAMP SHORT CIRCUIT PROTECTION
- SENSING INTERRUPT PROTECTION
- 100V DUMP PROTECTION
- 300V LOW ENERGY SPIKE PROTECTION
- THERMAL PROTECTION



DIP-16



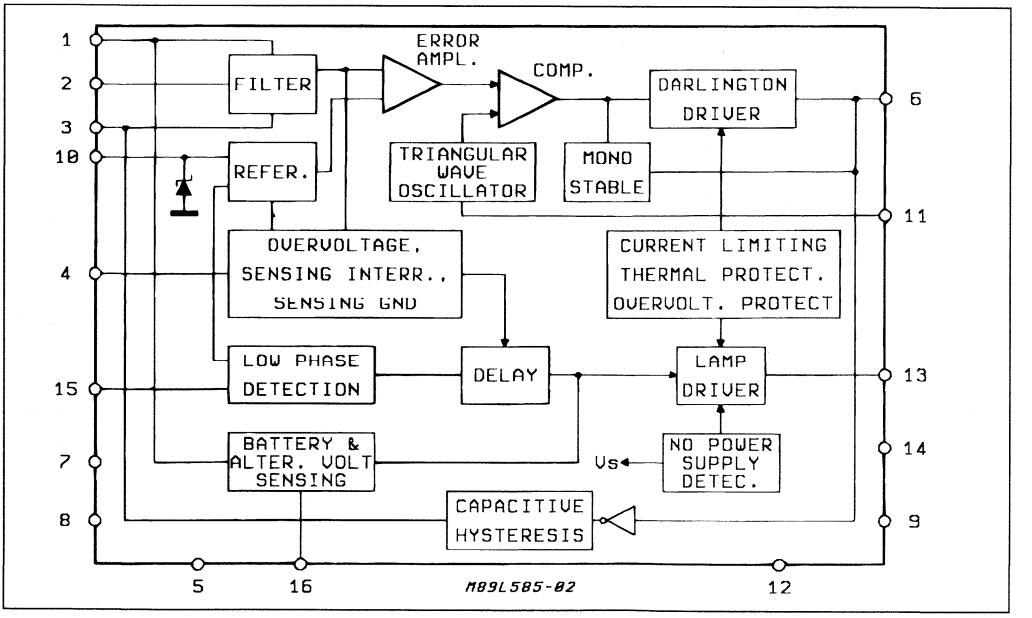
SO-16J

ORDER CODES : L585 (DIP-16)
L585D1 (SO-16)

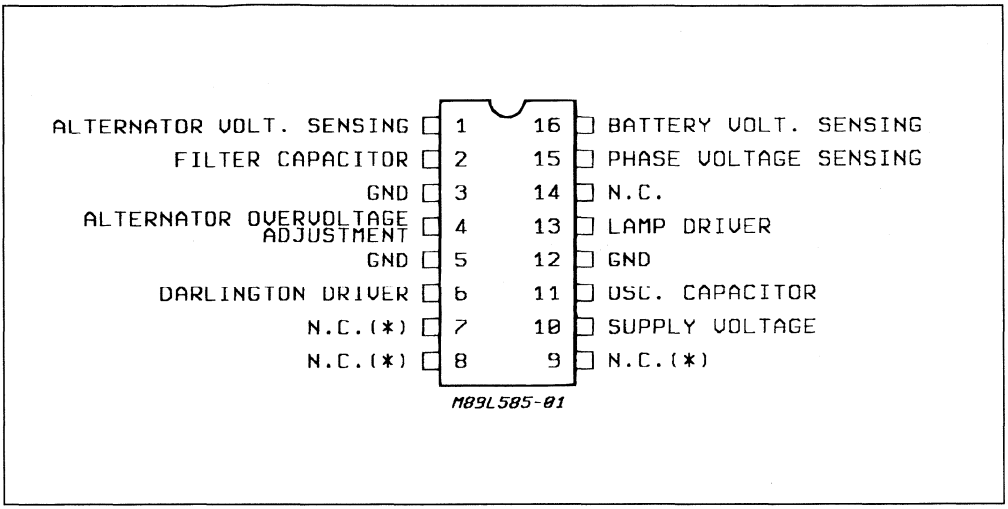
DESCRIPTION

The L585 is an integrated circuit designed for use with an external NPN darlington as a voltage regulator in a threephase alternator charging system. It includes fault diagnostic circuitry which drives a 3W warning lamp in fault conditions such as open or short circuit connections. Protection against load dump transients, short circuits and low energy spikes is incorporated.

BLOCK DIAGRAM



PIN CONNECTIONS (top view).



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_S	D. C. Supply Current Pulse " " (5ms ≤ t_{rise} ≤ 10ms, τ_f fall time constant = 100ms)	200 600	mA mA
V_1, V_{13} (*), $V1_6$	D. C. Voltages Transient Voltages : Load Dump : 5ms ≤ t_{rise} ≤ 10ms, τ_f = 100ms, R_{SOURCE} ≥ 0.5Ω Low Energy Spikes : t_{rise} = 100µs, τ_{fall} = 300µs, R_{SOURCE} = 800Ω	30 100 200	V V V
I_{13}	Lamp Driver Current (ON state)	int. limited	
T_j, T_{STG}	Junction and Storage Temperature Range	– 55 to 150	°C
P_D	Power Dissipation at T_{amb} = 80°C	875	mW

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (*) for DIP 16	Max	80	°C/W
$R_{th\ j\text{-}alumina}$(*)	Thermal Resistance Junction-alumina for SO-16	Max	50	°C/W

Note : Soldered on PC board that simulates an application with medium device density on board.

(*) Thermal resistance junction-pins with the chip soldered on the middle of an alumina supporting substrate measuring 15 ö 20 mm ; 0.65 mm thickness and infinite heathsink.

PIN FUNCTIONS

N°	Name	Functions
1	Alternator Voltage Sensing	Connection for voltage regulation sensing. V_{ALT} can be changed modifying R_1 value. The regulation sensitivity is a function of R1 and is given by : $S = \frac{\Delta V_{ALT}}{\Delta R1} = 0.5mV/\Omega$
2-3	Filter Capacitor	A capacitor connected between these two pins filters the feedback signal from the regulated output and provides a capacitive hysteresis to avoid spurious switchings of the external darlington. Typically the input impedance is 15KΩ.
4	Alternator Overvoltage Adjustment	When this pin is left floating the overvoltage threshold is a described in the specification. Typically the warning lamp is switched on when the voltage at this pin is greater than 3.5V. This threshold can be modified with a resistor between either the ground or pin 2.
5	GND	This pin must be connected to ground.
6	Darlington Driver	The internal open collector stage disables in PWM mode the external power darlington.
7-8-9	N.C.	These pins must be left floating.
10	IC Supply Voltage	Supply Voltage Input A 7.5V (typical) Zener is present at the input.
11	Oscillator Capacitor	A capacitor connected to ground sets the frequency of the internal oscillator. The frequency is given by : $f_{osc} = \frac{20 \times 10^{-6}}{8.4 \times C_{osc}}$
12	GND	This pin must be connected to ground.
13	Lamp Driver	Driver for External Alarm Lamp Internally protected agains short circuit (current limiting), load dump transients and, by means of a zener, against low energy spikes.
14	NC	Not connected.
15	Phase Voltage Sensing.	Connection for no charge sensing from the alternator . The internal low threshold is typically 2.4V. By means of the external divider R3/R4 the threshold can be adjusted to give the required sensitivity.
16	Battery Voltage Sensing	Connection for Voltage Battery Sensing This pin senses a failure of the alternator-battery lead as the voltage difference V_{ALT}-V_{BAT}. The external resistor R2 limits the current in overvoltage protection.

ELECTRICAL CHARACTERISTICS (V_s = 14.4V ; – 30°C ≤ T_j ≤ 100°C unless otherwise specified ; refer to application circuit)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
REGULATION						
V_S	Operating Supply Voltage		6		25	V
I_d	Quiescent Drain Current (pin 10)	V_{10} = 5.5V			24	mA
V_{ALT}	Alternator Reg. Voltage	T_j = 20°C, 100ms After Ignition R_1 = 1.3KΩ (1) T_j = – 30°C T_j = + 100°C	14.26 14.60 13.32	14.55	14.84 15.50 14.17	V V V
ΔV_{ALT}	Voltage Reg. Range	10% < d < 90%		± 60		mV
S	Sensitivity to R_1 Variation	$S = dV_{ALT}/dR_1$	0.35		0.65	mV/Ω
TC_{nS}	Normalized S Temperature Coeff.	1/S* dS/dT		– 2000		ppm/°C
$V_{6\ sat}$	Darlington Driver Satur. Voltage	I_6 = 20mA			200	mV
f_s	Oscillation Frequency	C_{osc} = 20nF	80		170	Hz
I_1	Standby Current (pin 1)	V_{batt} = 12V			2	mA
DIAGNOSTIC						
V_{AH}	Overcharging Voltage Threshold (2)	T_j = 25°C R_1 = 1.3KΩ $V_S = V_{AH}$ (3) – 30°C < T_j < + 100°C	1.054V_A 1.049V_A		1.086V_A 1.091V_A	V V
V_{PL}	Low Level Phase Voltage Threshold (no load) (4)	T_j = 25°C – 30°C < T_j < + 100°C	5 4.5	6 6	7 7.5	V V
V_{AS}	Difference Between Altern. and Supply Voltage (5)	T_j = 25°C – 30°C < T_j < + 100°C	2.33 2.00	3.10 3.31	3.88 4.18	V V
$V_{1\ 3\ sat}$	Lamp Driver Saturation Voltage	$I_{1\ 3}$ = 250mA			1.5	V
$V_{1\ 3\ off}$	Lamp Driver Voltage Without Power Supply (6)				4.5	V
t_d	Alarm Delay	C_{osc} = 20nF	70		1.50	s

Notes : 1. d = 50 % the duty cycle of the output signal at pin 6.
2. The lamp is switched on with a fixed delay when the alternator voltage becomes higher than V_{AH}. (overcharge indication).
3. Measured 100 ms after turn-on.
4. The lamp is switched on with a fixed delay when the voltage V_p becomes lower than V_{PL} (the alternator is not charging the battery).
5. The lamp is switched on when the cable B is broken (V_{ALT} - V_S becomes higher than V_{AS}).
6. The lamp is switched on when the cable A is broken (IC without power voltage supply).
7. When the voltage at pin 1 is greater than $V_{1\ dp}$ the internal darlington for the lamp driving is switched off.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PROTECTION						
T_{sh}	Darlingtyon Thermal Shutdown Threshold		150			°C
V_{Zen}	(pin 10) Zener Voltage	I_O = 60mA I_O = 130mA	6 6.2		8 8.2	V V
V_{1dp}	Overvoltage Protection Threshold (7)	T_j = 25°C – 30°C < T_j < + 100°C	25 23	32	38 40	V V
$I_{13\,sc}$	Lamp Driver Circuit Current		300		1500	mA
I_{Z13}	Zener Capability Current during Low Energy Spikes	V_{13} = 110V@ T_j = 25°C V_1 = 50V@ τ_f = 100ms			200	mA
V_{Z13}	Zener Clamping Voltage	I_{13} = 100mA@ t = < 3ms	110			V
		I_{13} = 40mA@ t = < 6ms, 0 ≤ T_J ≤ 100 – 30°C ≤ T_J < 0	100 90			V V

Notes : 1. d = 50% the duty cycle of the output signal at pin 6.
2. The lamp is switched on with a fixed delay when the alternator voltage becomes higher than V_{AH}. (overcharge indication).
3. Measured 100ms after turn-on.
4. The lamp is switched on with a fixed delay when the voltage V_p becomes lower than V_{PL} (the alternator is not charging the battery).
5. The lamp is switched on when the cable B is broken (V_A - V_S becomes higher than V_{AS}).
6. The lamp is switched on when the cable A is broken (IC without power voltage supply).
7. When the voltage at pin 1 is greater than $V_{1\,dp}$ the internal darlington for the lamp driving is switched off.

CIRCUIT OPERATION

The L585 alternator regulator performs three main functions : regulation control fault diagnostics and protections.

REGULATION

The alternator voltage is compared with a reference voltage in an error amplifier (see block diagram), the output of which determines the duty cycle of the external darlington by comparison with the triangle wave form of the internal oscillator. This darlington switches the current in the excitation coil of the alternator.

The switching frequency is fixed and is set by the external capacitor C_{OSC} (see application circuit).

Capacitive positive feedback (C_F) and a monostable eliminate spurious switching caused by V_{ALT} output noise and voltage drop at pin 10 during the turn on of the external darlington.The base current delivered to the external darlington is set by the resistor R_B (see application circuit) and must be dimensioned according to the characteristics of this darlington and the maximum coil current.

DIAGNOSTIC

This circuit receives information from the battery, the alternator and one alternator phase. It indicates anomolous conditions by driving a 3W lamp. To prevent spurious fault warnings some indications are not displayed immediately but are delayed by a fixed time. No external components are needed to implement this delay since it is produced internally by dividing the internal oscillator with an eight-stage divider to give a delay of 128 periods. For a one second delay the oscillator frequency must be 128 Hz.

The lamp is driven after a delay when the following conditions occur : overcharging, phase low level (no charge) break or short circuit to GND in the alternator sense wire. In these two last cases the external darlington is switched off.

The diagnostic lamp is driven immediately when the cable connecting the alternator to the battery is broken (Va-Vbatt above 3.1 typ.) or when the IC is without power supply ($V_{CE\,sat}$ of the lamp driver is 2.4V typ. in this case). The external capacitor C_D, at pin 13, avoids spurious alarms at – 40°C.

PROTECTION

SHORT CIRCUIT PROTECTION

The integrated darlington is protected against short circuits of the lamp. The short circuit current is limited at 600mA and if this condition persistes thermal protection will intervene.

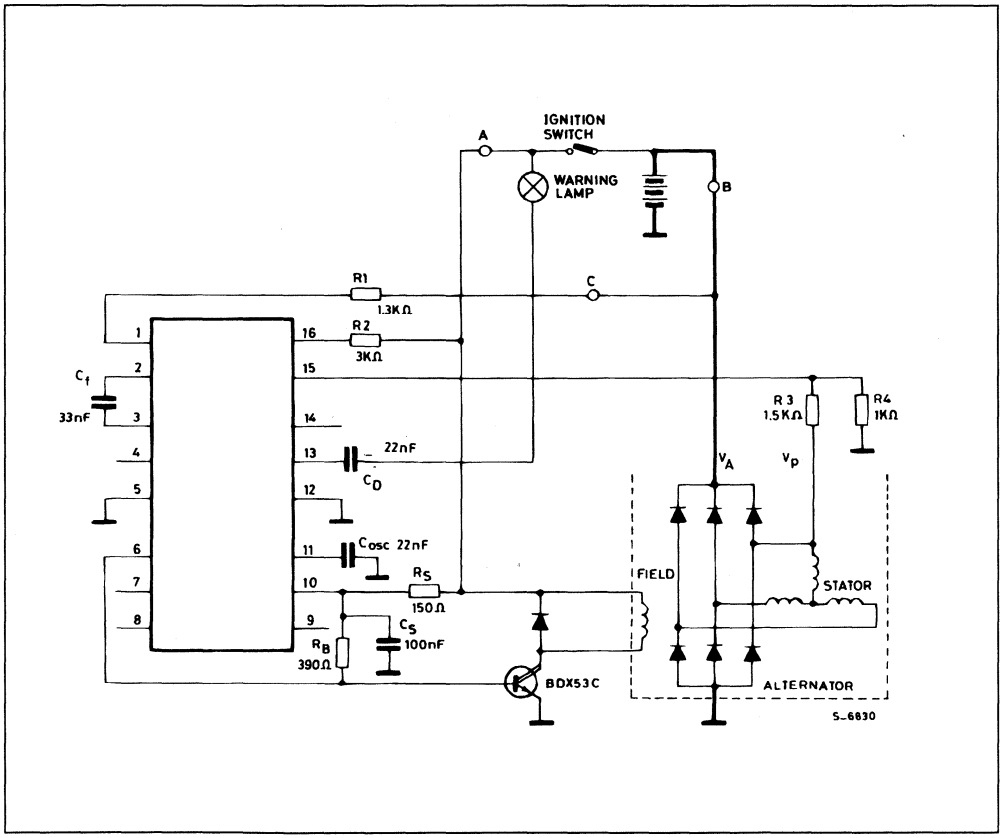
DUMP PROTECTION

The whole IC is protected against load dump transients (100V, 100ms fall time constant with a rise time within 5-10ms) in the typical application circuit. The only component to which this transient is directly applied (no series resistances) is the lamp driver darlington. During transients the darlington is kept off and can withstand peak voltages of 100V. Additionally, the IC can withstand low energy spikes up to 200V(t_{rise} = 100µs, τ_f = 300µs, R_{source} = 800 ohm). These spikes are clamped by an internal 100 V zener on the collector of the lamp driver darlington.

THERMAL PROTECTION

When the IC temperature reaches 170°C the lamp driver darlington is kept off.

Figure 1 : Application Circuit.



The device is able to withstand all the voltage transients mentioned in ISO DP7637/1. If voltage transients more severe than the above ISO standard have to be withstood, an external protection device (transil) must be connected between pin 15 and GND. For transients up to 250V, t_{pulse} = 500µs, R_{source} = 47Ω, the transil P6KE100P is recommended.

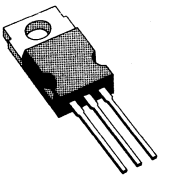
SGS-THOMSON MICROELECTRONICS

L9480VB

ONE CHIP CAR ALTERNATOR REGULATOR

ADVANCE DATA

- NO EXTERNAL COMPONENTS
- PRECISE TEMPERATURE COEFFICIENT
- PRECISE REGULATED VOLTAGE
- HIGH OUTPUT CURRENT
- SHORT CIRCUIT PROTECTED
- REVERSE BATTERY PROTECTION
- + 80 V LOAD DUMP PROTECTION
- LOW ENERGY SPIKE PROTECTION
- THERMAL SHUTDOWN
- VERY LOW START UP VOLTAGE



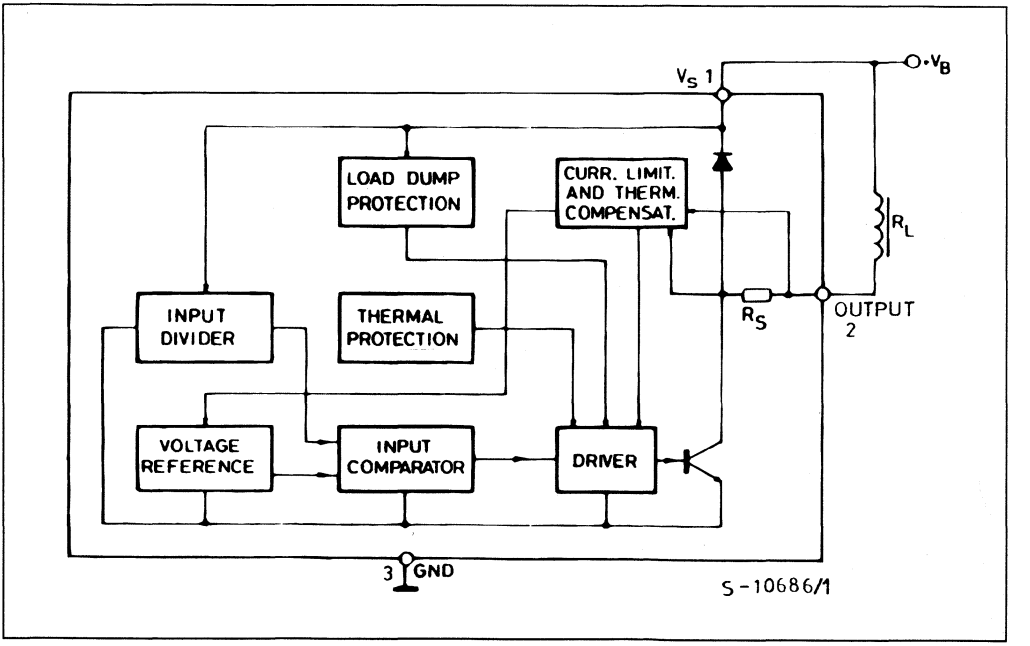
TO 220

ORDER CODE : L9480VB

DESCRIPTION

The L9480VB is a "single function" self-oscillating voltage regulator for car alternators. Integrating both the control section and the output power stage on a single chip, the L9480VB requires no external components, reducing significantly the cost of the system and increasing reliability.

BLOCK DIAGRAM



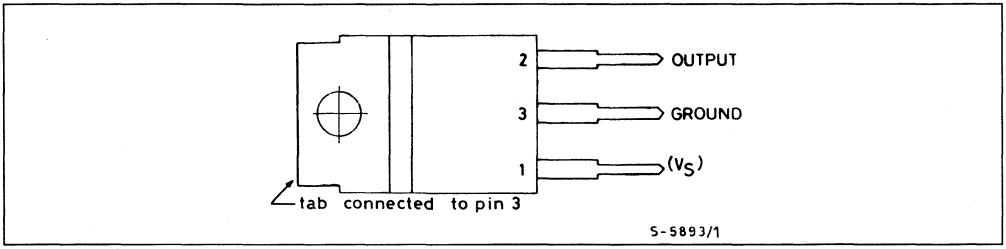
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Transient Overvoltage : Load Dump : 5ms ≤ T_{rise} ≤ 10ms τ_f Fall Time Constant ≤ 100ms, R_{source} ≥ 0.5Ω	80	V
I_{clamp}	Current into Low Energy Clamping Zener (T_{rise} = 5µs ; T_{decay} ≤ 2ms ; duty cycle ≤ 5%)	100	mA
I_{out}	Maximum Output Current	5	A
T_j , T_{stg}	Junction and Storage Temperature Range	– 55 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

PIN CONNECTIONS (top view)



DEVICE OPERATION

The alternator voltage, rectified by the auxiliary diode trio, is compared with an external reference and the resulting signal switches the output stage, driving the alternator field coil.

As the regulator is a self-oscillating type, the switching frequency depends on the whole system parameter set (including the alternator characteristics).

The regulator has an integrated filter in the voltage sensing path. Consequently it doesn't need -in the standard application- any external component.

Anyway an external capacitor (0.1 - 1µF) must be inserted between V_S and Ground guaranteeing the correct behaviour of the L9480VB when the rectifying diodes feature very high switching spikes that are not filtered by the device.

This external capacitor must also be used when the impedances of the cables connecting the alternator to the battery are so high to cause a superimposed ripple on the alternator voltage higher than 3-4V.

The L9480VB regulation voltage and the temperature coefficient may be independently set by suited metal mask selections ; furthermore the regulation voltage is trimmed within ± 1% of the nominal value @ 25°C.

The L9480VB has an unique -and patented- system to compensate the self-heating of the die due to the power dissipated in the output stage. In this way the internal reference voltage tracks the case temperature rather than the die one.

The L9480VB can withstand the reverse battery and the load dump (up to 80V) ; it can absorb, into the internal clamping zeners, low energy spikes up to a level of 100mA and its output is short circuit protected.

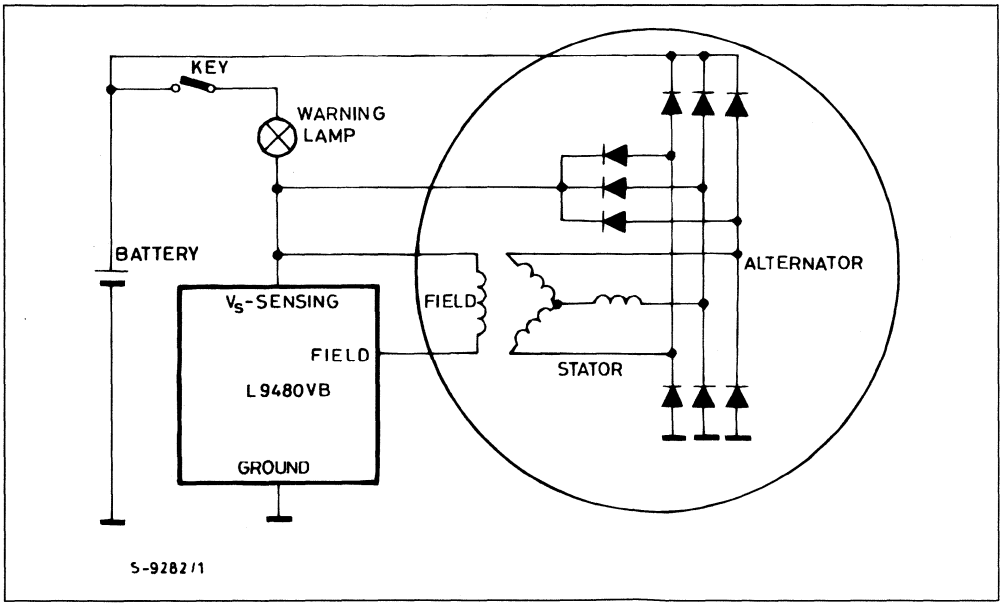
Finally the internal thermal shutdown avoids any possible device damage due to overtemperature problems.

ELECTRICAL CHARACTERISTICS(– 40 °C ≤ T_J ≤ 125 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_r	Regulation Voltage			14.4		V
eV_r	Error on Nominal Voltage	T_j = 25 °C		± 1	± 2	%
C_T	Temperature Coeff. of the Regulation Voltage			– 10		mV/°C
eC_T	Error on Nominal Temperature Coeff.			± 30		%
V_r	Load Regualtion	0.1 I_n < I_{alt} < 0.9 I_n (note 1)		250		mV
V_{su}	Control Circuit Minimum Start up Voltage	Measured at Supply Pin		2	3	V
V_{sd}	Shutdown Voltage (dump protection threshold)			22		V
$V_{sat\ 1}$	Output Saturation Voltage	I_{field} = 4 A_p		1.2	2	V
$V_{sat\ 2}$	Start Up Saturation Voltage	I_{field} = 200 mA		0.7	1	V
I_q	Quiescent Current	Field Off		20		mA
I_s	Supply Current	I_{field} = 4 A_p		50		mA
I_{fs}	Field Pin Sink Current	Field Off Field Pin @ 16 V			5	mA
$V_{1\ CLAMP}$	Low Energy Clamping Zener Voltage	I_{clamp} = 50 mA		120		V
f_{sw}	Switching Frequency	01 I_n < I_{alt} < 0.9 I_n	30		1000	Hz

Note : 1. measured on an alternator with the following characteristics : I_n = < 90A ; I_{alt} / I_{field} > = 23.

APPLICATION CIRCUIT



LIQUID LEVEL ALARM

PRELIMINARY DATA

- DRIVES DIRECTLY 300 mA ALARM LOAD
- PROGRAMMABLE INPUT POLARITY TO ACTIVATE THE OUTPUT STAGE
- PROGRAMMABLE DELAY TIME
- PROGRAMMABLE OUTPUT DUTY CYCLE
- OUTPUT SHORT CIRCUIT PROTECTION
- OVERVOLTAGE AND THERMAL PROTECTION

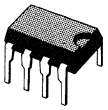
DESCRIPTION

The L4620 is an integrated circuit, designed for the liquid level control in automotive applications. The liquid level is indicated by an attenuation between transmitted and received signal across a sensor tip in the lquid. If the attenuation exceedes an internal threshold - sensor tip outside the liquid or liquid temperature higher than a determined value - a square-wave alarm output indicates an unsufficient liquid condition. If the liquid level is restored before the end of a delay time the alarm is not activated.

Through two pins it is possible to program : the delay time to activate the alarm, the duty cycle of the output squarewave, the polarity of the input threshold of the sensor for alarm activation.

The above features make the L4620 particularly versatile for many applications and give the possibility to use various sensor types.

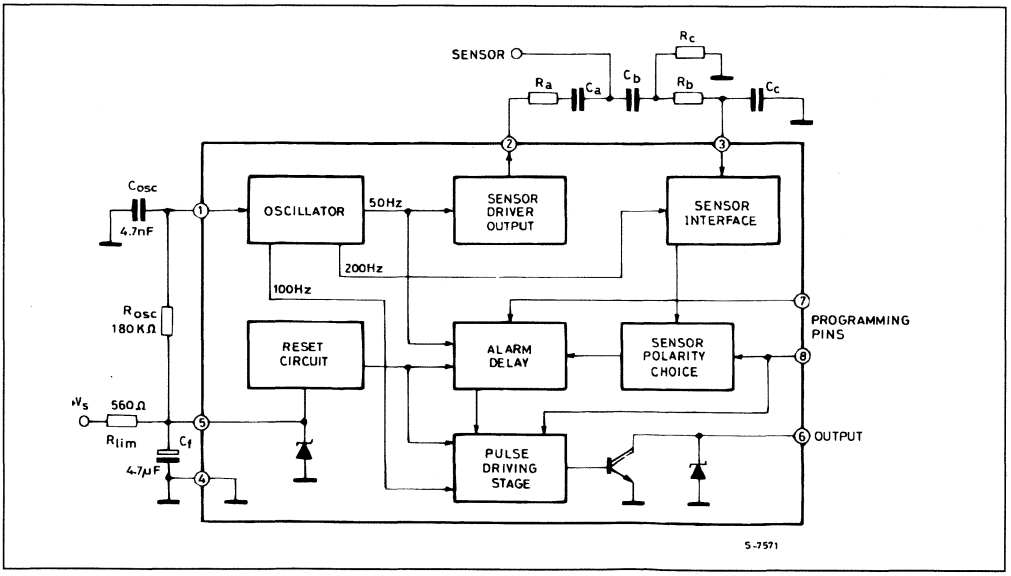
Internal circuits prevent spurious indications from the liquid sensor and a latch keeps the alarm acti-



MINIDIP

ORDER CODE : L4620

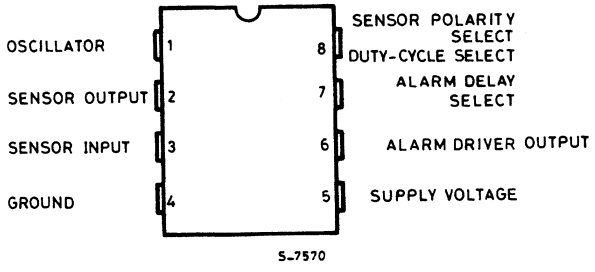
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_S	Supply Current ($V_S > V_Z$)	200	mA
V_3	Sensor Input Voltage (V_2 High)	7	V
I_{out}	Output Current	500	mA
P_{tot}	Power Dissipation at T_{amb} = 70°C	0.8	W
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

PIN FUNCTION (Block Diagram)

N°	Name	Function
1	Oscillator	A capacitor C_{osc} connected to ground and a resistor R_{osc} connected to pin 5 (supply voltage) set the frequency of the internal oscillator. The period is given by : $T_{osc} = 0.693\ (R_{osc} + 5000)\ C_{osc}$
2	Sensor Output	A squarewave is available at this pin to drive the external sensor. The output frequency is 1/32 of the internal oscillator fosc, i.e. 50Hz using the values of $R_{osc} = 180k\Omega$ and $C_{osc} = 4.7nF$ for the external components.
3	Sensor Input	Connection for liquid level sensing. During the zero level of the squarewave signal at pin 2, the internal sensing circuit is disabled. During the high level of the wave shape the input is compared with a threshold which depends on the output sensor voltage at pin 2. When the voltage at this pin is low, the threshold value is given by : $V_{SENSH} = 0.4V_2$ (typ). If the input voltage becomes higher than the above V_{SENSH}, the V_{sens} value is reduced to $V_{SENSL} = 0.22V_2$ (typ), providing an hysteresis available with both the programmable polarities.
4	GND	This pin must be connected to ground.
5	Supply Voltage	Supply voltage input. A 4.5V (typical) zener is present at the input. The external resistor limits the current through the zener for high supply voltages. Moreover when the voltage at this pin is down 2.5V (typical) the internal reset circuit is activated to inizialize the counters and to reset the memory alarm latch.
6	Alarm Driver Output	An internal open collector stage is available at this pin to drive the external alarm indicator by a rectangular waveshape. The output period depends on the external component R_{osc} and C_{osc}. Using the recommended values of block diagram the period T is 320ms (typ). The duty cycle depends on the status of the programming pin 8 (see pin 8 function) and can be or 1 : 2 or 1 : 64 i. e., refer to fig. 2, t = 160ms or t = 5ms.
7	Alarm Delay Select	This program pin selects the alarm delay to activate the output stage after a low liquid level indication of the sensor. The delay depends on the internal oscillator frequency. Refer to application circuit, if this pin is kept low the typical delay is 10.24s. When this pin is kept high, the typ delay becomes 20.48s.
8	Sensor Polarity Select Output Duty-cycle Select	Through this pin it is possible to program both the sensor polarity with respect to the internal threshold and the duty-cycle of the output waveform which drives the alarm. When this pin is kept low the output rectangular wave duty cycle is 1:64 (T = 320ms, t = 5ms in fig. 2) and the output is activated, after the delay time, if the voltage at pin 3 is higher than V_{SENS}. When the voltage at this pin is high the output duty cycle is 50% (t = 160ms) and the output goes on, after the delay time, if the voltage at pin 3 is less than V_{SENS}.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified. Refer to block diagram for external component values)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_Z	Internal Zener Voltage (pin 5)	I_S = 24mA	4	4.5	5	V
I_S	Supply Current (pin 5)	V_s = 3.8V		6.5	11	mA
f_{osc}	Oscillator Frequency (pin 1)	R_{osc} = 180kΩ, C_{osc} = 4.7nF	1.45	1.6	1.75	kHz
V_7, V_8	Programming Pins Input Voltage (pin 7, 8)	Low State			0.3	V
		High state	2			V
I_7, I_8	Programming Pins Input Current (pin 7, 8)	$V_7 = V_8$ = 0V	− 1			µA
		$V_7 = V_8 = V_Z$			150	µA
V_2	Sensor Drive Output Voltage, (*)	V_2 = Low, I_2 = 1mA			0.4	V
		V_2 = High, I_2 = 1mA	V_Z–1		V_Z–0.4	V
I_2	Sensor Driver Output Current		− 1		1	mA
V_{SENSH}/V_2	Sensor Input High Threshold Voltage Versus V_2 (pin 3)	V_2 = High $V_{pin\ 3} < V_{sensL}$	0.33	0.4	0.47	
$\frac{V_{SENSL}}{V_2}$	Sensor Input Low Threshold Voltage Versus V_2 (pin 3)	V_2 = High $V_{pin\ 3} > V_{sensH}$	0.15	0.22	0.29	
$V_{CLAMP3L}$	Sensor Input Clamping Voltage (pin 3)	− 100µA < I_{sens} < 100µA V_2 = Low	− 0.1		0.1	V
$V_{CLAMP3H}$		V_2 = High I_3 = − 100µA	− 0.8	− 0.6	− 0.4	V
		I_3 = + 100µA	V_Z		V_Z + 0.8	V
I_{sens}	Sensor Input Bias Current (pin 3)	V_{sens} = High			1.2	µA
T_d	Delay Time	f_{osc} = 1.6kHz V_7 = Low		10.24		sec
		V_7 = High		20.48		sec
$V_{out(sat)}$	Output Stage Saturation Voltage (pin 6) (**)	I_{out} = 200mA			1.3	V
$V_{out(clamp)}$	Output Stage Overvoltage Protection (pin 6)	I_{out} = 70mA	19	21	23	V

*) This is a squarewave signal. The frequency is given by : $f = \frac{1}{32} f_{osc}$.

**) The output squarewave signal frequency is given by $f = \frac{1}{512}$ fosc.

The duty cycle depends on the state of the pin 8 and can be or 1 : 2 or 1 : 64, i.e. refer to figure 2, T = 320 ms, t = 160 or 5 ms when the oscillator frequency f_{osc} = 1.6 KHz.

CIRCUIT OPERATION

The L4620 liquid level alarm is designed to operate with a variety of sensor types which change impedance depending on whether the sensor is above or below the level of a liquid. If the impedance variation of ther liquid itself is sensed, a very simple sensor (two electrodes) can be used. The output stage drives directly the alarm indicator with a 300mA rectangular wave signal, the duty cycle of which is programmable.

SENSOR INTERFACE.

As shown in the application circuit, the sensor is connected so that it varies the attenuation of a squarewave signal between pin 2 and pin 3 where its positive half cycle is compared with the reference threshold (with hysteresis).

This frequency, generated internally by a 50% duty cycle oscillator, is 50Hz in the typical application (R_{osc} = 180KΩ C_{osc} = 4.7nF).

The threshold of the sensor input is a function of the output voltage at pin 2. The hysteresis is provided by a Schmitt trigger comparator. As shown in figure 1, this gives hysteresis with either threshold polarity selected.

The AC driving of the level sensor allows the use of a capacitive filter (C_A, C_B, C_C in block diagram) which acts as a bandpass filter at the frequency used. The resistor R_C in the application circuit biases the sensor input stage. In this way the interference problems typical of automotive applications are reduced considerably. If, however, it is not necessary to decouple and filter the sensor a simple resistive network may be used, eliminating the capacitors.

SPURIOUS INDICATION PROTECTION.

To prevent spurious alarm signals when the liquid is agitated or in the presence of interference, the device includes two protection mechanism :

Firstly, the sensor interface which samples the positive half cycle of the sensor signal activates its output only if there are four consecutive alarm condition indications. Secondly, the alarm output stage is only activated after an externally programmable delay. During this delay if the alarm condition ceases the alarm output will not be activated.

Using the values C_{osc} = 4.7nF and R_{osc} = 180KΩ, which give a typical oscillator frequency of 1.6KHz, delays of about 10 s (programming pin 7 low) or 20s.

INTERNAL MEMORY.

When the alarm output has been activated an internal latch holds it in the active state until the power supply is removed. This feature ensures that the alarm will not be interrupted if the sensor connection breaks.

OUTPUT STAGE.

Through pin 8 it is possible to program the duty cycle of the alarm signal waveform (see figure 2). When pin 8 is high the output signal has a duty cycle of 50% ; if pin 8 is low the duty cycle is 1 : 64. The period of the output signal is always 320ms using the component values indicated in block diagram.

The output stage can deliver up to 300mA and is protected internally against overvoltages (by a zener).

A thermal shutdown circuit provides additional protection.

SENSOR INPUT WAVEFORM

Figure 1a : Pin 8 Low ; Alarm with Input Voltage > Threshold.

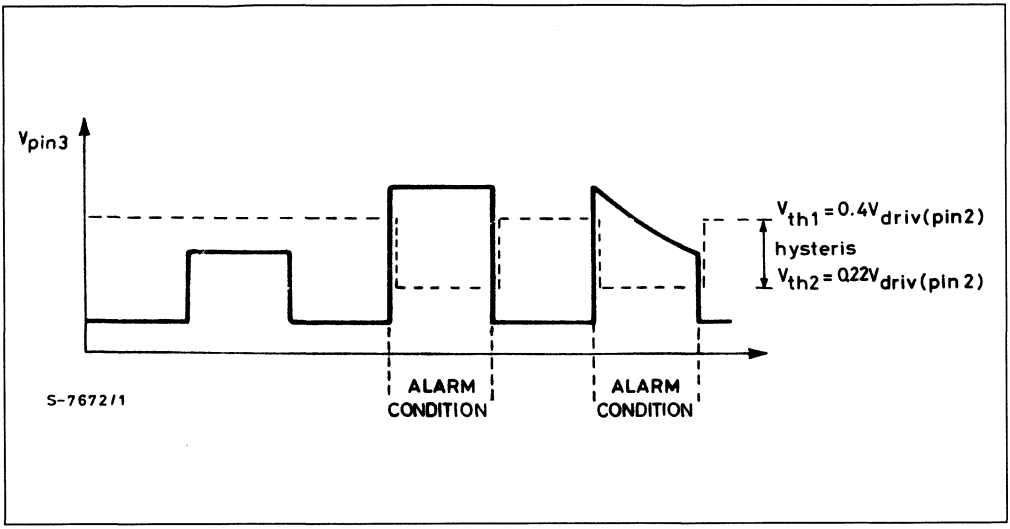


Figure 1b : Pin 8 High ; Alarm with Input Voltage < Threshold.

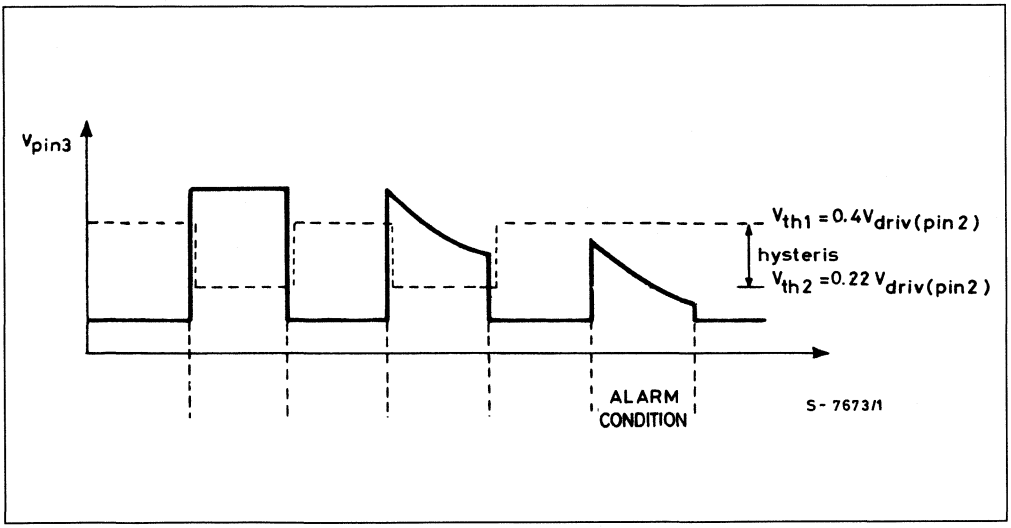


Figure 2a : Output Alarm Waveform with Pin 8 High : $t = \frac{1}{2} T$.

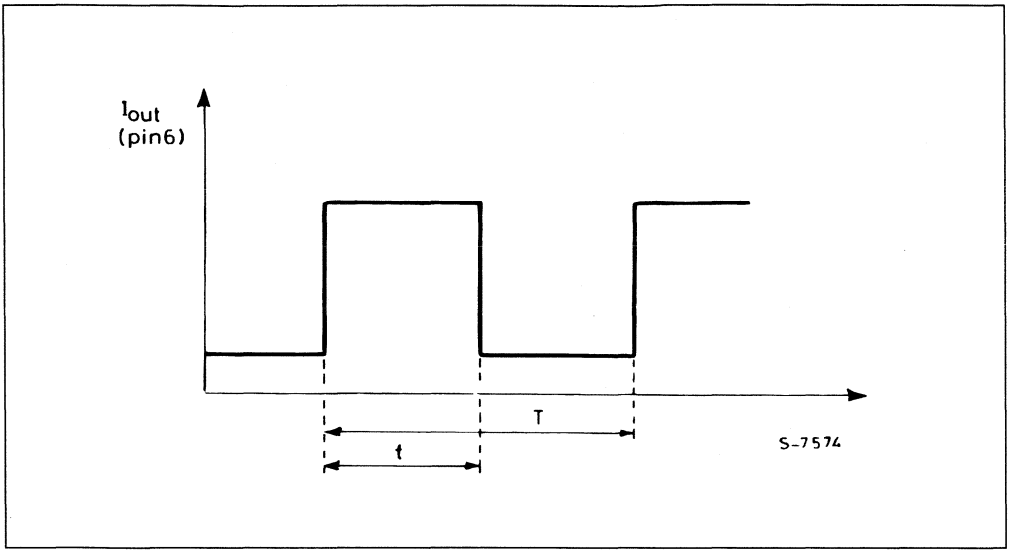
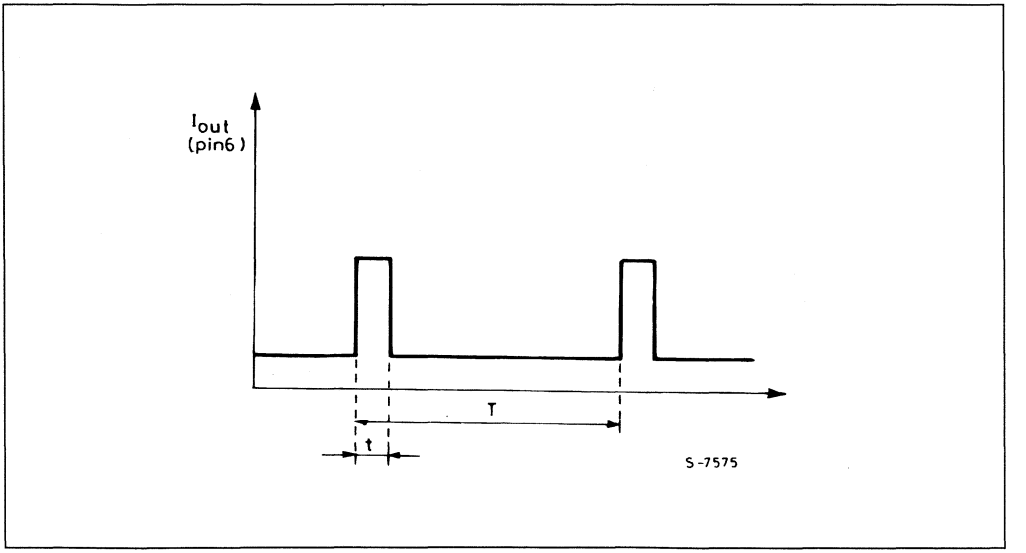


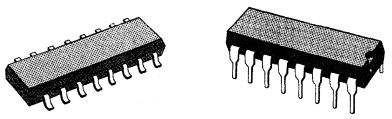
Figure 2b : Output Alarm Waveform with Pin 8 Low : $t = \frac{1}{64} T$.



PWM POWER MOS CONTROLLER

ADVANCE DATA

- HIGH EFFICIENCY DUE TO PWM CONTROL AND POWERMOS DRIVER
- LOAD DUMP PROTECTION
- LOAD POWER LIMITATION
- EXTERNAL POWERMOS PROTECTION
- LIMITED OUTPUT VOLTAGE SLEW RATE



SO-16 J **DIP-16**

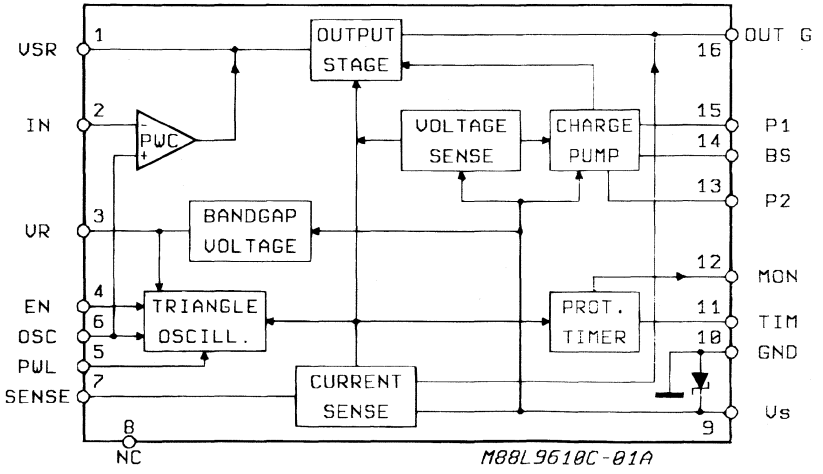
ORDER CODES : L9610C
L9611C

DESCRIPTION

The L9610C/11C is a monolithic integrated circuit working in PWM mode as controller of an external powerMOS transistor in High Side Driver configuration.

Features of the device include controlled slope of the leading and trailing edge of the gate driving voltage, linear current limiting with protection timer, settable switching frequency fo, TTL compatible enable function, protection status ouput pin. The device is mounted in SO 16 micropackage, and DIP 16 package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

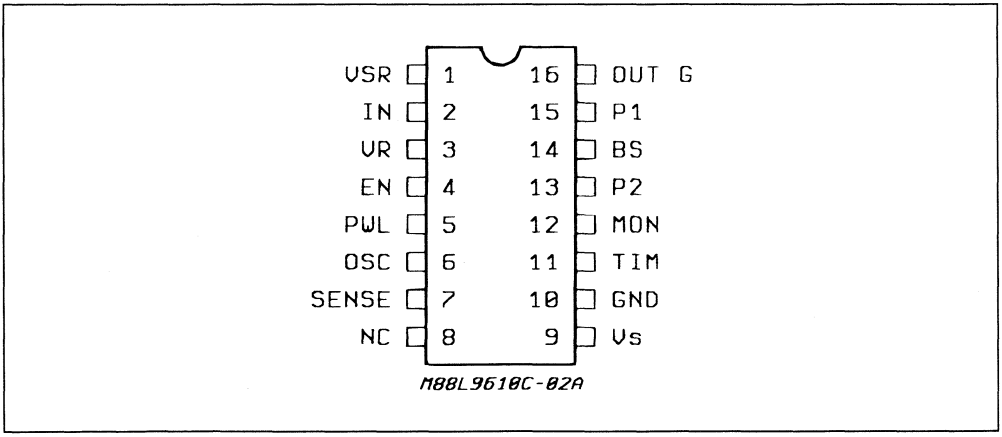
Symbol	Parameter	Value	Unit
V_S	D.C. Supply Voltage	26	V
	Transient Peak Supply voltage ($R_1 \geq 100\Omega$) : Load Dump : $5ms \leq t_{rise} \leq 10ms$ τ_f Fall Time Constant = 100ms $R_{SOURCE} \geq 0.5\Omega$ Field Decay : $5ms \leq t_{fall} \leq 10ms$, $R_{SOURCE} \geq 10\Omega$ τ_r Rise Time Constant = 33ms Low Energy Spike : $t_{rise} = 1\mu s$, $t_{Fall} = 2ms$, $R_{SOURCE} \geq 10\Omega$	 60 – 80 ± 100	 V V V
I_S	Maximum Supply Current (t < 300ms)	0.3	A
V_{IN}	Input Voltage	$-0.3 < V_{IN} < V_S - 2.5$	V
T_j, T_{STG}	Junction and Storage Temperature	– 55 to + 150	°C

THERMAL DATA

SO16J				
$R_{th\ j\text{-}alumina}$(*)	Thermal Resistance Junction-alumina	Max	50	°C/W
DIP16				
$R_{th\ j\text{-}a}$	Thermal Resistance Junction-ambient	Max	90	°C/W

Note : (*) Thermal resistance junction-pins with chip soldered on the middle of an alumina supporting substrate measuring 15 x 20mm : 0.65mm Thickness and infinite heatsink.

CONNECTION DIAGRAM



PIN FUNCTIONS

Pin	Name	Functions
1	VSR	A capacitor connected between this pin and Out_G defines the GATE Voltage Slew Rate.
2	IN	Analog Input Controlling the PWM Ratio. The operating range of the input voltage is 0 to V_R.
3	V_R	Output of an Internal Voltage Reference
4	EN	TTL Compatible Input for Switching off the Output
5	PWL	If this pin is Connected to GND and V_S > 13V, the duty cycle and the frequency fo are reduced : this allows to transfer a costant power to the load.
6	Osc	The capacitor connected to this pin defines the frequency of the internal triangle oscillator.
7	SENSE	Input of an Operational Amplifier for Short Current Sensing and Regulation.
8	NC	Not Connected.
9	V_S	Common Supply Voltage Input
10	GND	Common Ground Connection
11	TIM	A capacitor connected between this pin and GND defines the protection delay time.
12	MON	Open Collector Monitoring Output off the PowerMOS Protection.
13,15	P2, P1	Connection for the Charge Pump Capacitor.
14	BS	The Capacitor Connected between this Pin and the Source of the Power MOS Allows to Bootstrap the Gate Driving Voltage.
16	Out G	Output for Driving the Gate of the External PowerMOS.

ELECTRICAL CHARACTERISITCS (T_{amb} = – 40°C to 85°C ; 6V ≤ V_S ≤ 16V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage		6		16	V
I_q	Quiescent Current			2.5	6	mA
V_{SC}	Internal Supply Voltage Clamp	I_S = 20mA	28	32	36	V
V_{SH}	Supply Voltage High Threshold		16	18.5	21	V
V_{SL}	Supply Voltage Low Threshold		4	5	6	V
V_R	Reference Voltage		3.3	3.5	3.7	V
I_R	Reference Current	ΔV_R ≤ 100mV			1	mA
V_{INL}	Input Low Threshold		0.13	0.15	0.2	V_{IN}/V_R
K_F	Oscillator Frequency Constant	Note 1	900		2000	nF/s
K_S	Gate Voltage Slew Rate Constant	Note 2	3.25	5	6.75	nFV/ms
K_T	Protection Time Delay Constant	Note 3	0.17		0.39	ms/nF
V_{Si}	Sense Input Voltage		80	100	120	mV
V_{GON}	Gate Driving Voltage above V_S	V_S = 16V	8		16	V
V_{GOFF}	Gate Voltage in OFF Condition	I_G = 100µA			1.2	V
I_{IN}	Input Current		– 5	– 1		µA
V_{ENL}	Low Enable Voltage				0.8	V
V_{ENH}	High Enable Voltage		2.0			V
I_{EN}	Enable Input Current				2	µA
SR	Slew Rate	Without C_S		0.5		V/µs
V_{MONsat}	Saturation Voltage (pin 12)	I_{MON} = 2.5mA			1.5	V

Notes : 1. $f_o = K_F/C_F$.
2. $dV_G/dt = K_S/C_S$.
3. $t_{prot} = K_T C_T$.

FUNCTIONAL DESCRIPTION

PULSE WIDTH COMPARATOR

A ground compatible comparator generates the PWM signal which controls the gate of the external powerMOS.

The slopes of the leading and trailing edges of the gate driving signal are defined by the external capacitor C_S according to :

$$dV_G/dt = K_S/C_S$$

This feature allows to optimize the switching speed for the power and RFI performance best suited for the application.

The lower limit of the duty cycle is fixed at 15 % of the ratio between the input and the reference voltage (see fig. 1). Input voltages lower than this value disable the internal oscillator signal and therefore the gate driver.

GROUND COMPATIBLE TRIANGLE OSCILLATOR

The triangle oscillator provides the switching frequency f_o set by the external capacitor C_F according to :

$$f_o = K_F/C_F$$

If the pin PWL (power limitation) is connected to ground and Vs is higher than the PWL threshold voltage, the duty cycle and the f_o frequency are reduced : this allows to transfer a costant power to the load (see fig. 2).

TIMER AND PROTECTION LATCH

When an overcurrent occurs, the device starts charging the external capacitor C_T ; the protection time is set according to :

$$t_{prot} = K_T \cdot C_T$$

After the overcurrent protection time is reached, the powerMOS is switched-off ; this condition is latched by setting an internal flip-flop and is externally monitored by the low state of the MON pin.

To reset the latch the supply voltage has to fall below V_{SL} or the device must be switched off.

UNDER AND OVERVOLTAGE SENSE WITH LOAD DUMP PROTECTION

The undervoltage detection feature resets the timer and switches off the output driving signal when the supply voltage is less than V_{SL}.

If the supply voltage exceeds the max operating supply voltage value, an internal comparator disables the charge pump, the oscillator and the external powerMOS.

In both cases the thresholds are provided with suitable hysteresis values.

The load dump protection function allows the device to withstand - for a limited time - high overvoltages. It consists of an active clamping diode which limits the circuit supply voltage to V_{CLAMP} and an external current limiting resistor R1. The maximum pulse supply current (see abs. max. ratings is equal to 0.3A. Therefore the maximum load dump voltage is given by :

$$V_{DUMP} = V_{SC} + 0.3R_1$$

In this condition the gate of the powerMOS is held at the GND pin potential and thus the load voltage is :

$$V_L = Vs - V_{CLAMP} - V_{GS}$$

Figure 1 : Typical Transfer Curve.

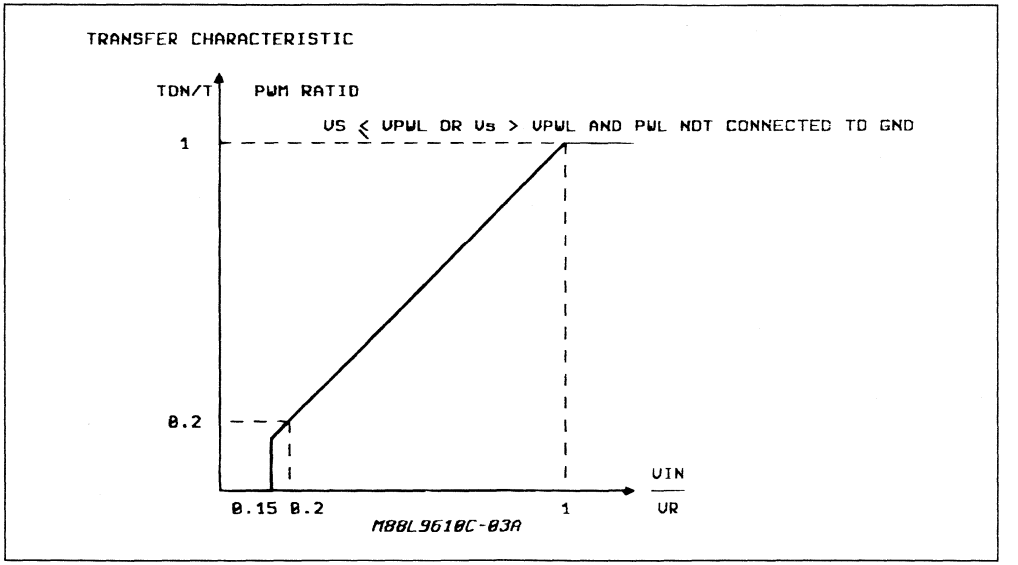
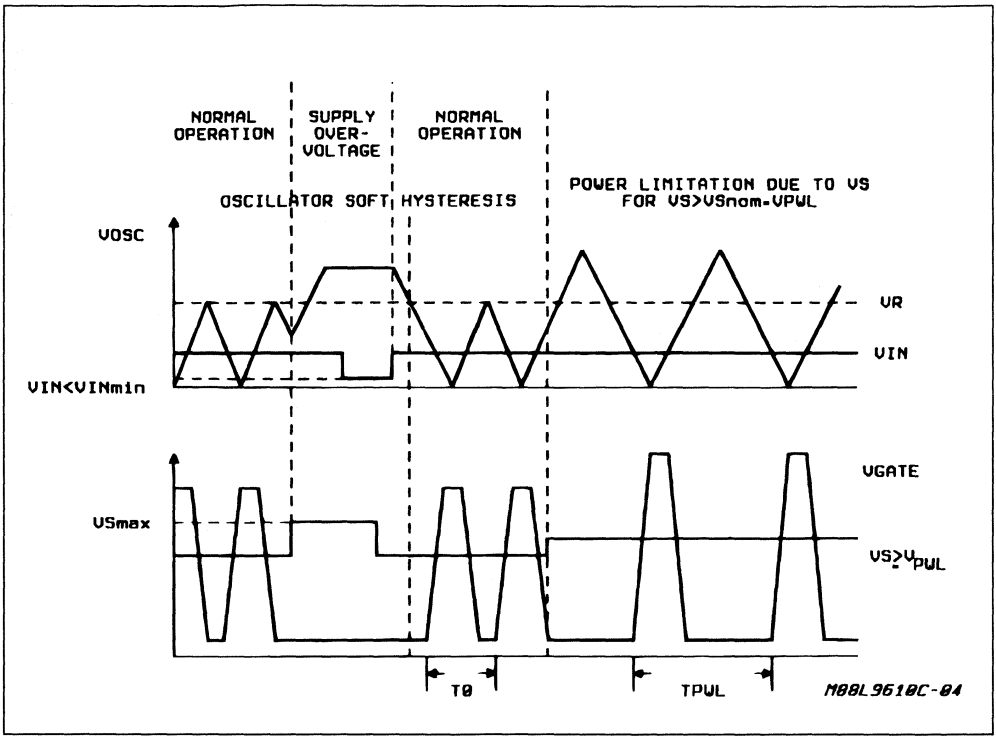


Figure 2 : The Typical Waveforms for the Power Limitation Function.



SHORT CIRCUIT CURRENT REGULATION

The maximum load current in the short circuit condition can be chosen by the value of the current sensing resistor R_S according to :

$$I_{SC} = V_{SI}/R_S$$

Two identical V_S compatible comparators are provided to realize the short circuit protection.

After reaching the lower threshold voltage (typical value V_{SI}-10 mV), the first comparator enables the timer and the gate is driven with the full continuous pump voltage : when the upper threshold voltage value is reached the second comparator maintains the chosen I_{SC} driving the NMOS gate in continuous mode.

This function - showed in fig. 3 - speeds up the switch on phase for a lamp as a load.

BANDGAP VOLTAGE REFERENCE

The circuit provides a reference voltage which may be used as control input voltage through a resistive divider. This reference is protected against the short circuit current.

CHARGE PUMP

The charge pump circuit holds the N-MOS gate above the supply voltage during the ON phase. This circuit consists of an RC astable which drives a comparator with a push-pull output stage. The external charge pump capacitor C_P must be at least equal to the NMOS parasitic input capacitance.

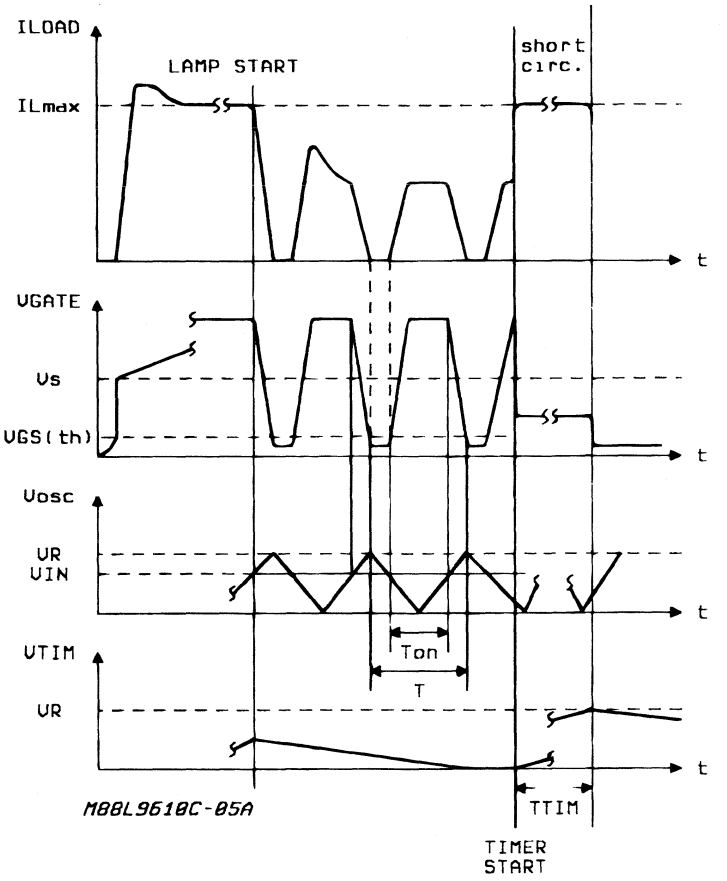
For fast gate voltage variation C_P must be increased or the bootstrap function can be used. The bootstrap capacitor should be at least 10 times greater than the powerMOS parasitic capacitance.

The charge pump voltage V_{PUMP} can reach to :

$$V_{PUMP} = 2\,V_S - V_{BE} - V_{CESAT}$$

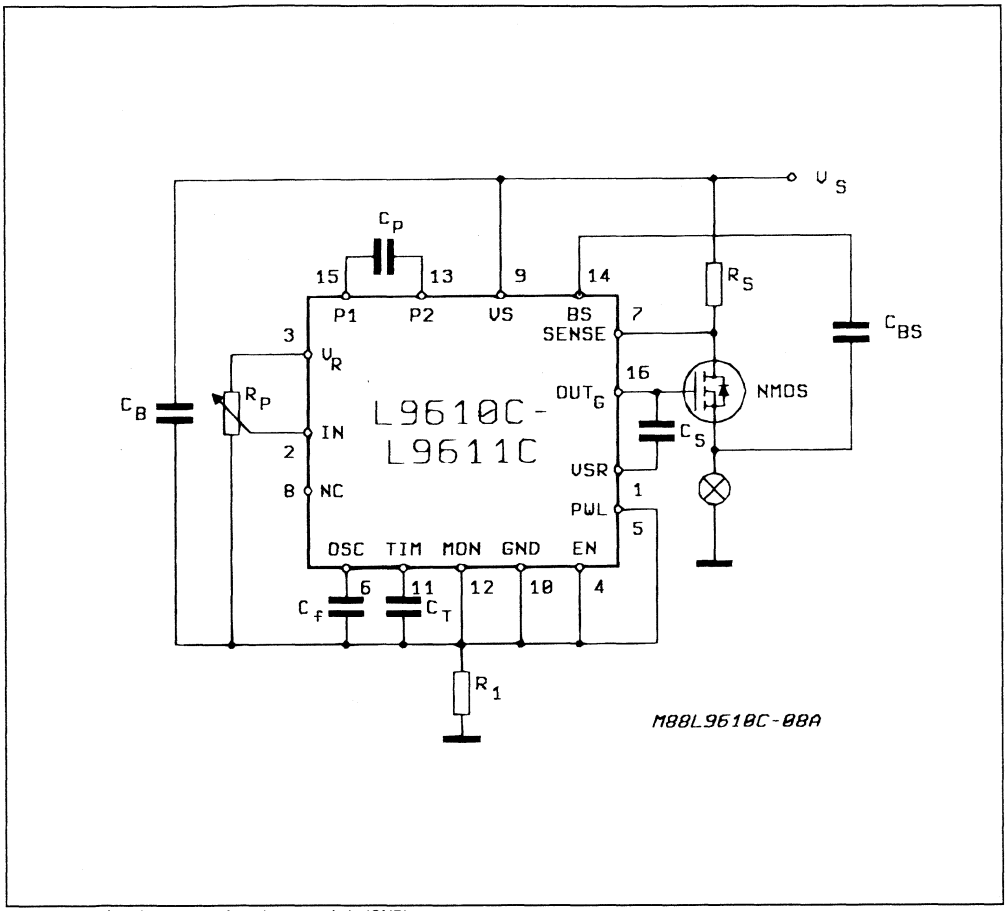
The circuit is disabled if the supply voltage is higher than V_{SH}.

Figure 3 : The Typical Waveforms for Short Circuit Current Condition.



APPLICATION CIRCUIT

Figure 4.



Note : All node voltages are referred to ground pin (GND)
The currents flowing in the arrow direction are assumed positive
without C_{BS} : C_P = 1nF
without C_{BS} : C_{BS} must be at least 10 times higher than the gate capacitance : C_P = 100 pF.

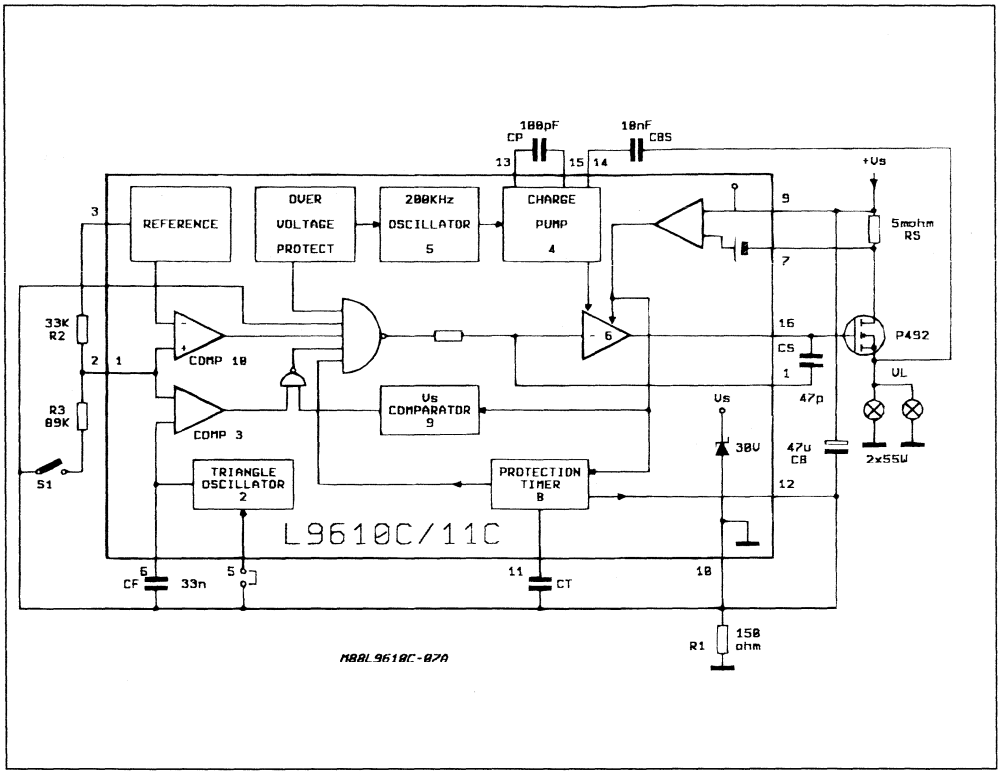
CONTROLLING A 120W HALOGEN LAMP WITH THE L9610C/11C DIMMER

The L9610C/11C Lamp Dimmer is used to control the brightness of vehicle headlamps using H4 type lamps (see fig. 5). With switch S1 open the full supply voltage is applied to the lamps : closing the switch it is a possible to reduce the average lamp voltage as desired :

$$VL = VS \frac{R3}{R2 + R3}$$

If pin 5 is connected to ground the average lamp voltage is constant, even for supply voltages in excess of 13 V.

Figure 5 : Application Circuit.



The sensing resistor R_S and timing capacitor C_t should be dimensioned according to :

$$R_S = \frac{V_{Si}}{2Inom\ (@Vs=14\ V)}$$

$$C_t = \frac{2 \times limitation\ time}{K_T}$$

In normal conditions (V_{CC} = 14 V, maximum brightness) the voltage drop across the sense resistor must be 50 mV. The current limiter intervenes attwice the nominal current, I_{nom}.

The timing capacitor C_t (V_{ct} = 3.5 V) must be chosen so that the delay before intervention is twice the duration of the current limitation at power-on.

The optimal value of the oscillator frequency, taking tolerances into account, must be slightly higher than the frequency at which lamp flicker is noticable (min 60 Hz).

The switching times are a compromise between possible EMI and switching power losses. The recommended value for Cs is 47pF.

AUTOMOTIVE DIRECTION INDICATOR

ADVANCE DATA

- RELAY DRIVER IN CAR DIRECTION INDICATORS
- DOUBLE FLASH FREQUENCY TO INDICATE LAMP FAILURE
- DUMP PROTECTION (± 80V)
- REVERSE BATTERY PROTECTION

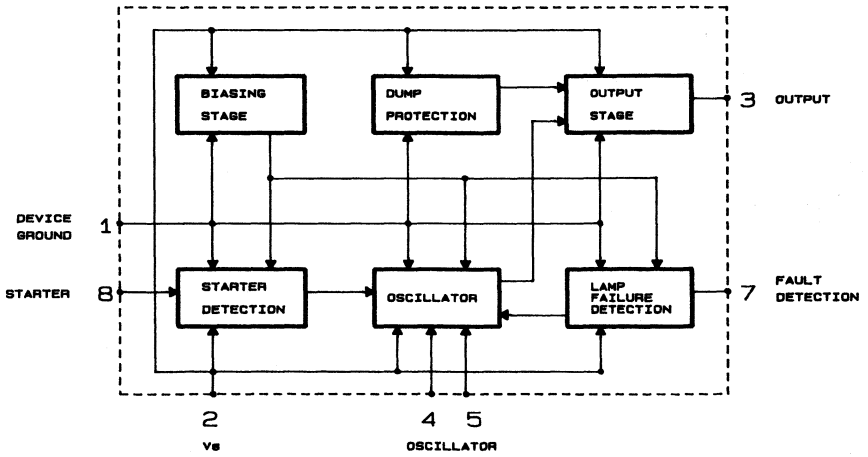
PlasticMinidip

ORDER CODE : L9686

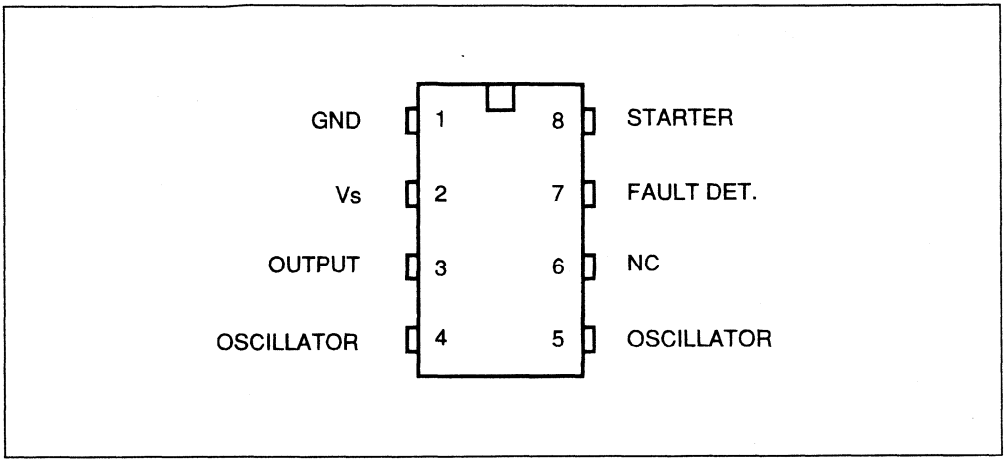
DESCRIPTION

The L9686 is a two frequency oscillator particularly suitable as relay driver for flashing light control in automotive applications. The circuit may be also used for other warning lamps like "handbrake on" etc. The lamp failure detection is given by doubling the flash repetition frequency. The L9686 is supplied in a minidip 8-lead plastic package.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Transient Peak Supply Voltage ($R_3 \geq 220\Omega$) : Load Dump : $5ms \leq t_{rise} \leq 10ms$ τ_f Fall Time Constant = 100ms $R_{SOURCE} \geq 0.5\Omega$ Field Decay : $5ms \leq t_{fall} \leq 10ms$, $R_{SOURCE} \geq \Omega$ τ_r Rise Time Constant = 33ms Low Energy Spike : $t_{rise} = 1\mu s$, $t_{fall} = 2ms$, $R_{SOURCE} \geq 10\Omega$	 80 – 80 ± 100	 V V V
T_j, T_{STG}	Junction and Storage Temperature Range	– 55 to 150	°C
P_d	Power Dissipation (T_{amb} = 100°C)	500	mW

THERMAL DATA

$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	100	°C/W

ELECTRICAL CHARACTERISTICS $40°C \leq T_{amb} \leq 85°C$, $8V \leq V_S \leq 18V$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Voltage		8		18	V
V2 – V1	Clamping Voltage	See Note 1	28.5		34.5	
V2 – V3	Output Saturation Voltage	I_{RL} = 250mA			1.7	V
R_2	Starter Resistance	See Note 2			3.6	KΩ
K_N	Oscillator Constant K_N (normal Operation)	Fn = 1/KnRoCo Osc Frequency	1.27		1.74	
C_T	Temperature Coefficient of Kn	See Note 3		– 1.5 • 10–3		1/°C
D.C.	Duty Cycle (normal operation)		45	50	55	%
Kc	Oscillator Constant Kc (lamp failure detection)	Fc = 1/KcRoCo Osc Frequency	0.58		0.79	
DC_{LF}	Duty Cycle (lamp failure detection)		35	40	45	%
I_Q	Current Consumption Relay off I_{pin1}	V_S = 8V 13.5V 18V		2.2 2.7 3.3	3.8 3.6 4.0	mA
V_{th}	Lamp Failure Threshold (see note 4)	R_3 = 220Ω V_S = 13.5V $-40°C \leq T_{amb} \leq 85°C$	70	85	95	mV

Notes :
1. This voltage is the threshold used to protect the circuit against overvoltage : if V_S is > than this threshold, the relay will be on and the voltage across the device will maintain constant increasing the current in the protective resistor R_3.
2. This is the maximum value for operation. This value must be higher than 1KΩ in order to limit the current in pin 8 during load dumps. A recommended value for application should be 1.5KΩ.
   The external leakage from the blinker unit to ground must be with an equivalent resistor higher than 5.6 KΩ to avoid parasitic operation when the switch S_1 is off.
3. This temperature coefficient is usefull to compensate the drift of the external timing network (R_1, C_1).
4. This threshold is calculated for a 20mΩ shunt. The threshold is dependant of V_{bat} as the bulb current.

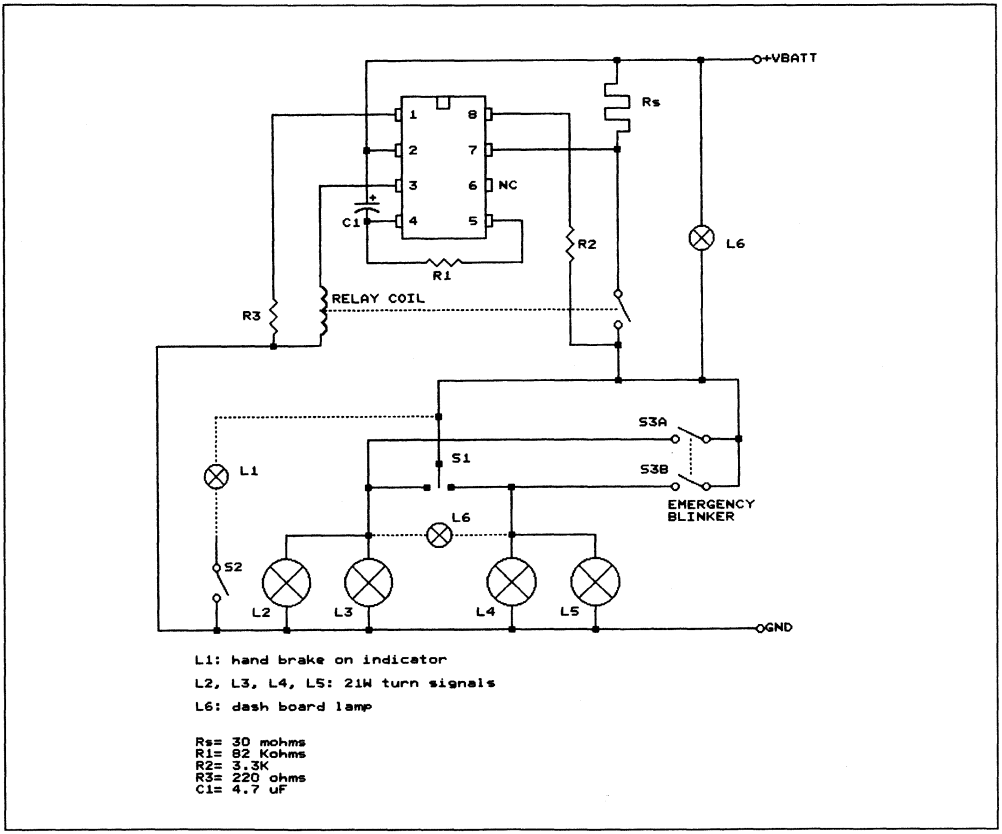
FUNCTIONAL DESCRIPTION

The application circuit shows the typical system configuration used to drive the direction indicator flasher relay consists of a network (R_1 C_1) to determine the oscillator frequency, a shunt resistor (R_S) to detect defective bulbs and two current limiting resistors (R_2/R_3) to protect the IC against load dump transients.

The lightbulbs L_2, L_3, L_4, L_5, are the turn signal indicators with the dashboard-light L_6. The S_1 switch position is sensed across resistor R_2 and R_{lamp} by input 8. The flashing cycle is starts closing S_1 : then, after a delay time t_d typically equal to 1.5 ms, pin 3 goes high activating the relay and switching on the corresponding lamps L_2, L_3, (or L_4, L_5). These lamps will flash at the oscillator frequency not depending on the battery voltage value (8 - 18 V). The flashing cycle stops and the circuit is reset to the initial position when the switch S_1 is open.

The lamp failure detection circuit senses the current through the shunt resistor R_S. When one of the lightbulbs is defective the voltage drop across R_S is reduced to a half and the failure is indicated by doubling the flashing frequency.

Figure 1 : Application Circuit.



SGS-THOMSON MICROELECTRONICS

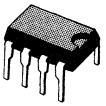
L9700

HEX PRECISION LIMITER

ADVANCE DATA

- HIGH PERFORMANCE CLAMPING AT GROUND AND POSITIVE REFERENCE VOLTAGE
- FAST ACTIVE CLAMPING
- OPERATING RANGE 4.75 - 5.25 V
- SINGLE VOLTAGE FOR SUPPLY AND POSITIVE REFERENCE
- LOW QUIESCENT CURRENT
- LOW INPUT LEAKAGE CURRENT

MINIDIP
(Plastic)



ORDER CODE : L9700

DESCRIPTION

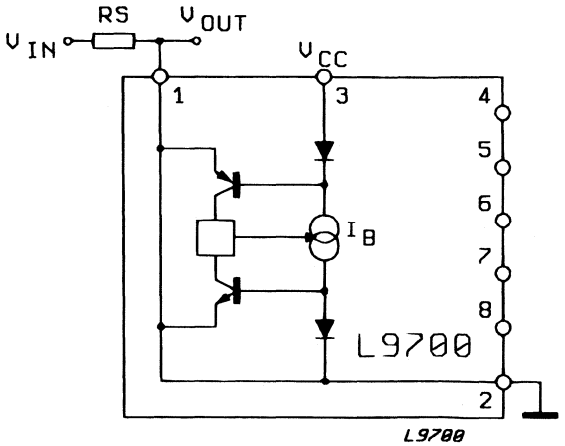
The L9700 is a monolithic circuit which is suited for input protection and voltage clamping purpose.

The limiting function is referred to ground and the positive supply voltage.

One single element contains six independent channels.

Very fast speed is achieved by internal feedback and the application of a new vertical PNP-transistor with isolated collector.

BLOCK DIAGRAM



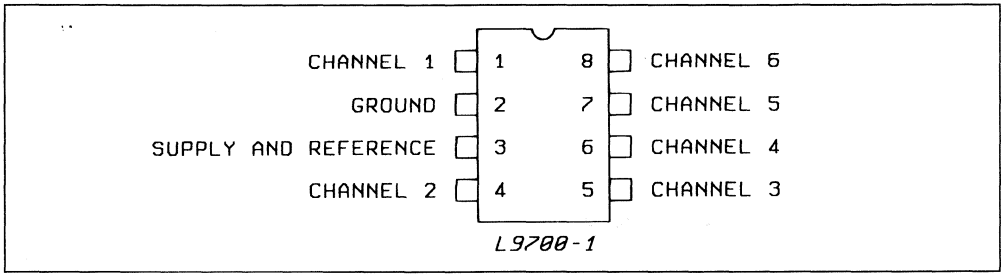
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	20	V
I_{IN}	Input Current per Channel	30	mA
T_j, T_{stg}	Junction and Storage Temperature	– 55 to 150	°C
P_D	Power Dissipation (T_A = 85°C)	650	mW

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

PIN CONNECTION



L9700-1

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_j = – 40 to 125°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75		5.25	V
I_{CC}	Supply Current			1.5	3	mA
V_{cls}	Static Input Clamping Voltage					
	Negative	I_{IN} = – 10mA	– 250		0	mV
	Positive	I_{IN} = + 10mA	V_{CC}		V_{CC} + 250	mV
I_{IN}	Input Current (static)	V_{IN} = 0 V_{IN} = V_{CC} V_{IN} = 50mV V_{IN} = V_{CC} – 50mV			15 15 5 5	µA µA µA µA
V_{cld} (*)	Dynamic Input Clamping Voltage	I_{in} = ± 10mA t_R = 5ns				
	Positive Overshoot				400	mV
	Negative Overshoot				400	mV
t_S (*)	Settling Time	See fig. 2			20	ns
R_{IN}	Dynamic Input				5	Ω
C_{rtk}	Crosstalk between any two Inputs	0 ≤ V_{IN} ≤ V_{CC}, f_{IN} < 10kHz		70		dB

(*) Design limits are guaranteed by statistical control on production samples over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Figure 1 : DC INPUT CHARACTERISTIC Limit Points of the Characteristic Approximation.

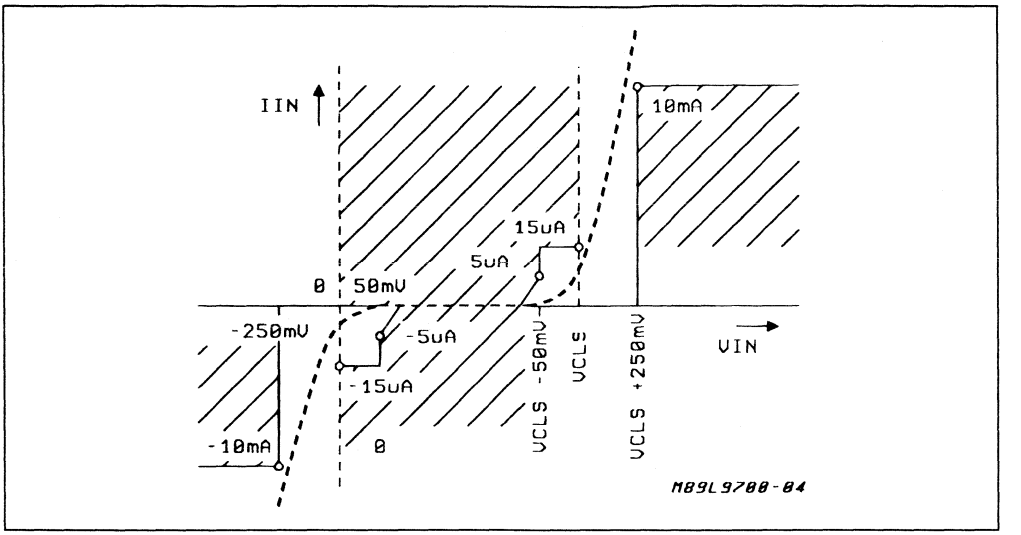


Figure 2 : Dynamical Input Characteristics.

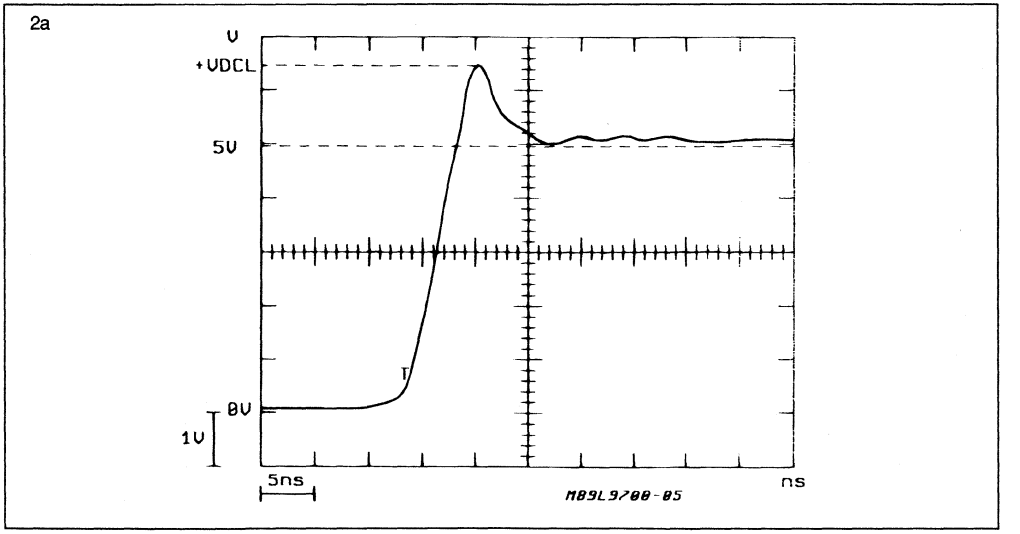
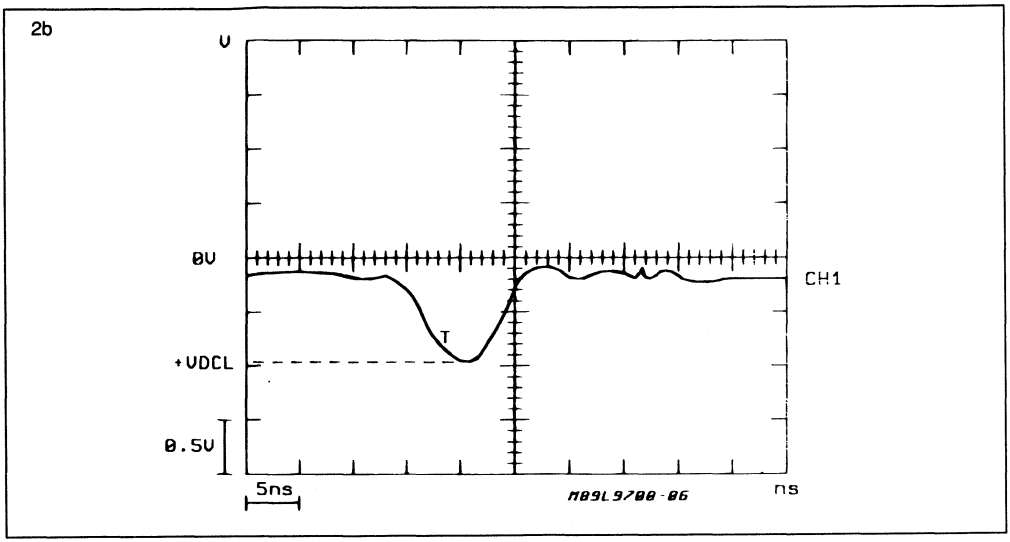


Figure 2 : Dynamical Input Characteristics (continued) .



APPLICATION INFORMATION

Most integrated circuits, both HNMOS and bipolar, are very sensitive to positive and negative overvoltages on the supply and at the inputs.

These transients occur in large numbers and with different magnitudes in the automotive environment, making adequate protection for devices aimed at it indispensible.

Overvoltages on the supply line are faced through high voltage integration technologies or through external protection (transil, varistor).

Signal inputs are generally protected using clamp diodes to the supply and ground, and a current limiter resistor. However, such solutions do not always completely satisfy the protection specifications in terms of intervention speed, negative clamping and current leakage high enough to change analog signals.

The L9700 device combines a high intervention speed with a high precision positive and negative clamp and a low current leakage providing the optimal solution to the problems of the automotive environment.

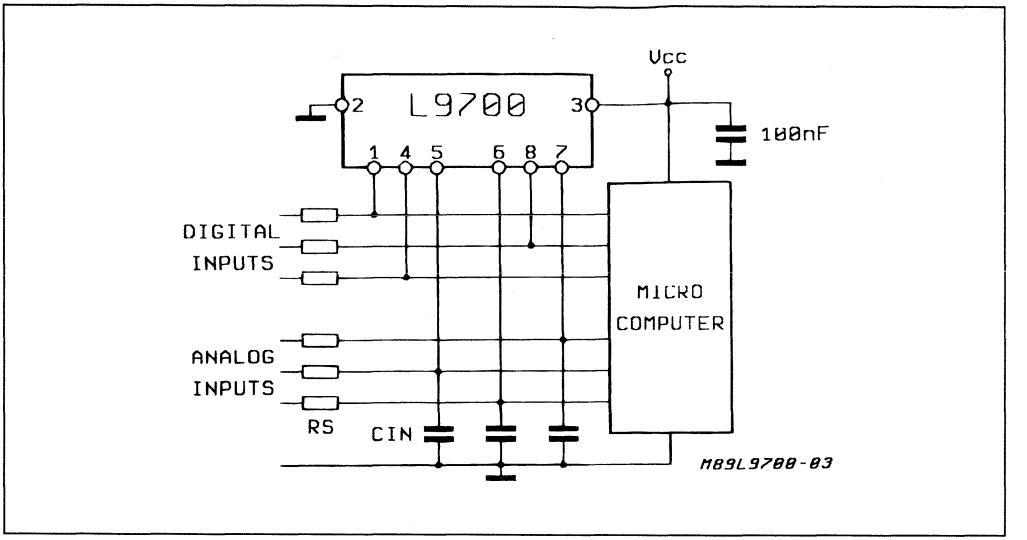
The high intervention speed, due to the pre-bias of the limiter stage and internal feedback, limits the voltage overshoot and avoid the use of external capacitors for the limitation of the transient rise times.

Figure 3 illustrates a typical automotive application scheme. The resistor R_S limits the input current of the device and is therefore dimensioned considering the characteristics of the transients to be eliminated. Consequently :

$$R_S = \frac{V_{transient\ Peak}}{I_{IN\ MAX}}$$

The C_{IN} capacitors must be used only on analog inputs because they present a low impedance during the sampling period.

Figure 3 : Typical Application.



The minimum value for C_{IN} is determined by the accuracy required, the time taken to sample the input and the input impedance during that time, while the maximum value is determined by the required frequency response and the value of R_S.

Thus for a resistive input A/D connector where :

T_S = Sample time (Seconds)
R_D = Device input resistance (Ohms)
V_{IN} = Input voltage (Volts)
k = Required accuracy (%)
Q_1 = Charge on capacitor before sampling
Q_2 = Charge on capacitor after sampling
I_D = Device input current (Amps)

Thus :

$$Q_1 - Q_2 = \frac{k \cdot Q_1}{100}$$

but $Q_1 = C_{IN} V_{IN}$

and $Q_1 - Q_2 = I_D - T_S$

so that $I_D T_S = \frac{k \cdot C_{IN} - V_{IN}}{100}$

and $C_{IN}(\text{min}) = \frac{I_D \cdot T_S}{V_{IN} \cdot k}$ Farad

so $C_{IN}(\text{min}) = \frac{100 \cdot T_S}{k \cdot R_D}$ Farad

The calculation for a sample and hold type convertor is even simpler :

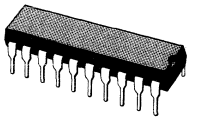
k = Required accuracy (%)
C_H = Hold capacitor (Farad)

$$C_{IN}(\text{min}) = \frac{100 \cdot C_H}{k} \text{ Farad}$$

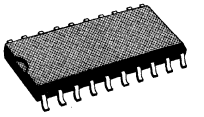
OCTAL GROUND CONTACT MONOTORING CIRCUIT

ADVANCE DATA

- OPERATING DC SUPPLY VOLTAGE RANGE 5V TO 25V
- SUPPLY OVERVOLTAGE PULSE UP TO 40V
- VERY LOW STANDBY QUIESCENT CURRENT 0.2mA
- INTERNAL CLAMPING DIODES AT CONTACT INPUTS TO V_S AND GND
- INPUT PULSE CURRENT CAPABILITY UP TO + 500mA ; – 750mA
- NOMINAL CONTACT CURRENT OF 10mA DEFINED BY EXTERNAL CONTACT SERIES RESISTORS R_{IN1-8}
- CONTACT STATUS MONITORING BY COMPARING THE RESISTANCE AT CONTACT SENSE INPUTS WITH THE INTERNAL REFERENCE RESISTOR VALUE
- HIGH IMMUNITY DUE TO RESISTANCE COMPARISON WITH HYSTERESIS



DIP-20



SO-20L

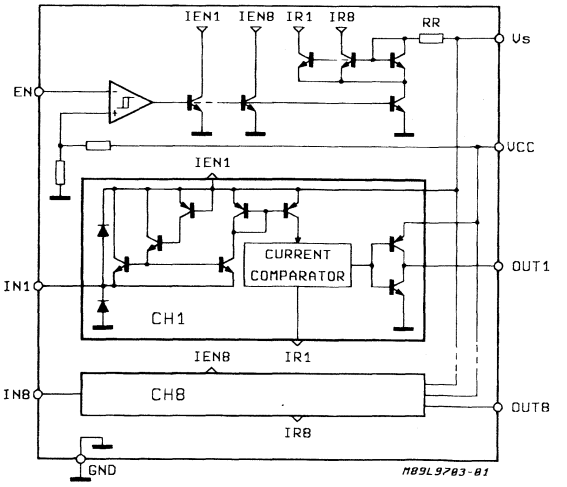
ORDER CODES : L9703(DIP-20)
L9703(SO-20L)

DESCRIPTION

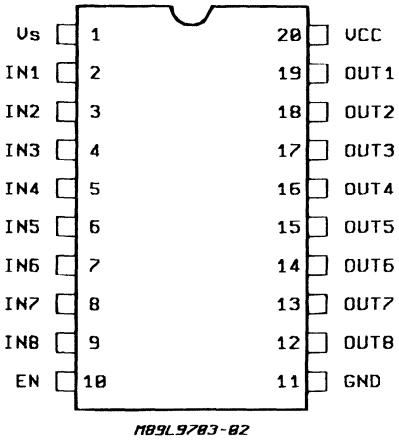
The L9703 is a bipolar monolithic integrated circuit for monitoring the status of up to eight contacts connected to GND.

It contains eight contact sense inputs and eight microcomputer compatible three-state outputs.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Transient Supply Voltage ($t \leq 1sec$)	+ 40	V
V_{CC}	Logic Supply Voltage	7	V
I_{INDC}	Input DC Current	± 40	mA
I_{INP}	Input Pulse (test pulse specification : $0 < t_p < 2ms$, $f \leq 0.2Hz$, $n = 25000$)	 + 50 − 75	 mA mA
I_{OUT}	Output Current	Internally Limited	
V_{EN}	Enable Input Voltage	− 0.3 to + 7	V
P_O	Power Dissipation ($T_A = 80°C$) DIP 20 SO 20	 875 420	 mW mW
T_j, T_{stg}	Junction and Storage Temperature Range	− 55 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}A}$	Thermal Resistance Junction to Ambient : DIP 20	Max	80	k/W
	SO 20	Max	165	k/W

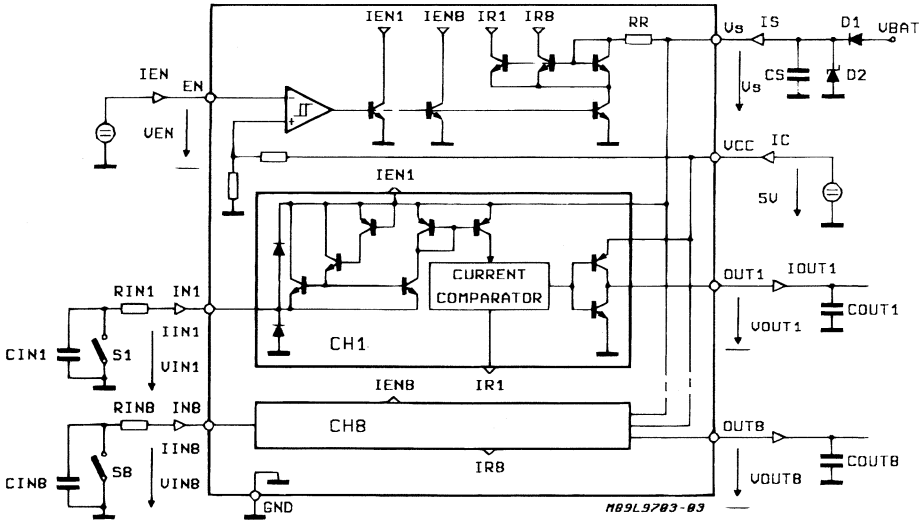
ELECTRICAL CHARACTERISTICS ($5V \leq V_S \leq 25V$; $-40°C \leq T_j \leq 125°C$; $4.75V \leq V_{CC} \leq 5.25V$ unless otherwise specified ; the currents flowing in the arrow direction are assumed positive as marked in the application circuit diagram, fig. 1).

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{ENL}	Enable Input Voltage LOW (device activated)				0.8	V
V_{ENH}	Enable Input Voltage HIGH		2.4			V
$V_{EN\ hyst}$	Enable Input Hysteresis		200	300	400	mV
I_{EN}	Enable Input Current	$2.4V < V_{EN} < V_{CC}$			5	µA
		$0V < V_{EN} < 0.8V$	-5	-1		µA
V_{OUTH}	Output Voltage HIGH	$0 < I_{OUT} < 100µA$	4.0	$V_{CC} - 0.1$	5.25	V
V_{OUTL}	Output Voltage LOW	$I_{OUT} = -1mA$	0.05	0.2	0.4	V
$I_{OUT\ TS}$	Output TRISTATE Current	$0 < V_{OUT} < 5.5V$			0.5	µA
V_{IN}	Input Voltage (device active)	EN = LOW $R_{IN} = 650Ω$	$V_S - 2$	$V_S - 1.5$	$V_S - 0.6$	V
V_{IN}	Input Clamped Voltage (device disabled)	E_N = HIGH $I_{IN} = 30mA$ $I_{IN} = -30mA$	$V_S + 0.3$ -2	$V_S + 1$ -1	$V_S + 2$ -0.3	V V
I_{OUT}	Output Current	OUT = HIGH $V_{OUT} = 0$			2	mA
I_{OUT}	Output Current	OUT = LOW $V_{OUT} = 5.5V$			-15	mA
R_{IL}	Input Resistor (note 1) LOW Threshold	$5V < V_S < 16V$ $\lvert\Delta V_{GND}\rvert \leq 0.1V_S$	1.1	4		KΩ
R_{IH}	Input Resistor (note 1) HIGH Threshold			5.3	20	KΩ
$\frac{R_{IL}}{R_{IH}}$	Input Resistor Threshold Ratio (note1)		0.65	0.75	0.85	
I_{QC}	Quiescent Current	EN = HIGH ($t_{ENH} \geq 20µs$) $5V < V_S < 16V$ $-40°C \leq T_j \leq 100°C$		0.12	0.16	
I_{QS}		All Inputs Open			0.04	mA
		All Inputs Closed			0.24	mA
I_{QS}		EN = LOW $R_R \geq 50kΩ$			3 9	mA
t_{do}	Delay Time/Output (EN LOW to output data ready)	$C_{OUT} \leq 50pF$			15 $+ 3R_{IN}\ C_{IN}$	µs
t_{dTS}	Delay Time/Tristate (EN HIGH to output TRISTATE)	$C_{OUT} \leq 50\ pF$			10	µs

Note : 1. The input resistor threshold value is the resistor value from the IN-pin to ground at which the corresponding output changes its status (see fig. 3).

APPLICATION CIRCUIT

Figure 1 : Typical Application Diagram for the L9703 Circuit. The current flowing in the arrow direction is assumed positive. The external capacitors C_{IN} and C_{OUT} represent the total wiring capacitance at the corresponding pins.



FUNCTIONAL DESCRIPTION

The L9703 circuit monitors the status of the contacts connected to ground and through this series external resistors R_{IN} to the contact sense input pins. The contacts equivalent circuit is supposed to be as shown in fig. 2.

The L9703 circuit compares the input current with the current through the internal reference resistor. The device is designed to work with an external input series resistor of $R_{IN1-8} = 1k\Omega$. With this input resistor the contact current, when the contact is closed and the device activated (EN = LOW) is

$$I_{IN} = \frac{V_S - 2V}{1k\Omega} \quad (1)$$

For this calculation the limit value of the V_S to IN saturation voltage of 2V was considered so that the lowest limit value of I_{IN} is calculated in (1).

The function of the circuit can be demonstrated with the transfer characteristics, showing the output status as a function of the input resistor R_I, shown in figure 3. The input resistor is a sum of the R_{IN} and the contact resistance R_{CON} or R_{COFF}, for the closed contact :

$$R_I = R_{IN} + R_{CON}, \quad (2)$$

and for the open contact :

$$R_I = R_{IN} + R_{COFF}. \quad (3)$$

The output goes HIGH when the input resistance increases above 5.3kΩ (typical value) and goes LOW, when the input resistance decreases below 4kΩ (typical value). The limit values of R_I = 1.1KΩ for LOW and R_I = 2kΩ for HIGH implies that a contact with R_{CON} = 100Ω (at I_{IN} = 10mA) will be recognized as ON = LOW and a contact with R_{COFF} = 19kΩ will be recognized as OFF = HIGH. These limits are valid within the supply voltage range $6V \leq VS \leq 16V$ and the ground potential difference of $|\Delta VGND| = 0,1V$.

The internal clamping diodes at the contact monitoring inputs, together with the external contacts series resistors R_{IN}, allows the device to withstand transients at the contact connection. The contact series resistor R_{IN} limits the input current at the transient.

The dynamic behaviour of the circuit is defined by the times t_{do} and t_{dTs}. When the contact is open, the input capacitor C_{IN} must be charged through the resistor R_{IN}. In this case the total delay time may also be influenced by the time constant $R_{IN}C_{IN}$.

The delay time t_{dTs}, when disabling the device, is defined only by the internal circuitry. In both cases, an external output capacitance less than 50pF is assumed, the internal output capacitances of the three-state buffers are less than 5pF.

Figure 2 : The Contact Sense Input Connection with the Contact Equivalent Circuit.

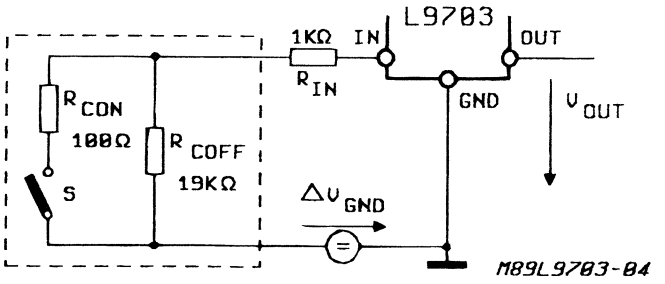
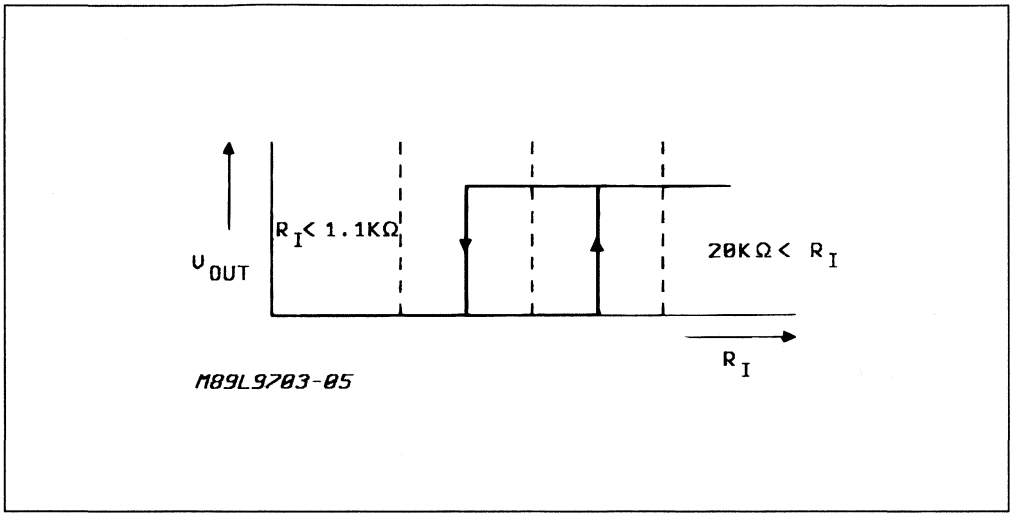


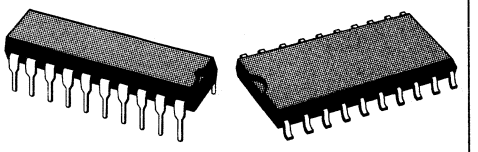
Figure 3 : The Output Voltage as a Function of the Input Resistance at the Corresponding Contact Sense Input.



OCTAL SUPPLY CONTACT MONITORING CIRCUIT

ADVANCE DATA

- OPERATING DC SUPPLY VOLTAGE RANGE 5V TO 25V
- SUPPLY OVERVOLTAGE PULSE UP TO 40V
- VERY LOW STANDBY QUIESCENT CURRENT 0.2mA
- INTERNAL CLAMPING DIODES AT CONTACT INPUTS TO V_S AND GND
- INPUT PULSE CURRENT CAPABILITY UP TO + 50mA, – 75mA
- NOMINAL CONTACT CURRENTS OF 10mA DEFINED BY EXTERNAL CONTACT SERIES RESISTORS R_{IN1-8}
- CONTACT STATUS MONITORING BY COMPARING THE RESISTANCE AT CONTACT SENSE INPUTS WITH THE INTERNAL REFERENCE RESISTOR VALUE
- HIGH IMMUNITY DUE TO RESISTANCE COMPARISON WITH HYSTERESIS



DIP–20 **SO–20L**

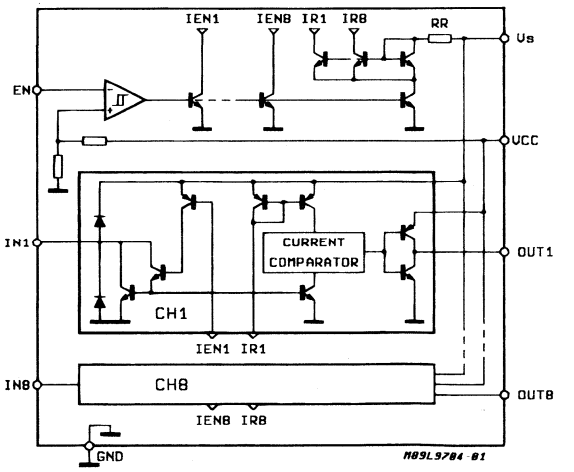
ORDER CODES: L9704 (DIP–20)
L9704D (SO–20L)

DESCRIPTION

The L9704 is a bipolar monolithic integrated circuit for monitoring the status of up to eight contacts connected to the power supply (battery).

It contains eight contact sense inputs and eight microcomputer compatible three-state outputs.

BLOCK DIAGRAM



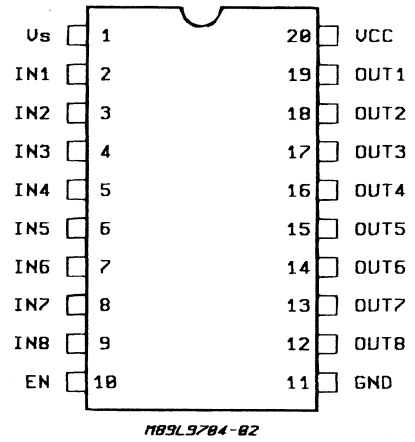
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Transient Supply Voltage ($t \leq 1$ sec.)	+ 40	V
V_{CC}	Logic Supply Voltage	7	V
I_{INDC}	Input DC Current	± 40	mA
I_{INP}	Input Pulse (test pulse specification : $0 < t_p < 2ms$, $f \leq 0,2Hz$, $n = 25000$)	+ 50 − 75	mA mA
I_{OUT}	Output Current	Internally Limited	
V_{EN}	Enable Input Voltage	− 0.3 to + 7	V
P_O	Power Dissipation ($T_A = 80°C$) DIP-20 SO-20	 875 420	 mW mW
T_j, T_{stg}	Junction and Storage Temperature Range	− 55 to 150	°C

THERMAL DATA

			DIP20	SO-20L	
$R_{th\ j\text{-}a}$	Thermal Resistance Junction to Ambient	Max	80	165	°C/W

PIN CONNECTION (top view)



ELECTRICAL CHARACTERISTICS ($5V \leq V_S \leq 25V$; $-40°C \leq T_j \leq 125°C$; $4.75V \leq V_{CC} \leq 5.25V$; $V_{BAT} - 0.5V \leq V_S \leq V_{BAT} - 1V$ unless otherwise specified ; the currents flowing in the arrow direction are assumed positive as marked in the application circuit diagram, fig. 1).

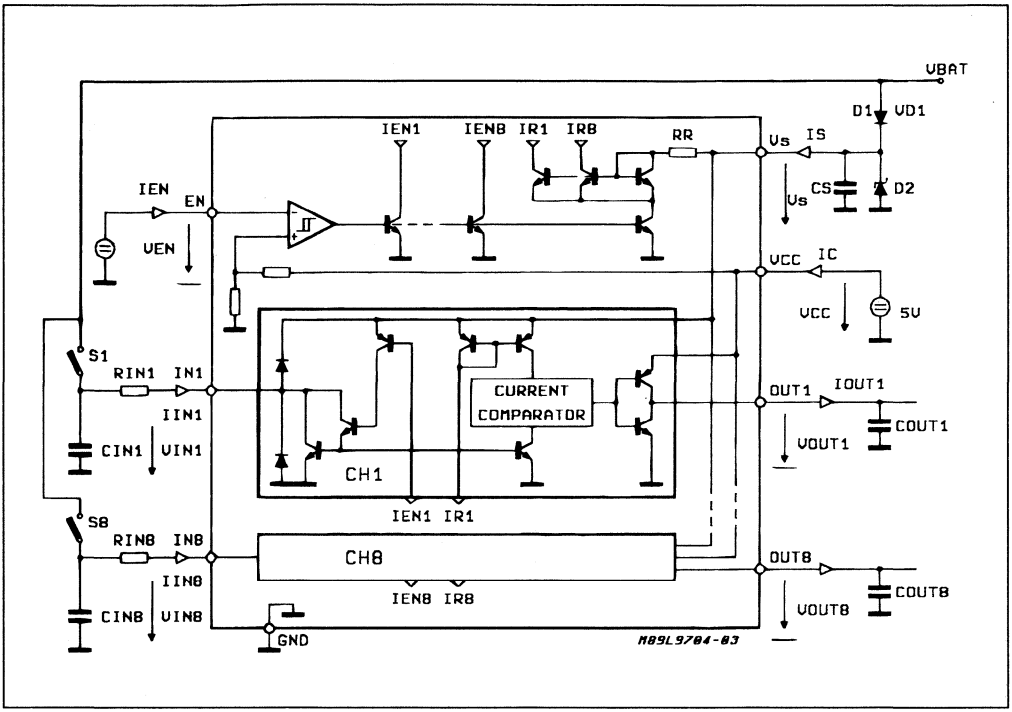
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{ENL}	Enable Input Voltage LOW (device activated)				0.8	V
V_{ENH}	Enable Input Voltage HIGH		2.4			V
V_{ENhyst}	Enable Input Hysteresis		200	300	400	mV
I_{EN}	Enable Input Current	$2.4V < V_{EN} < V_{CC}$ $0V < V_{EN} < 0.8V$	 -5	 -1	5	µA µA
V_{OUTH}	Output Voltage HIGH	$0 < I_{OUT} < 100µA$	4.0	$V_{CC}-0.1$	5.25	V
V_{OUTL}	Output Voltage LOW	$I_{OUT} = -1mA$	0.05	0.2	0.4	V
$I_{OUT\ TS}$	Output TRISTATE Current	$0 < V_{OUT} < 5.5V$			0.5	µA
V_{IN}	Input Voltage (device active)	EN = LOW $R_{IN} = 650Ω$ $R_R = 50kΩ$	0.6	1.5	2	V
V_{IN}	Input Clamped Voltage (device disabled)	EN = HIGH $I_{IN} = 50mA$ $I_{IN} = -50mA$	$V_S + 0.3$ -2	$V_S + 1$ -1	$V_S + 2$ -0.3	V V
I_{OUT}		OUT = HIGH $V_{OUT} = 0$			2	mA
I_{OUT}		OUT = LOW $V_{OUT} = 5.5V$			-15	mA
R_{IL}	Input Resistor LOW Threshold 1)	$5V < V_S < 16V$ $\|\Delta V_{BAT}\| \leq 0.1V_{BAT}$	1.1	4.8		KΩ
R_{IH}	Input Resistor HIGH Threshold 1)			6.5	29	KΩ
R_{IL} R_{IH}	Input Resistor Threshold Ratio 1)		0.65	0.75	0.85	
I_{QC}	Quiescent Current	EN = HIGH ($t_{ENH} \geq 80µs$) $5V < V_S < 16V$ $-40°C \leq T_j \leq 100°C$		0.12	0.16	mA
I_{QS}		All Inputs Open			0.04	mA
SI_{IN} 2)	Input Leakage Current	All Inputs Closed $V_{BAT} \leq V_{D1}$			0.24	mA
I_{QC}	Quiescent Current	EN = LOW $R_R \geq 50kΩ$			3	mA
I_{QS}					9	mA
t_{do}	Delay Time/output (EN LOW to output data ready)	$C_{OUT} \leq 50pF$			15 $+3R_{IN}C_{IN}$	µs
t_{dTS}	Delay Time/tristate (EN HIGH to output TRISTATE)	$C_{OUT} \leq 50pF$			10	µs

Notes : 1. The input resistor threshold value is a resistor value from the IN–pin to battery at which the corresponding output changes its status (see fig. 3).

2. SI_{IN} is the sum of the input currents $SI_{IN} = \sum_{i=1}^{8} I_{IN1}$.

APPLICATION CIRCUIT DIAGRAM

Figure 1 : Typical application diagram for the L9704 circuit. The current flowing in the arrow direction is assumed positive. The external capacitors C_{IN} and C_{OUT} represent the total wiring capacitance at the corresponding pins.



FUNCTIONAL DESCRIPTION

The L9704 circuit monitors the status of the contacts connected to battery and through the series external resistors R_{IN} to the contact sense input pins. The contacts equivalent circuit is supposed to be as shown in fig. 2.

The L9704 circuit compares the input current with the current through the internal reference resistor. The device is designed to work with an external input series resistor of $R_{IN1\text{-}8} = 1k\Omega$. With this input resistor the contact current, when the contact is closed and the device activated (EN = LOW) is

$$I_{IN} = \frac{V_{BAT} + \Delta V_{BAT} - 2V}{1K\Omega} \qquad (1)$$

For this calculation the limit value of the V_{IN} (saturation voltage of 2V) was considered so that the lowest limit value of I_{IN} is calculated in (1).

The function of the circuit can be demonstrated with the transfer characteristics, showing the output status as a function of the input resistor R_I, shown in figure 3. The input resistor is a sum of the R_{IN} and the contact resistance R_{CON} or R_{COFF}, for the closed contact :

$$R_I = R_{IN} + R_{CON}, \qquad (2)$$

and for the open contact :

$$R_I = R_{IN} + R_{COFF}. \qquad (3)$$

The output goes HIGH when the input resistance increases above 6.5kΩ (typical value) and goes LOW, when the input resistance decreases below 4.8KΩ (typical value). The limit values of R_I = 1.1KΩ for LOW and R_I = 29kΩ for HIGH implies that a contact with $R_{CON} = 100\Omega$ (at I_{IN} = 10mA) will be recognized as ON = LOW and a contact with R_{COFF} = 28kΩ will be recognized as OFF = HIGH. These limits are valid within the supply voltage range $5V \le V_S \le 16V$, the battery voltage potential difference of $|\Delta VBAT| \le 0.1V_{BAT}$ and the variation of the reverse battery protection diode D1 voltage from 0.5V to 1V.

The internal clamping diodes at the contact monitoring inputs, together with the external contact series resistors R_{IN}, allows the device to withstand transients at the contact connection. The contact series resistor R_{IN} limits the input current at the transient.

The dynamic behaviour of the circuit is defined by the times t_{do} and t_{dTS}. When the contact becomes open, the input capacitor C_{IN} must be charged through the resistor R_{IN}. In this case the total delay time may also be influenced by the time constant R_{IN} C_{IN}. The delay time t_{dTS}, when disabling the device is defined only by the internal circuitry. In both cases, an external output capacitance less than 50pF is assumed, the internal output capacitances of the three-state buffers are less than 5pF.

Figure 2 : The Contact Sense Input Connection with the Contact Equivalent Circuit.

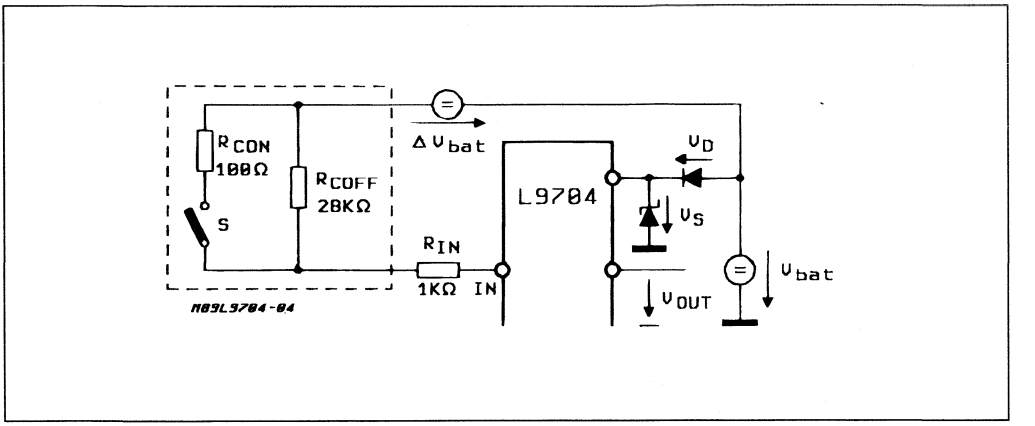
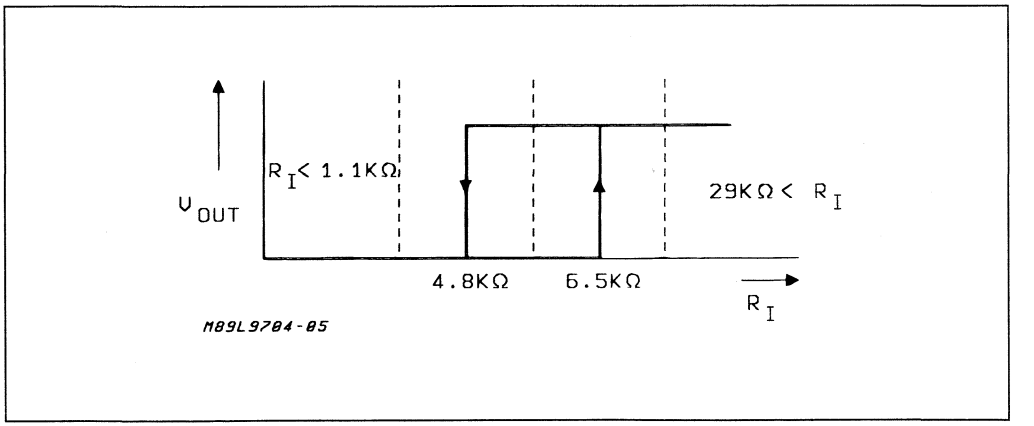


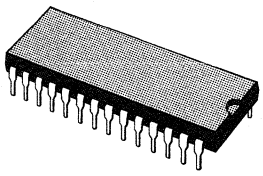
Figure 3 : The Output Voltage as a Function of the Input Resistance at the Corresponding Contact Sense Input.



AUTOMOTIVE LAMPS AND FUSES MONITOR CIRCUIT

ADVANCE DATA

- FOUR DOUBLE CONTROL CHANNELS
- SEPARATE FAULT DETECTION FOR LAMP AND FUSE
- INTERNAL LATCH FOR STOP LAMP FAULT
- INTERNAL PROGRAMMABLE DELAY TO PREVENT FALSE DETECTION



28 LEAD PLASTIC DIP

ORDER CODE : TEA7203

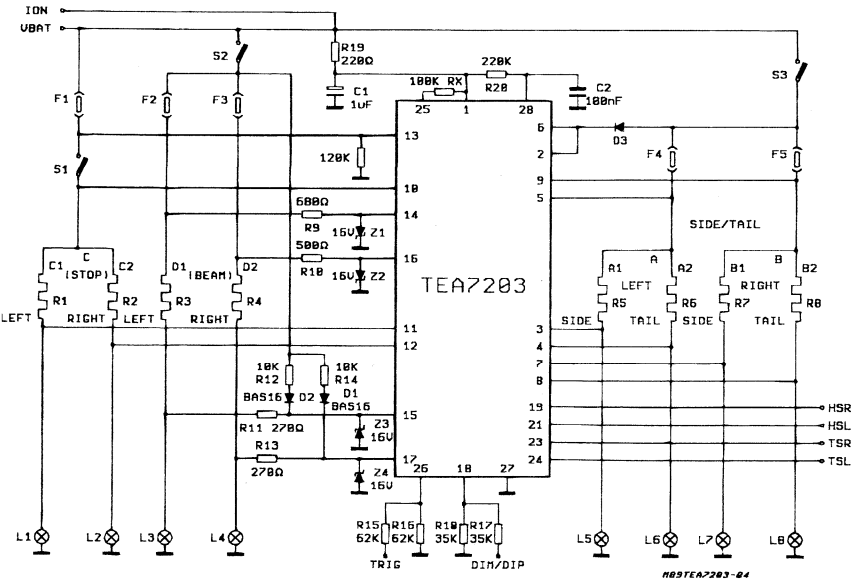
DESCRIPTION

The TEA7203 is a device particularly suited to control lamps and corresponding fuses in the automotive environment.

Furthermore an internal control channel is dedicated to the stop lamps and is able to check the brake contact status.

The internal programmable delay avoids false fault alarms due to spurious signals during the transients.

APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
V_1	Supply Voltage	35		V
V_{13}, V_{14}, V_{15}, V_{16}, V_{17}, V_{26}, V_{28}	Input Voltages	35		V
V_2, V_3, V_4, V_5, V_6, V_7, V_8, V_9, V_{10}, V_{11}, V_{12}	Transient Overvoltages (= 2ms) (= 300ms)	– 100	100 80	V V
V_{19}, V_{21}, V_{23}, V_{24}	Transient Overvoltages (through external resistor R = 250Ω) (= 2ms) (= 300ms)	– 100	100 80	V V
I_{19}, I_{21}, I_{23}, I_{24}	Input Current		50	mA
T_J, T_{STG}	Junction and Storage Temperature Range	– 55 to 150		°C

PIN OUT

1	Vcc		15	D1	CHANNEL CONTROL
2	A	CHANNEL FUSE CONTROL	16	D2	CHANNEL REFERENCE
3	A	CHANNEL LAMP CONTROL	17	D2	CHANNEL CONTROL
4	A	CHANNEL LAMP CONTROL	18		DIM/DIP
5	A	CHANNEL REFERENCE	19		OUTPUT
6	B	CHANNEL FUSE CONTROL	20		NC
7	B	CHANNEL LAMP CONTROL	21		OUTPUT
8	B	CHANNEL LAMP CONTROL	22		NC
9	B	CHANNEL REFERENCE	23		OUTPUT
10	C	CHANNEL REFERENCE (STOPS)	24		OUTPUT
11	C	CHANNEL LAMP CONTROL	25		ADDITIONAL TRIGGER
12	C	CHANNEL LAMP CONTROL	26		TRIGGER SIGNAL CONTROL
13	C	CHANNEL FUSE CONTROL	27		GROUND
14	D1	CHANNEL REFERENCE	28		OSCILLATOR

INPUT/OUTPUT MATRIX

INPUT	ACTIVATED OUTPUT
2	21, 24
3	21
4	24
6	19, 23
7	19
8	23
11	24
12	23
13	23, 24
15	21
17	19

FUNCTIONAL DESCRIPTION

A, B CHANNELS

LAMPS CONTROL. The lamps supply current flows through two shunt resistors. The shunt drop voltage value is compared with an internal reference ; if this drop is too low a fault indication is sent to a digital timer circuit. When the delay time is exceeded, the corresponding output is activated.

FUSES CONTROL. An input similar to the lamp inputs is connected to the high side fuse but, in this case, an external diode supplies an additional offset. If the fuse is destroyed, this input becomes active and signals the fault. When the fault condition ceases, the alarm is immediately suppressed. The faults are not detected only when the A and B channels are switched off.

D_1, D_2 CHANNELS

LAMPS CONTROL. Two different resistors are connected to the inputs ; the input currents cause two voltage drops. In this way, the reference voltage is given by the voltage drops difference.

FUSES CONTROL. An external diode connected to the fuse, and normally disactivated, is directly biased when the fuse destruction occurs, supplying the input comparator to signal the fault condition. In this circuit configuration the input current can be ≤ 100mA. The D1, D2 channel inputs are not internally protected against the overvoltages.

DIM/DIP pin function : it allows to inhibit the alarms on D_1, D_2 channels.

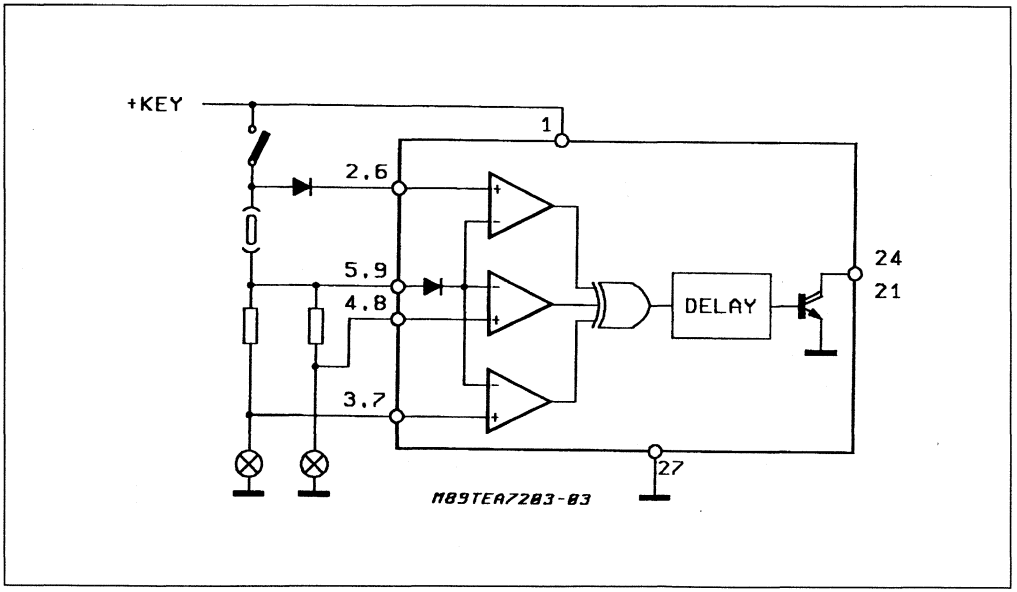
C1, C2 CHANNELS (STOP)

- Every fault on the C1, C2 channels is latched by an internal flip-flop and is signaled at the output until the reset signal is generated.
- Brakes and fuses contact control. Through the Trigger pin, at the start, the flip-flop receive a SET signal and a fault condition is signaled. To have a RESET signal the fuse must be not damaged, pin 13 voltage value must be higher than 1.9V and the contact must be closed.
- Lamps control : if the lamps current is unsufficient, the corresponding flip-flop receives a SET signal. SET has priority over RESET.

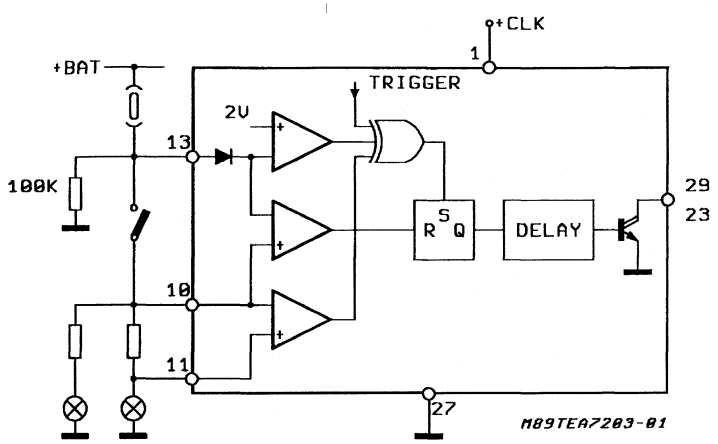
FAULT WARNING LED CONTROL

A Low level at the Trigger input activates the outputs. This activation continues for the STOP lamps until the flip-flop circuits are resetted.

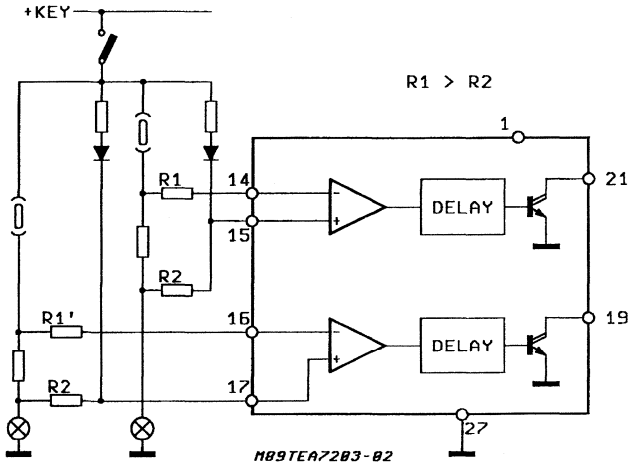
A, B CHANNELS



C CHANNEL



D CHANNEL



ELECTRICAL CHARACTERISTICS $T_J = -40 + 85°C$ $V_{CC} = 13.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit
V1	Operating Supply Voltage	9	13.5	16	V
I1	Quiescent Current			20	mA

TIMER CIRCUIT

Symbol	Parameter	Min.	Typ.	Max.	Unit
I28	Oscillator Current	2	5	200	nA
	Resistor Range		1		MΩ
	Fault Delay Time (with R = 1MΩ ; C = 100nF)		1.25		s

TRIGGER

Symbol	Parameter	Min.	Typ.	Max.	Unit
V26	Low Threshold Voltage (all active inputs)	2.6	2.8		V
I26	Low Current Level			500	µA
V26	High Treshold Voltage			10.5	V
I26	Input Current (high status) V26 = 10.5...16V		0	200	µA

OUTPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
I19, 21 I23, 24	Leakage Output Current (output high)			100	µA
V19, 21, V23, 24	Output Saturation Voltage			1.5	V
	@I_{OUT} = 25mA				

DIM/DIP DIP Function (low level)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V18	Inhibit Threshold	0.4	1.3	9	V
	Threshold Input Current (externally limited)			50	µA

ELECTRICAL CHARACTERISTICS (continued)

CHANNELS A, B

Symbol	Parameter	Min.	Typ.	Max.	Unit
I5, I9	Reference Input Current	50	100	200	µA
I3, 4, 7, 8	Input Current (S.C. lamps)	70	150	400	µA
I2, 6	Input Current			2	mA
V5-V2, 3, 4 V9-V6, 7, 8	Voltage Reference	9	13	17	mV

CHANNELS C1, C2

Fault Flip-flop Truthtable

S	R	Fault Indication
0	0	Previous Status
0	1	0
1	0	1
1	1	1

SET FUNCTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
V10-V11, 12	Trigger (p.m.) Low Status Lamps Input Voltage	9	13	17	mV
V13	Fuses Input Voltage	0		1.9	V
I10	Reference Current	50	100	200	µA
I11, 12	Input Current (S.C. lamps)	70	150	400	µA
I13	Standby Current (pin Vcc open)			200	µA
V13-V10	Reset Threshold Voltage		0.7		V

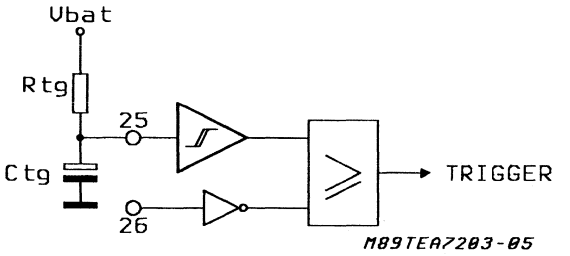
CHANNELS D1, D2

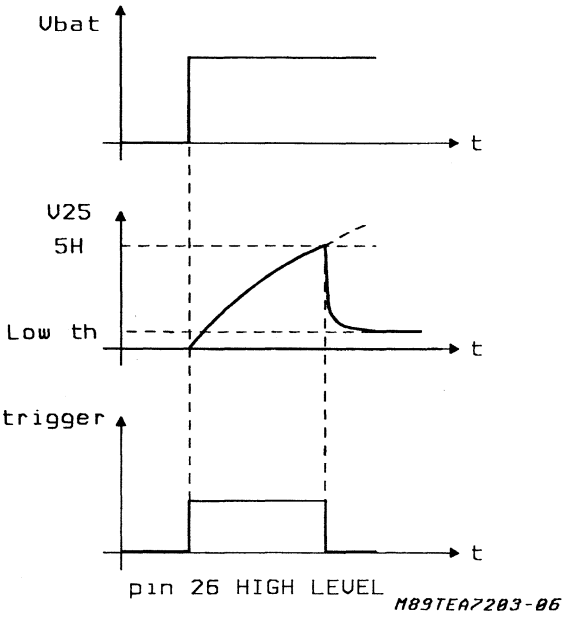
Symbol	Parameter	Min.	Typ.	Max.	Unit
I14, 15 I16, 17	Input Currents	52.5 70	75 100	105 140	µA µA
V14-V15 V16-V17	Input Comparator Offsets (fault for V15 > V14 or V17 > V16)	– 4 – 4	0 0	4 4	mV mV

ADDITIONAL TRIGGER INPUT

Symbol	Parameter	Min.	Typ.	Max.	Unit
V25	High Threshold	3.7	4.4	5.1	V
V25	Low Threshold		2.1		V
I25	Leakage Input Current		0	20	µA

ADDITIONAL INPUT TRIGGER





SGS-THOMSON MICROELECTRONICS

BUZ71
BUZ71FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

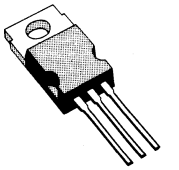
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
BUZ71	50 V	0.1 Ω	14 A
BUZ71FI	50 V	0.1 Ω	12 A

- VERY FAST SWITCHING
- LOW DRIVE ENERGY FOR EASY DRIVE, REDUCED SIZE AND COST
- HIGH PULSED CURRENT - 56A FOR POWER APPLICATIONS

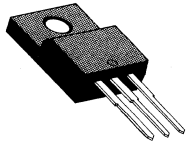
INDUSTRIAL APPLICATIONS:

- POWER ACTUATORS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits in applications such as power actuator driving, motor drive including brushless motors, robotics, actuators and many other uses in automotive control applications. They also find use in DC/DC converters and uninterruptible power supplies.

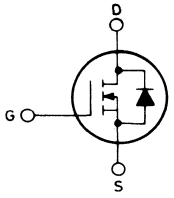


TO-220



ISOWATT 220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50		V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	50		V
V_{GS}	Gate-source voltage	±20		V
I_{DM}	Drain current (pulsed) $T_c=25°C$	56		A
		BUZ71	**BUZ71FI**	
I_D ■	Drain current (continuous) $T_c=30°C$	14	12	A
P_{tot} ■	Total dissipation at $T_c<25°C$	40	30	W
T_{stg}	Storage temperature	−55 to 150		°C
T_j	Max. operating junction temperature	150		°C
	DIN humidity category (DIN 40040)	E		
	IEC climatic category (DIN IEC 68-1)	55/150/56		

■ See note on ISOWATT 220 in this datasheet

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	3.1	4.16	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	75		°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

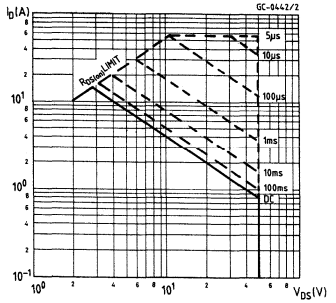
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 9 A			0.1	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 9 A	3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			650 450 280	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3 A V_{GS} = 10 V			30 85 90 110	ns ns ns ns

■ See note on ISOWATT 220 in this datasheet

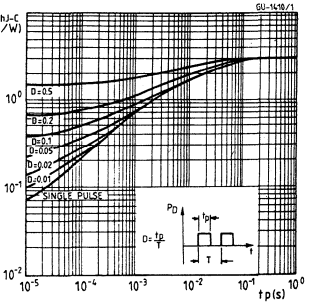
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} Source-drain current (pulsed)				14 56	A A
V_{SD} Forward on voltage	I_{SD} = 28 A V_{GS} = 0			1.8	V
t_{rr} Reverse recovery time			120		ns
Q_{rr} Reverse recovered charge	I_{SD} = 14 A di/dt = 100A/μs		0.15		μC

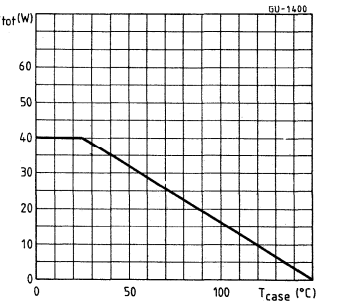
Safe operating areas



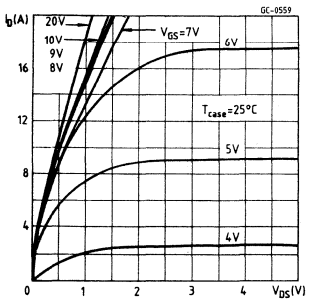
Thermal impedance



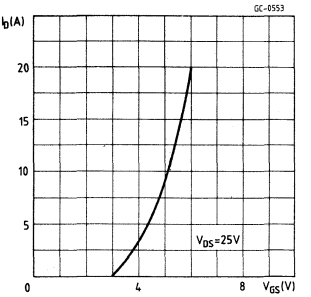
Derating curve



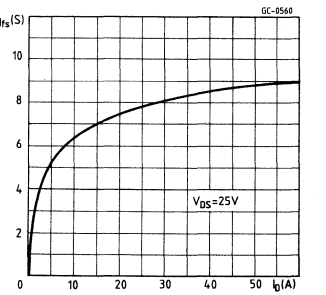
Output characteristics



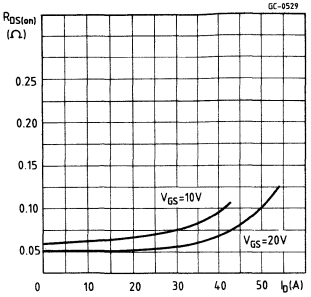
Transfer characteristics



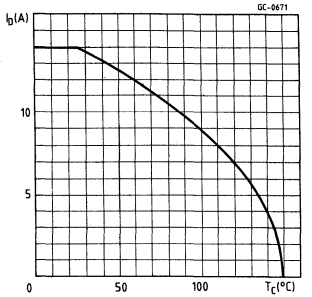
Transconductance



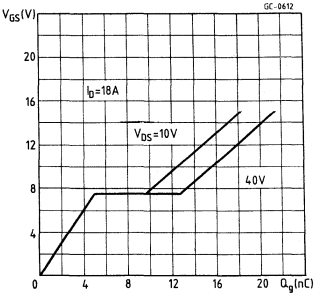
Static drain-source on resistance



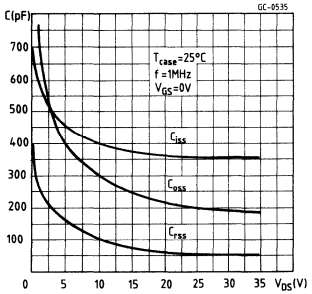
Maximum drain current vs temperature



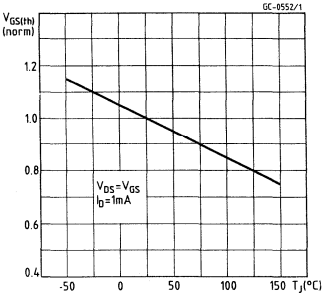
Gate charge vs gate-source voltage



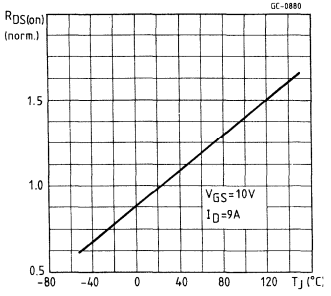
Capacitance variation



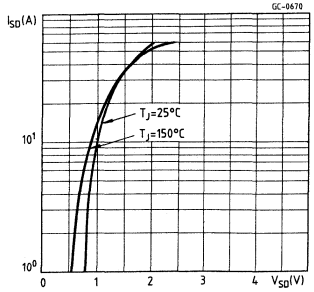
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ-C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

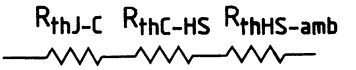
$$Z_{th} = R_{thJ-C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ-C} + R_{thC-HS} + R_{thHS-amb}$$

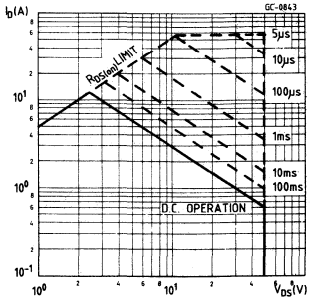
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

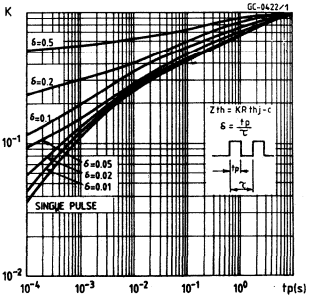


ISOWATT DATA

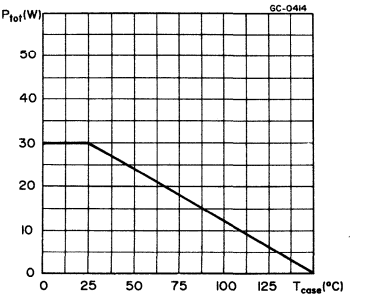
Safe operating areas



Thermal impedance



Derating curve



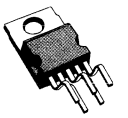
10W CAR RADIO AUDIO AMPLIFIER

DESCRIPTION

The TDA2003 has improved performance with the same pin configuration as the TDA 2002. The additional features of TDA 2002, very low number of external components, ease of assembly, space and cost saving, are maintained.

The device provides a high output current capability (up to 3.5 A) very low harmonic and cross-over distortion.

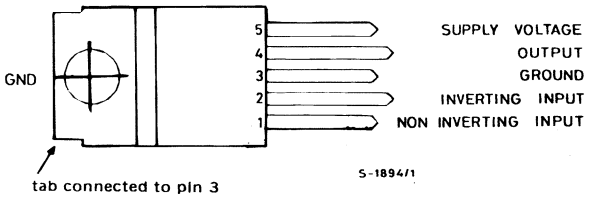
Completely safe operation is guaranteed due to protection against DC and AC short circuit between all pins and ground, thermal over-range,load dump voltage surge up to 40 V and fortuitous open ground.



PENTAWATT

ORDER CODE : TDA2003H
TDA2003V

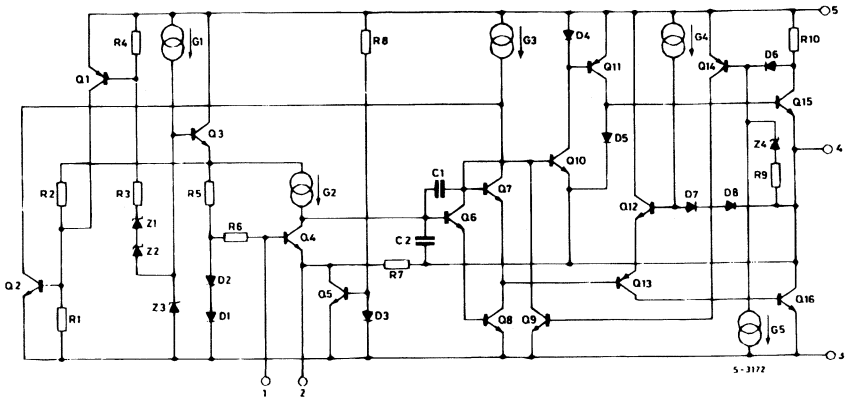
PIN CONNECTION (top view)



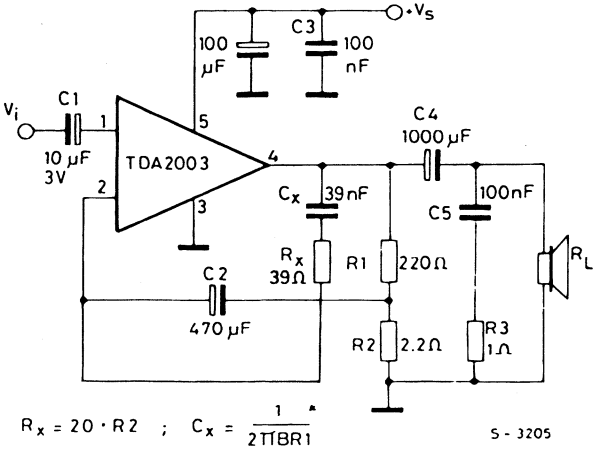
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Peak Supply Voltage (50ms)	40	V
V_s	DC Supply Voltage	28	V
V_s	Operating Supply Voltage	18	V
I_o	Output Peak Current (repetitive)	3.5	A
I_o	Output Peak Current (non repetitive)	4.5	A
P_{tot}	Power Dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

SCHEMATIC DIAGRAM



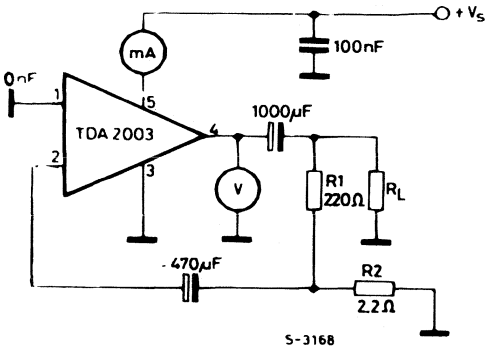
TEST CIRCUIT



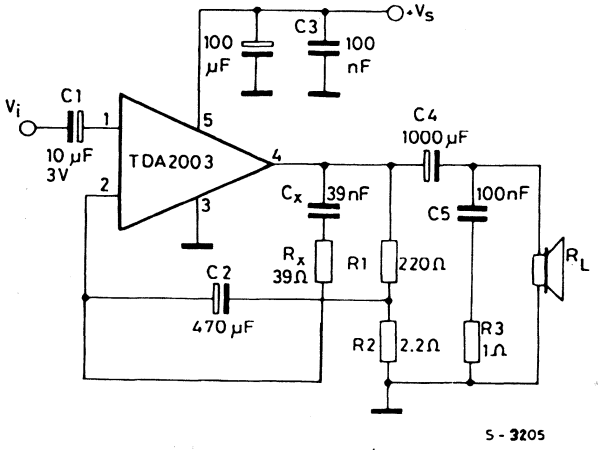
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

DC TEST CIRCUIT



AC TEST CIRCUIT



$$Rx = 20 \cdot R2 \; ; \; Cx = \frac{1}{2\,\Pi BR1}$$

ELECTRICAL CHARACTERISTICS (V_5 = 14.4 V, T_{amb} = 25 °C unless otherwise specified)

DC CHARACTERISTICS (refer to DC test circuit)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		8		18	V
V_o	Quiescent Output Voltage (pin 4)		6.1	6.9	7.7	V
I_d	Quiescent Drain Current (pin 5)			44	50	mA

ELECTRICAL CHARACTERISTICS (continued)

AC CHARACTERISTICS (refer to AC test circuit, G_v = 40 dB)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
P_o	Output Power	d = 10 % R_L = 4 Ω f = 1 kHz R_L = 2 Ω R_L = 3.2 Ω R_L = 1.6 Ω	5.5 9	6 10 7.5 12		W W W W
$V_{i(rms)}$	Input Saturation Voltage		300			mV
V_i	Input Sensitivity	f = 1 kHz P_o = 0.5 W R_L = 4 Ω P_o = 6 W R_L = 4 Ω P_o = 0.5 W R_L = 2 Ω P_o = 10 W R_L = 2 Ω		 14 55 10 50		 mV mV mV mV
B	Frequency Response (– 3 dB)	P_o = 1 W R_L = 4 Ω		40 to 15,000		Hz
d	Distortion	f = 1 kHz P_o = 0.05 to 4.5 W R_L = 4 Ω P_o = 0.05 to 7.5 W R_L = 2 Ω		 0.15 0.15		 % %
R_i	Input Resistance (pin 1)	f = 1 kHz	70	150		kΩ
G_V	Voltage Gain (open loop)	f = 1 kHz f = 10 kHz		80 60		dB dB
G_V	Voltage Gain (closed loop)	f = 1 kHz R_L = 4 Ω	39.3	40	40.3	dB
^eN	Input Noise Voltage (0)			1	5	μV
^iN	Input Noise Current (0)			60	200	pA
η	Efficiency	f = 1 kHz P_o = 6 W R_L = 4 Ω P_o = 10 W R_L = 2 Ω		 69 65		 % %
SVR	Supply Voltage Rejection	f = 100 Hz V_{ripple} = 0.5 V R_g = 10 kΩ R_L = 4 Ω	 30	 36		 dB

(0) Filter with noise bandwidth : 22 Hz to 22 kHz

Figure 1 : Quiescent Output Voltage vs. Supply Voltage.

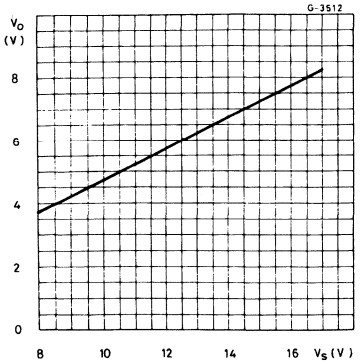


Figure 2 : Quiescent Drain Current vs. Supply Voltage.

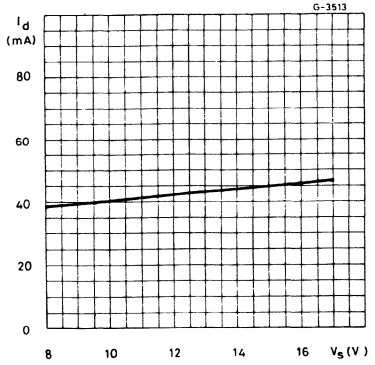


Figure 3 : Output Power vs. Supply Voltage.

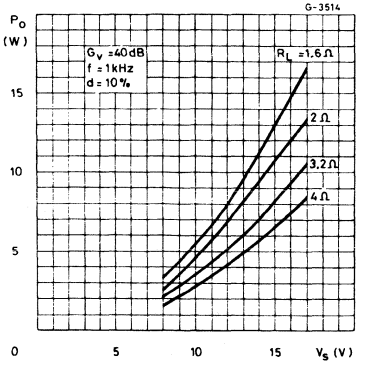


Figure 4 : Output Power vs. Load Resistance R_L.

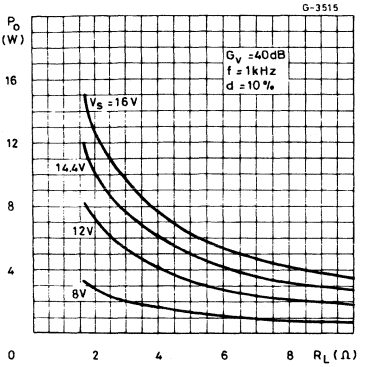


Figure 5 : Gain vs. Input Sensitivity.

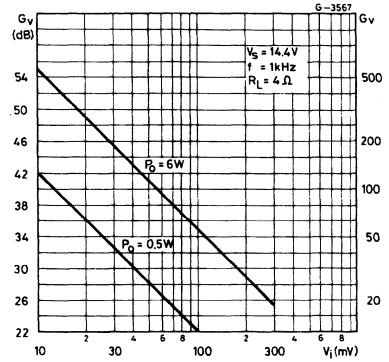


Figure 6 : Gain vs. Input Sensitivity.

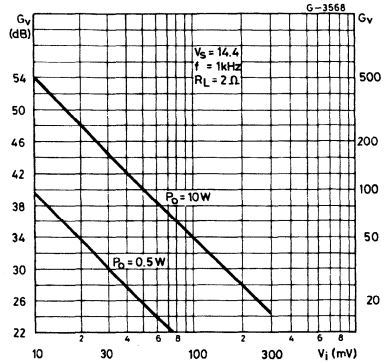


Figure 7 : Distortion vs. Output Power.

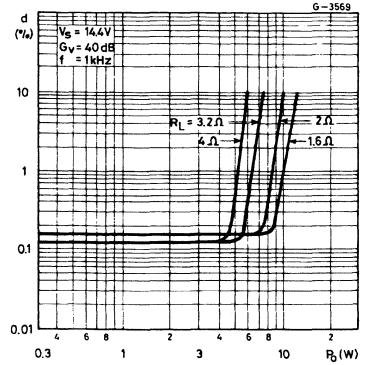


Figure 8 : Distortion vs. Frequency.

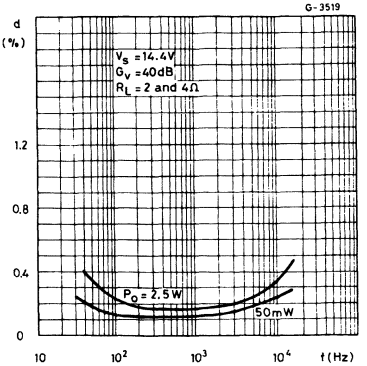


Figure 9 : Supply Voltage Rejection vs. Voltage Gain.

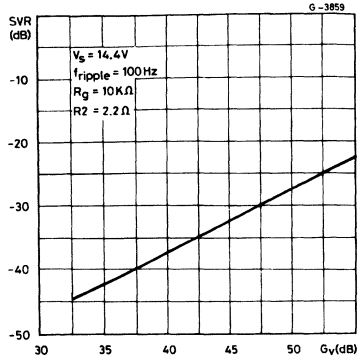


Figure 10 : Supply Voltage Rejection vs. Frequency.

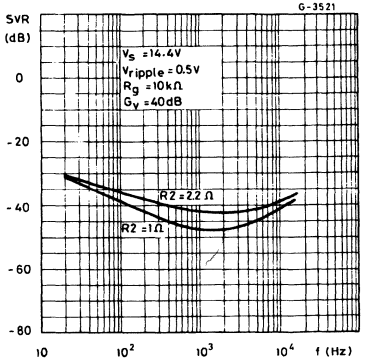


Figure 11 : Power Dissipation and Efficiency vs. Output Power (R_L = 4 Ω).

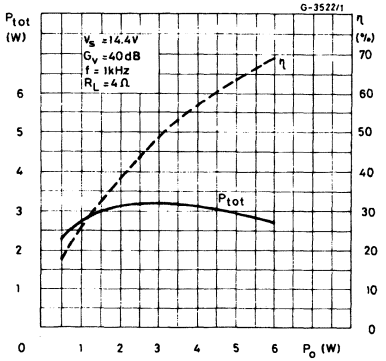


Figure 12 : Power Dissipation and Efficiency vs. Output Power (R_L = 2 Ω).

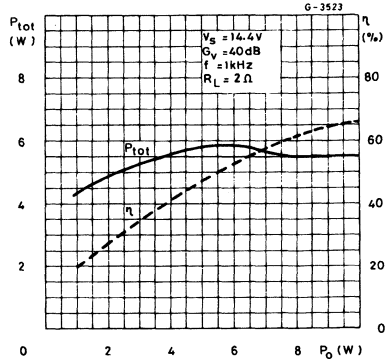


Figure 13 : Maximum Power Dissipation vs. Supply Voltage (sine wave operation).

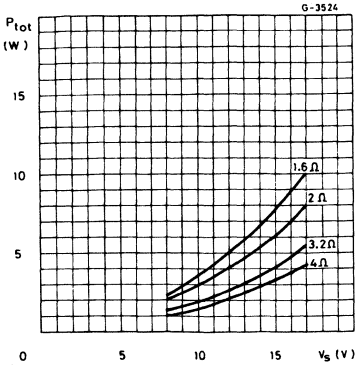


Figure 14 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

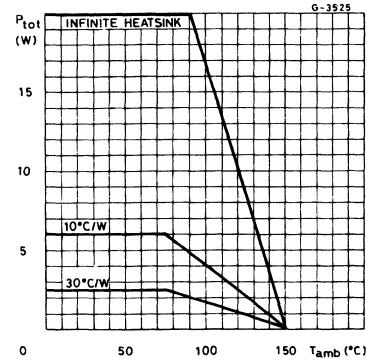
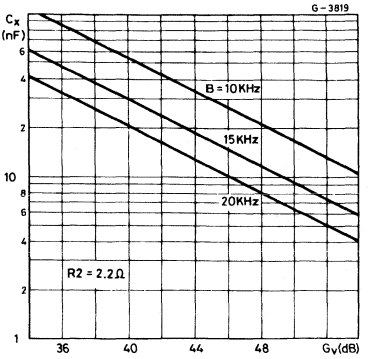


Figure 15 : Typical Values of Capacitor (C_X) for Different Values of Frequency Response (B).



APPLICATION INFORMATION

Figure 16 : Typical Application Circuit.

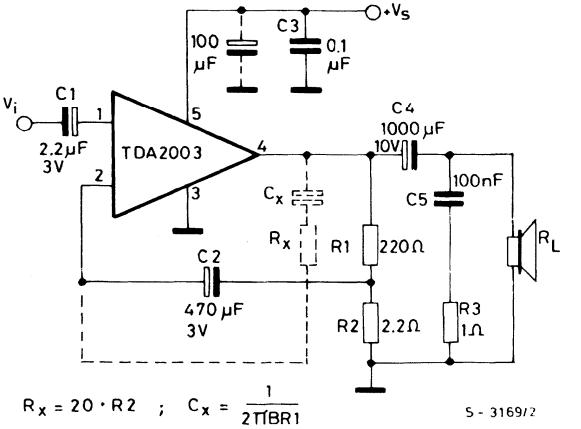


Figure 17 : P.C. Board and Component Layout for the Circuit of Fig. 16 (1 : 1 scale).

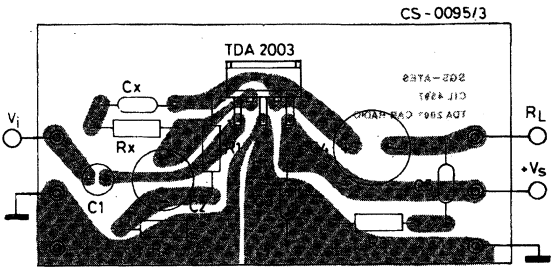
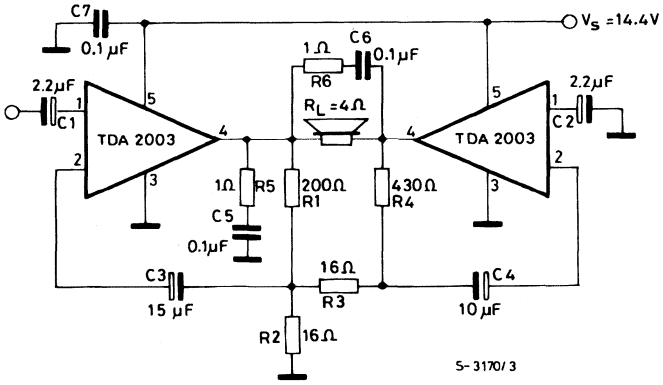


Figure 18 : 20 W Bridge Configuration Application Circuit (*).



(*) The values of the capacitors C3 and C4 are different to optimize the SVR (typ. = 40 dB)

Figure 19 : P.C. Board and Component Layout for the Circuit of Fig. 18 (1 : 1 scale).

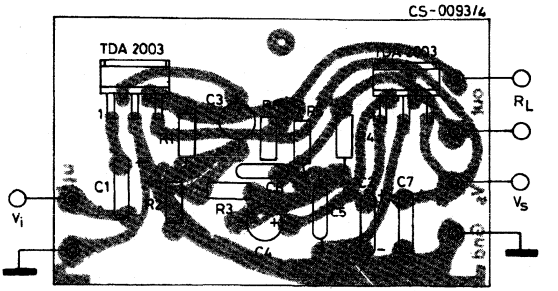
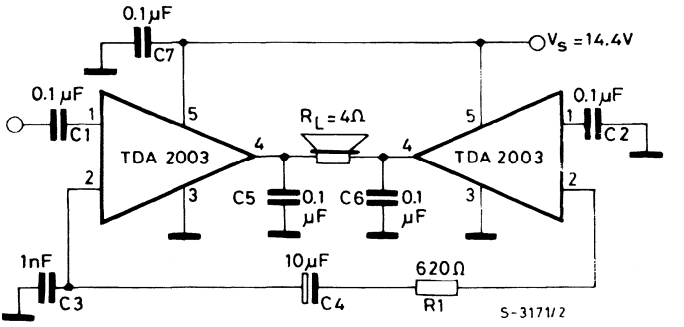
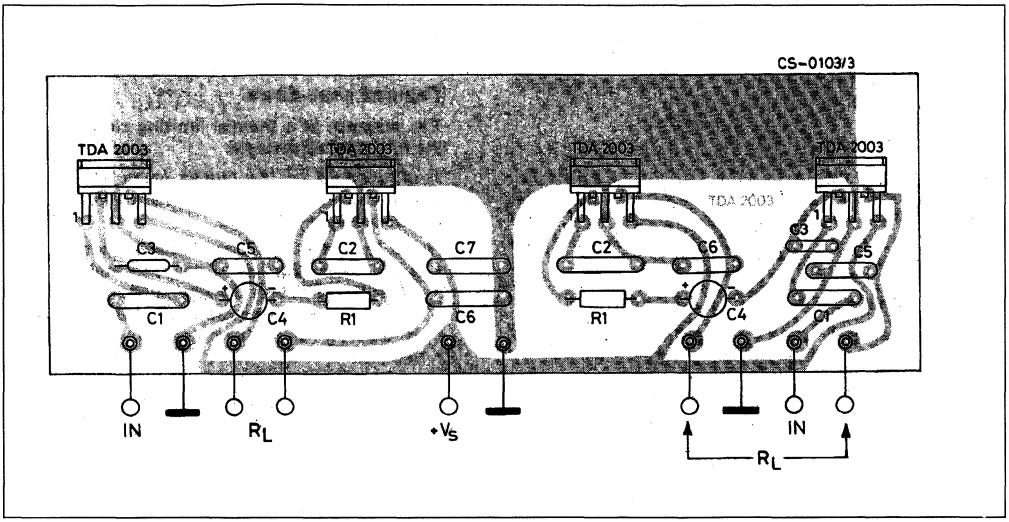


Figure 20 : Low Cost Bridge Configuration Application Circuit (*) (P_o = 18 W).



(*) In this application the device can support a short circuit between every side of the loudspeaker and ground.

Figure 21 : P.C. Board and Component Layout for the Low-cost Bridge Amplifier of Fig. 20, in Stereo Version (1 : 1 scale).



BUILT-IN PROTECTION SYSTEMS

LOAD DUMP VOLTAGE SURGE

The TDA 2003 has a circuit which enables it to withstand a voltage pulse train, on pin 5, of the type shown in fig. 23. If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 5, in order to assure that the pulses at pin 5 will be held within the limits shown in fig. 22.

A suggested LC network is shown in fig. 23. With this network, a train of pulses with amplitude up to 120 V and width of 2 ms can be applied at point A. This type of protection is ON when the supply voltage (pulsed or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

SHORT-CIRCUIT (AC AND DC CONDITIONS)

The TDA 2003 can withstand a permanent short-circuit on the output for a supply voltage up to 16V.

POLARITY INVERSION

High current (up to 5A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 1A fuse (normally connected in series with the supply).

This feature is added to avoid destruction if, during fitting to the car, a mistake on the connection of the supply is made.

OPEN GROUND

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA 2003 protection diodes are included to avoid any damage.

INDUCTIVE LOAD

A protection diode is provided between pin 4 and 5 (see the internal schematic diagram) to allow use of the TDA 2003 with inductive loads.In particular, the TDA 2003 can drive a coupling transformer for audio modulation.

DC VOLTAGE

The maximum operating DC voltage on the TDA 2003 is 18V.

However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries were series connected to crank the engine.

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), oran excessive ambient temperature can be easily withstood.

2) the heat-sink can have a smaller factor comparedwith that of a conventional circuit.There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced.

Figure 22.

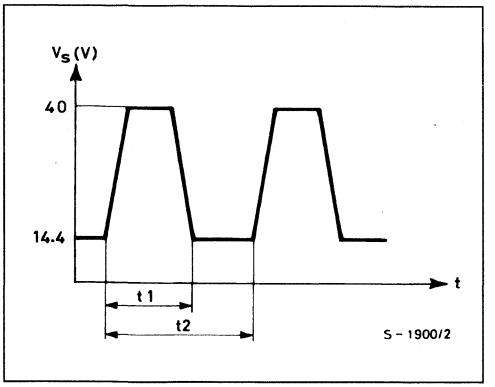


Figure 23.

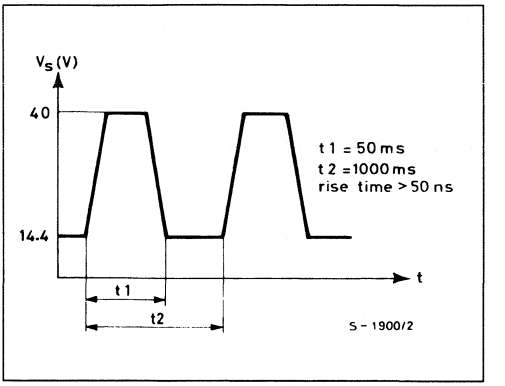


Figure 24 : Output Power and Drain Current vs. Case Temperature (R_L = 4 Ω).

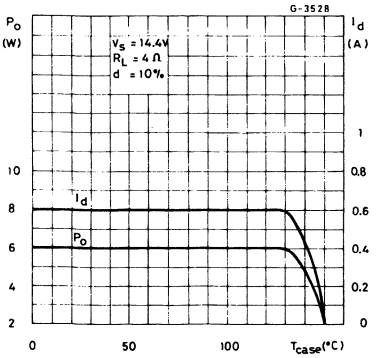
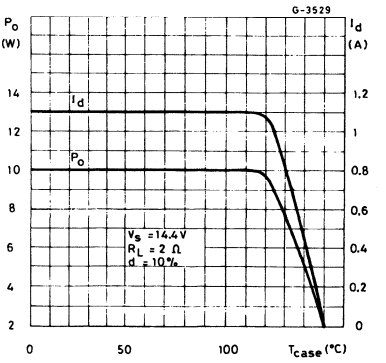


Figure 25 : Output Power and Drain Current vs. Case Temperature (R_L = 2 Ω).



PRACTICAL CONSIDERATION

PRINTED CIRCUIT BOARD

The layout shown in fig. 17 is recommended. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground of the output through which a rather high current flows.

ASSEMBLY SUGGESTION

No electrical insulation is required between the package and the heat-sink. Pin length should be as short as possible. The soldering temperature must not exceed 260 °C for 12 seconds.

APPLICATION SUGGESTIONS

The recommended component values are those shown in the application circuits of fig.16. Different values can be used. The following table is intended to aid the car-radio designer.

Component	Recommended Value	Purpose	Larger Than Recommended Value	Smaller Than Recommended Value
C1	2.2 μF	Input DC Decoupling		Noise at Switch-on, Switch-off
C2	470 μF	Ripple Rejection		Degradation of SVR
C3	0.1 μF	Supply Bypassing		Danger of Oscillation
C4	1000 μF	Output Coupling to Load		Higher Low Frequency Cutoff
C5	0.1 μF	Frequency Stability		Danger of Oscillation at High Frequencies with Inductive Loads
C_X	$\cong \frac{1}{2\pi B R1}$	Upper Frequency Cutoff	Lower Bandwidth	Larger Bandwidth
R1	(Gv – 1) • R2	Setting of Gain		Increase of Drain Current
R2	2.2 Ω	Setting of Gain and SVR	Degradation of SVR	
R3	1 Ω	Frequency Stability	Danger of Oscillation at High Frequencies with Inductive Loads	
R_X	≅ 20 R2	Upper Frequency Cutoff	Poor High Frequency Attenuation	Danger of Oscillation

10 + 10W STEREO AMPLIFIER FOR CAR RADIO

Its main features are :

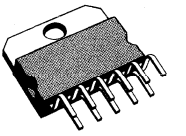
Low distortion.

Low noise.

High reliability of the chip and of the package with additional safety during operation thanks to protections against :

- OUTPUT AC SHORT CIRCUIT TO GROUND
- VERY INDUCTIVE LOADS
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE SURGE
- FORTUITOUS OPEN GROUND

Space and cost saving : very low number of external components, very simple mounting system with no electrical isolation between the package and the heatsink.



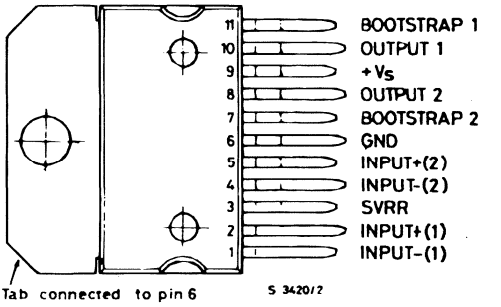
Multiwatt 11®

ORDER CODE : TDA2004

DESCRIPTION

The TDA2004 is a class B dual audio power amplifier in MULTIWATT® package specifically designed for car radio applications ; stereo amplifiers are easily designed using this device that provides a high current capability (up to 3.5 A) and that can drive very low impedance loads (down to 1.6Ω).

PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Operating Supply Voltage	18	V
V_s	DC Supply Voltage	28	V
V_s	Peak Supply Voltage (for 50 ms)	40	V
I_o (*)	Output Peak Current (non repetitive t = 0.1 ms)	4.5	A
I_o (*)	Output Peak Current (repetitive f ≥ 10 Hz)	3.5	A
P_{tot}	Power Dissipation at T_{case} = 60 °C	30	W
T_j, T_{stg}	Storage and Junction Temperature	– 40 to 150	°C

(*) The max. output current is internally limited.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_{amb} = 25 °C, G_v = 50 dB, $R_{th\ (heatsink)}$ = 4 °C/W, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage			8		18	V
V_o	Quiescent Output Voltage	V_s = 14.4 V		6.6	7.2	7.8	V
		V_s = 13.2 V		6.0	6.6	7.2	V
I_d	Total Quiescent Drain Current	V_s = 14.4 V			65	120	mA
		V_s = 13.2 V			62	120	mA
I_{SB}	Stand-by Current	Pin 3 Grounded			5		mA
P_o	Output Power (each channel)	f = 1 kHz	d = 10 %				
		V_s = 14.4 V					
			R_L = 4 Ω	6	6.5		W
			R_L = 3.2 Ω	7	8		W
			R_L = 2 Ω	9	10 (*)		W
			R_L = 1.6 Ω	10	11		W
		V_s = 13.2 V					
			R_L = 3.2 Ω	6	6.5		W
			R_L = 1.6 Ω	9	10		W
		V_s = 16 V					
			R_L = 2 Ω		12		W
d	Distortion (each channel)	f = 1 kHz					
		V_s = 14.4V	R_L = 4 Ω				
		P_o = 50 mW to 4 W			0.2	1	%
		V_s = 14.4 V	R_L = 2 Ω				
		P_o = 50 mW to 6 W			0.3	1	%
		V_s = 13.2 V	R_L = 3.2 Ω				
		P_o = 50 mW to 3 W			0.2	1	%
		V_s = 13.2 V	R_L = 1.6 Ω				
		P_o = 50 mW to 6 W			0.3	1	%
CT	Cross Talk	V_s = 14.4 V					
		V_o = 4 V_{rms}	R_L = 4 Ω				
		f = 1 kHz		50	60		dB
		f = 10 kHz	R_g = 5 kΩ	40	45		dB
V_i	Input Saturation Voltage			300			mV
R_i	Input Resistance (non inverting input)	f = 1 kHz		70	200		kΩ

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_L	Low Frequency Roll Off (– 3 dB)	R_L = 4 Ω R_L = 2 Ω R_L = 3.2 Ω R_L = 1.6 Ω			35 50 40 55	Hz Hz Hz Hz
f_H	High Frequency Roll Off (– 3 dB)	R_L = 1.6 Ω to 4 Ω	15			kHz
G_v	Voltage Gain (open loop)	f = 1 kHz		90		dB
G_v	Voltage Gain (closed loop)	f = 1 kHz	48	50	51	dB
	Closed Loop Gain Matching			0.5		dB
e_N	Total Input Noise Voltage	R_g = 10 kΩ (°)		1.5	5	μV
SVR	Supply Voltage Rejection	f_{ripple} = 100 Hz R_g = 10 kΩ C_3 = 10 μF V_{ripple} = 0.5 V_{rms}	35	45		dB
η	Efficiency	V_s = 14.4 V f = 1 kHz R_L = 4 Ω P_o = 6.5 W R_L = 2 Ω P_o = 10 W V_s = 13.2 V f = 1 kHz R_L = 3.2 Ω P_o = 6.5 W R_L = 1.6 Ω P_o = 10 W		 70 60 70 60		 % % % %
T_j	Thermal Shut Down Junction Temperature			145		°C

Notes : (*) 9.3W without Bootstrap
(**) Bandwith Filter : 22Hz to 22KHz.

Figure 1 : Test and Application Circuit.

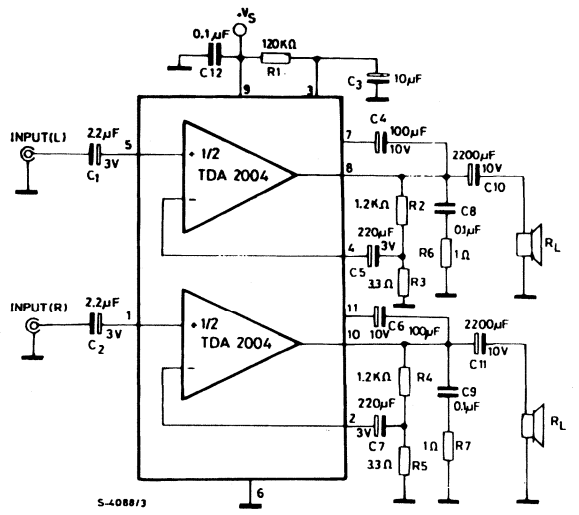


Figure 2 : P.C. Board and Component layout (scale 1 : 1).

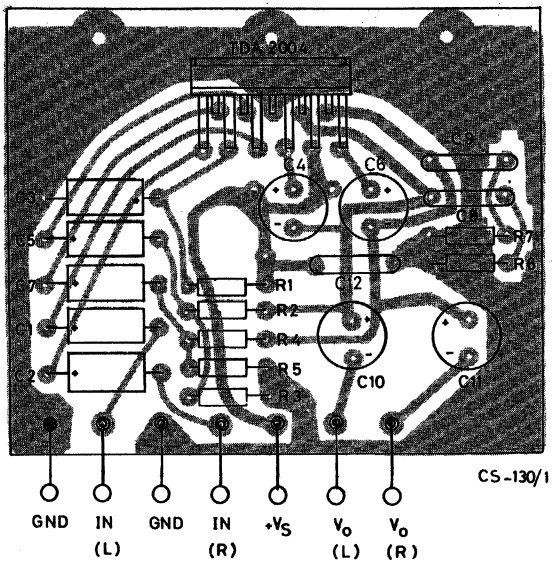


Figure 3 : Quiescent Output Voltage vs. Supply Voltage.

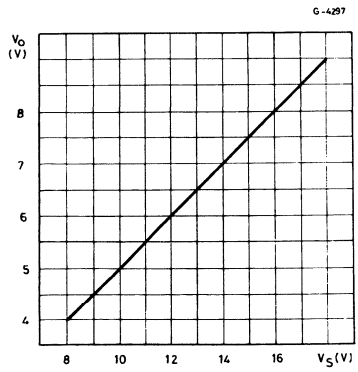


Figure 4 : Quiescent Drain Current vs. Supply Voltage.

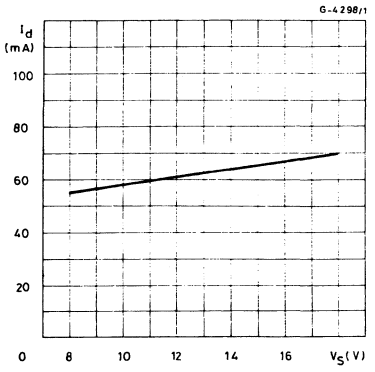


Figure 5 : Distortion vs. Output Power.

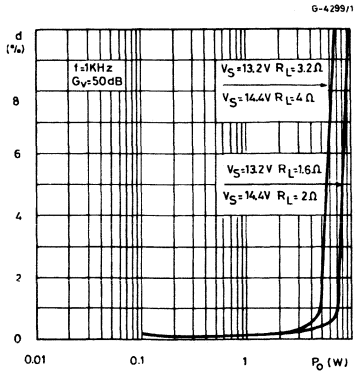


Figure 6 : Output Power vs. Supply Voltage.

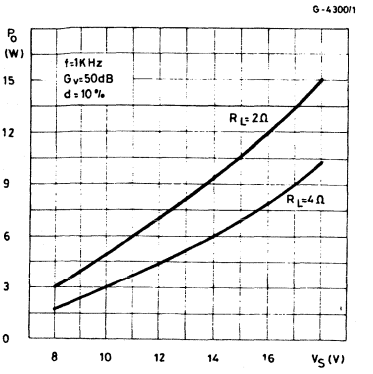


Figure 7 : Output Power vs. Supply Voltage.

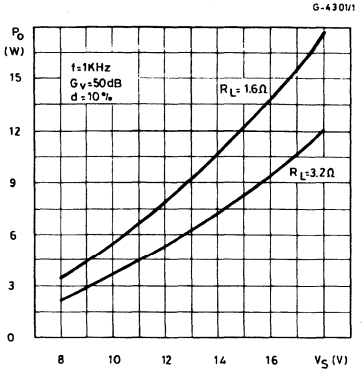


Figure 8 : Distortion vs. Frequency.

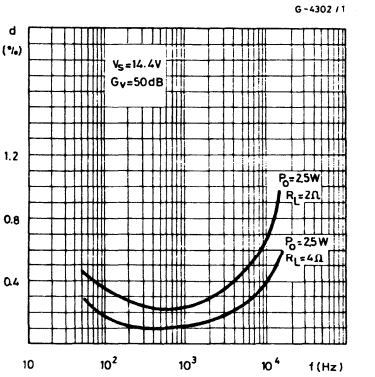


Figure 9 : Distortion vs. Frequency.

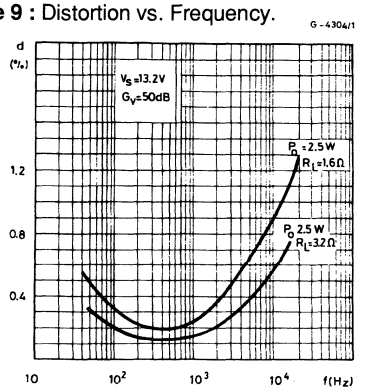


Figure 10 : Supply Voltage Rejection vs. C_3.

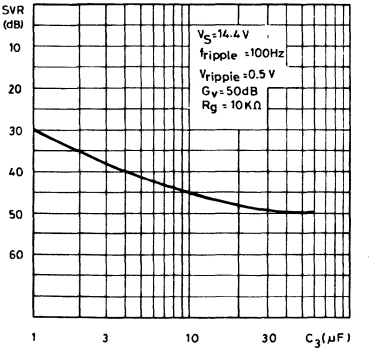


Figure 11 : Supply Voltage Rejection vs. Frequency.

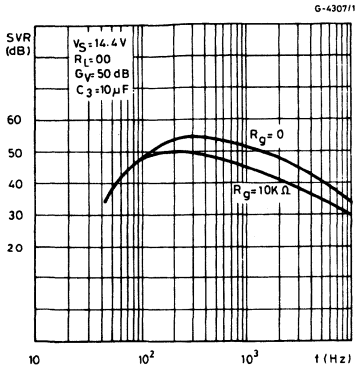


Figure 12 : Supply Voltage Rejection vs. Values of Capacitors C_2 and C_3.

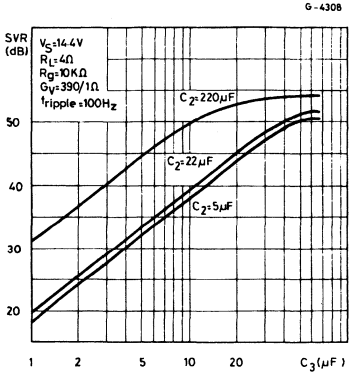


Figure 13 : Supply Voltage Rejection vs. Values of Capacitors C_2 and C_3.

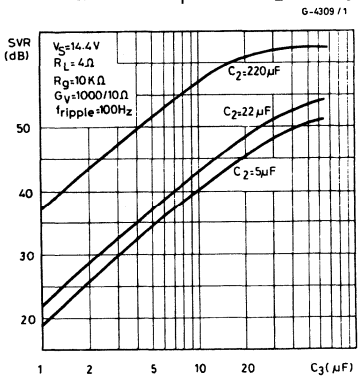


Figure 14 : Gain vs. Input Sensitivity.

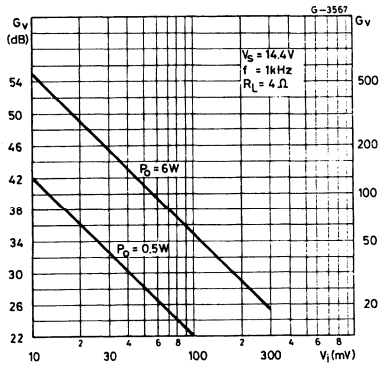


Figure 15 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

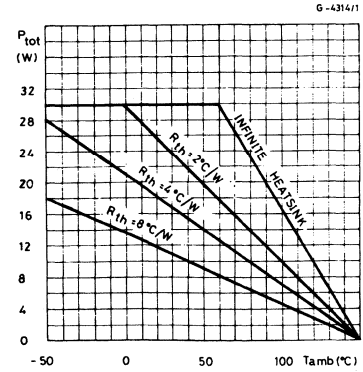


Figure 16 : Total Power Dissipation and Efficiency vs. Output Power.

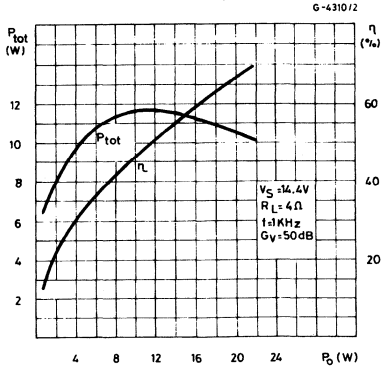
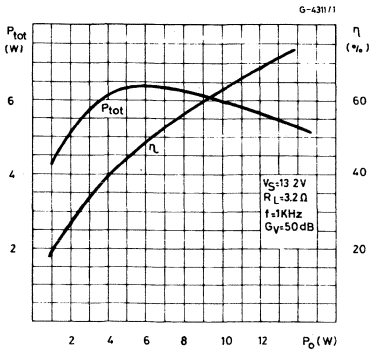


Figure 17 : Total Power Dissipation and Efficiency vs. Output Power .



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig.1. Different values can be used ; the following table can help the designer.

Component	Recommended Value	Purpose	Larger Than	Smaller Than
R_1	120 kΩ	Optimisation of the Output Signal Simmetry	Smaller $P_{o\ max}$	Smaller $P_{o\ max}$
R_2 and R_4	1 kΩ	Close Loop Gain Setting (*)	Increase of Gain	Decrease of Gain
R_3 and R_5	3.3 Ω		Decrease of Gain	Increase of Gain
R_6 and R_7	1 Ω	Frequency Stability	Danger of Oscillation at High Frequency with Inductive Load	
C_1 and C_2	2.2 µF	Input DC Decoupling	High Turn-on Delay	High Turn-on Pop Higher Low Frequency Cutoff. Increase of Noise
C_3	10 µF	Ripple Rejection	Increase of SVR Increase of the Switch-on Time	Degradation of SVR
C_4 and C_6	100 µF	Bootstrapping		Increase of Distortion at Low Frequency
C_5 and C_7	100 µF	Feedback Input DC Decoupling		
C_8 and C_9	0.1 µF	Frequency Stability		Danger of Oscillation
C_{10} and C_{11}	1000 µF to 2200 µF	Output DC Decoupling		Higher Low-frequency Cut-off

(*) The closed–loop gain must be higher than 26dB.

BUILT–IN PROTECTION SYSTEMS

LOAD DUMP VOLTAGE SURGE

The TDA2004 has a circuit which enables it to withstand a voltage pulse train, on pin 9, of the type shown in Fig. 19.

If the supply voltage peaks to more than 40 V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.

A suggested LC network is shown in Fig. 18. With this network, a train of pulse with amplitude up to 120 V and with of 2 ms can be applied to point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18 V. For this reason the maximum operating supply voltage is 18 V.

Figure 18.

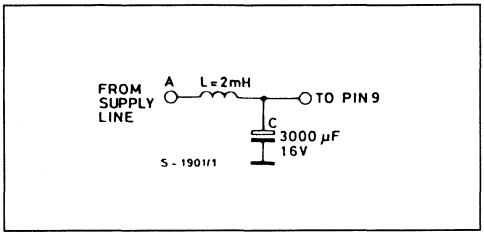
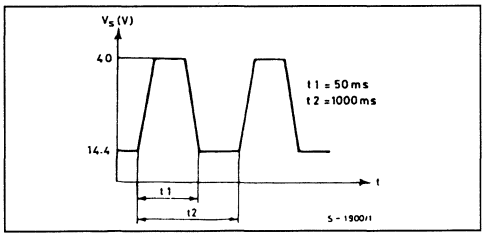


Figure 19.



SHORT CIRCUIT (AC conditions)

The TDA2004 can withstand an accidental short-circuit from the output to ground caused by a wrong connection during normal working.

POLARITY INVERSION

High current (up to 10 A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2 A fuse (normally connected in series with the supply). This feature is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

OPEN GROUND

When the ratio is the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA2004 protection diodes are included to avoid any damage.

INDUCTIVE LOAD

A protection diode is provided to allow use of the TDA2004 with inductive loads.

DC VOLTAGE

The maximum operating DC voltage on the TDA2004 is 18 V.

However the device can withstand a DC voltage up to 28 V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages :

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature ; all that happens is the P_O (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance) ; fig. 20 shown this dissipable power as a function of ambient temperature for different thermal resistance.

20W BRIDGE AMPLIFIER FOR CAR RADIO

High output power : P_O = 10 + 10 W@R_L = 2 Ω, d = 10 % ; P_O = 20 W@R_L = 4Ω , d = 10 %.

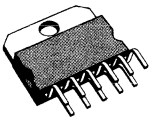
High reliability of the chip and package with additional complete safety during operation thanks to protection against :

- OUTPUT DC AND AC SHORT CIRCUIT TO GROUND
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE SURGE
- FORTUITOUS OPEN GROUND
- VERY INDUCTIVE LOADS

Flexibility in use : bridge or stereo booster amplifiers with or without boostrap and with programmable gain and bandwidth.

Space and cost saving : very low number of external components, very simple mounting system with no electrical isolation between the package and the heatsink (one screw only).

In addition, the circuit offers **loudspeaker protection** during short circuit for one wire to ground.



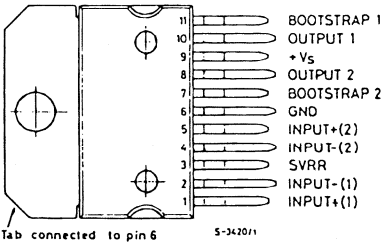
Multiwatt 11®

ORDER CODES : TDA2005M – Bridge Application
TDA2005S – Stereo Application

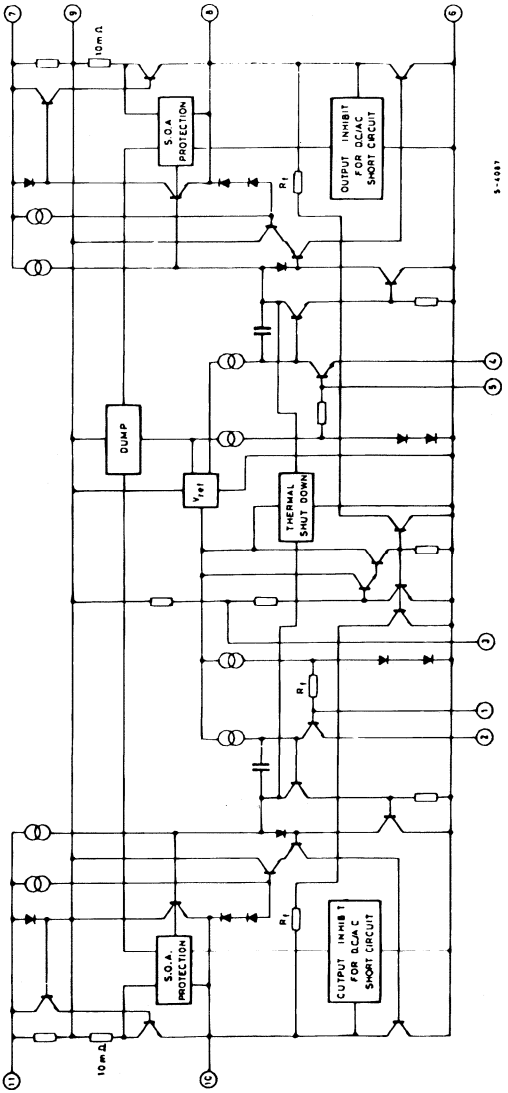
DESCRIPTION

The TDA2005 is class B dual audio power amplifier in MULTIWATT® package specifically designed for car radio application : **power booster amplifiers** are easily designed using this device that provides a high current capability (up to 3.5 A) and that can drive very low impedance loads (down to 1.6Ω in stereo applications) obtaining an output power of more than 20 W (bridge configuration).

PIN CONNECTION (top view)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

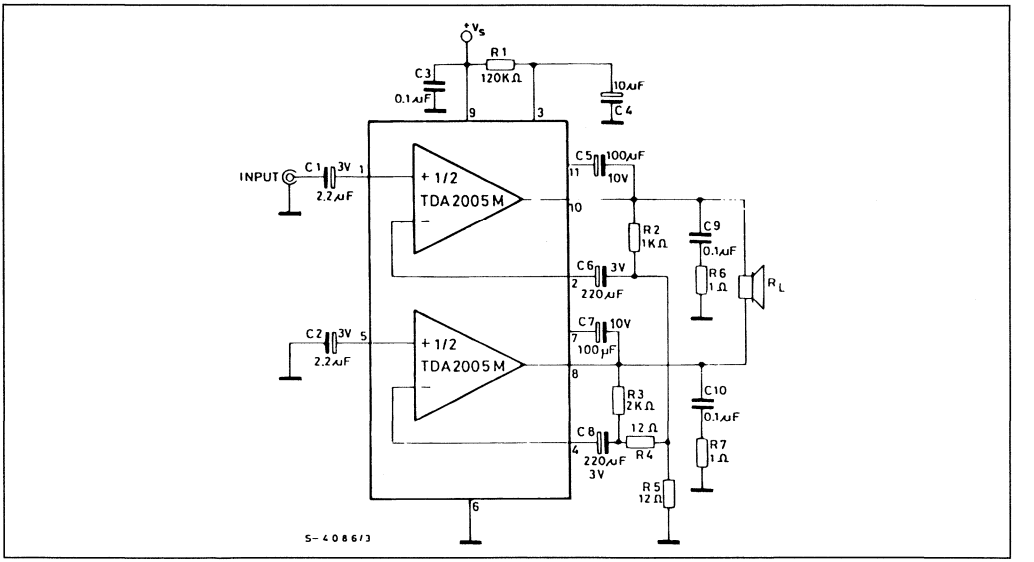
Symbol	Parameter	Value	Unit
V_s	Operating Supply Voltage	18	V
V_s	DC Supply Voltage	28	V
V_s	Peak Supply Voltage (for 50 ms)	40	V
I_o (*)	Output Peak Current (non repetitive t = 0.1 ms)	4.5	A
I_o (*)	Output Peak Current (repetitive f ≥ 10 Hz)	3.5	A
P_{tot}	Power Dissipation at T_{case} = 60 °C	30	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

BRIDGE AMPLIFIER APPLICATION (TDA2005M)

Figure 1 : Test and Application Circuit (bridge amplifier).



ELECTRICAL CHARACTERISTICS (refer to the **bridge** application circuit, T_{amb} = 25 °C, G_v = 50 dB, $R_{th\ (heatsink)}$ = 4 °C/W, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage			8		18	V
V_{os}	Output Offset Voltage (°) (between pin 8 and pin 10)	V_s = 14.4 V V_s = 13.2 V				150 150	mV mV
I_d	Total Quiescent Drain Current	V_s = 14.4 V	R_L = 4 Ω		75	150	mA
		V_s = 13.2 V	R_L = 3.2 Ω		70	160	mA
P_o	Output Power	d = 10 %	f = 1 kHz				
		V_s = 14.4 V	R_L = 4 Ω	18	20		W
			R_L = 3.2 Ω	20	22		W
		V_s = 13.2 V	R_L = 3.2 Ω	17	19		W
d	Distortion	f = 1 kHz V_s = 14.4V P_o = 50 mW to 15 W	R_L = 4 Ω			1	%
		V_s = 13.2 V P_o = 50 mW to 13 W	R_L = 3.2 Ω			1	%
V_i	Input Sensitivity	f = 1 kHz P_o = 2 W P_o = 2 W	R_L = 4 Ω R_L = 3.2 Ω		9 8		mV mV
R_i	Input Resistance	f = 1 kHz		70			kΩ
f_L	Low Frequency Roll Off (– 3 dB)	R_L = 3.2 Ω				40	Hz
f_H	High Frequency Roll Off (– 3 dB)	R_L = 3.2 Ω		20			kHz
G_v	Closed Loop Voltage Gain	f = 1 kHz			50		dB
e_N	Total Input Noise Voltage	R_g = 10 kΩ (°°)			3	10	μV
SVR	Supply Voltage Rejection	R_g = 10 kΩ f_{ripple} = 100 Hz V_{ripple} = 0.5 V	C_4 = 10 μF	45	55		dB
η	Efficiency	V_s = 14.4 V P_o = 20 W P_o = 22 W V_s = 13.2 V P_o = 19 W	f = 1 kHz R_L = 4 Ω R_L = 3.2 Ω f = 1 kHz R_L = 3.2 Ω		60 60 58		% % %
T_j	Thermal Shut-down Junction Temperature	V_s = 14.4 V f = 1 kHz	R_L = 4 Ω P_{tot} = 13 W		145		°C
V_{OSH}	Output Voltage with one Side of the Speaker shorted to ground	V_s = 14.4 V V_s = 13.2 V	R_L = 4 Ω R_L = 3.2 Ω			2	V

Note : (*) For TDA2005M only
(**) Bandwith Filter : 22Hz to 22KHz.

BRIDGE AMPLIFIER APPLICATION (continued)

Figure 2 : P.C. Board and Component layout (scale 1 : 1).

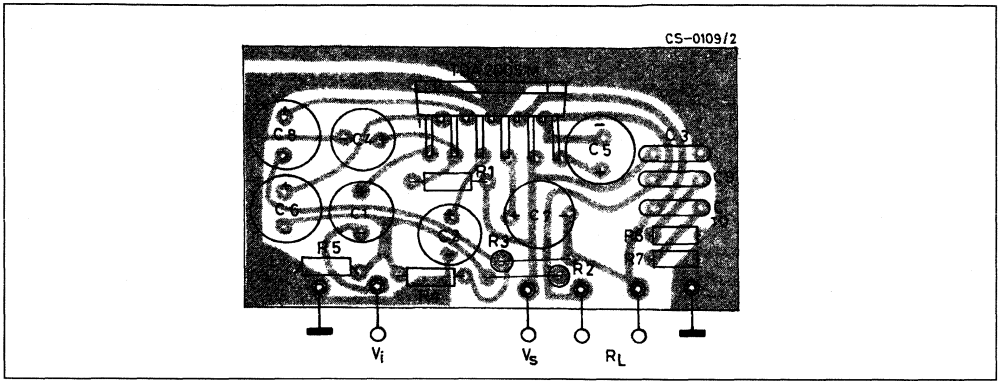


Figure 3 : Output Offset Voltage vs. Supply Voltage.

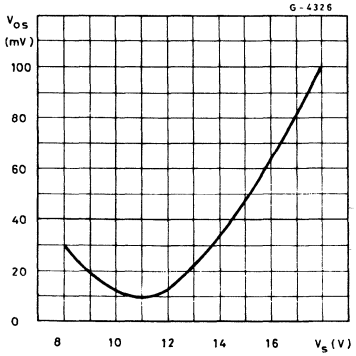


Figure 4 : Distortion vs. Output Power (bridge amplifier).

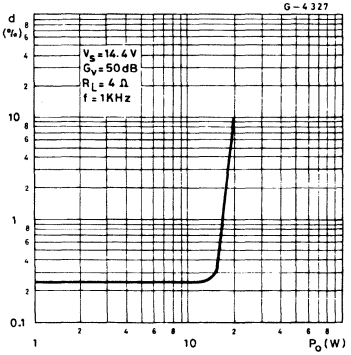
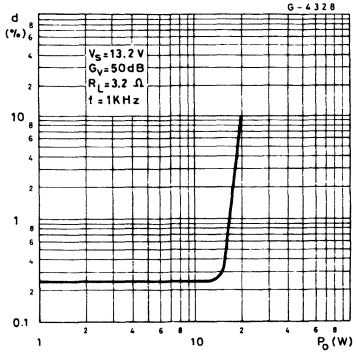


Figure 5 : Distortion vs. Output Power (bridge amplifier).



BRIDGE AMPLIFIER DESIGN

The following consideraions can be useful when designing a bridge amplifier.

Parameter		Single Ended	Bridge
$V_{o\ max}$	Peak Output Voltage (before clipping)	$\frac{1}{2}(V_s - 2\ V_{CE\ sat})$	$V_s - 2\ V_{CE\ sat}$
$I_{o\ max}$	Peak Output Current (before clippling)	$\frac{1}{2}\frac{(V_s - 2\ V_{CE\ sat})}{R_L}$	$\frac{V_s - 2\ V_{CE\ sat}}{R_L}$
$P_{o\ max}$	rms Output Power (before clipping)	$\frac{1}{4}\frac{(V_s - 2\ V_{CE\ sat})^2}{2\ R_L}$	$\frac{(V_s - 2\ V_{CE\ sat})^2}{2\ R_L}$

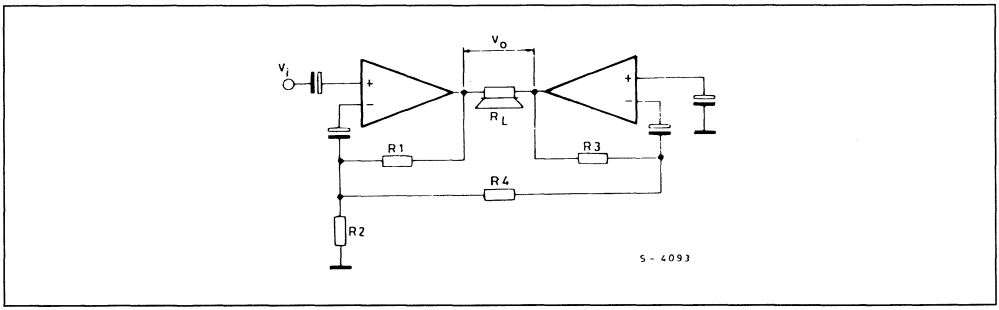
Where : $V_{CE\ sat}$ = output transistors saturation voltage
V_S = allowable supply voltage
R_L = load impedance.

Voltage and current swings are twice for a bridge amplifier in comparison with single ended amplifier. In order words, with the same R_L the bridge configuration can deliver an output power that is four times the output power of a single ended amplifier, while, with the same max output current the bridge configuration can deliver an output power that is twice the output power of a single ended amplifier. Core must be taken when selecting V_S and R_L in order to avoid an output peak current above the absolute maximum rating.

From the expression for $I_{O\ max}$, assuming V_S = 14.4 V and $V_{CE\ sat}$ = 2 V, the minimum load that can be driven by TDA2005 in bridge configuration is :

$$R_{Lmin} = \frac{V_S - 2\ V_{CEsat}}{I_{O\ max}} = \frac{14.4 - 4}{3.5} = 2.97\Omega$$

Figure 6 : Bridge Configuration.



The voltage gain of the bridge configuration is given by (see fig. 6) :

$$G_V = \frac{V_O}{V_I} = 1 + \frac{R_1}{\frac{R2\ .\ R_4}{R_2 + R4}} + \frac{R_3}{R_4}$$

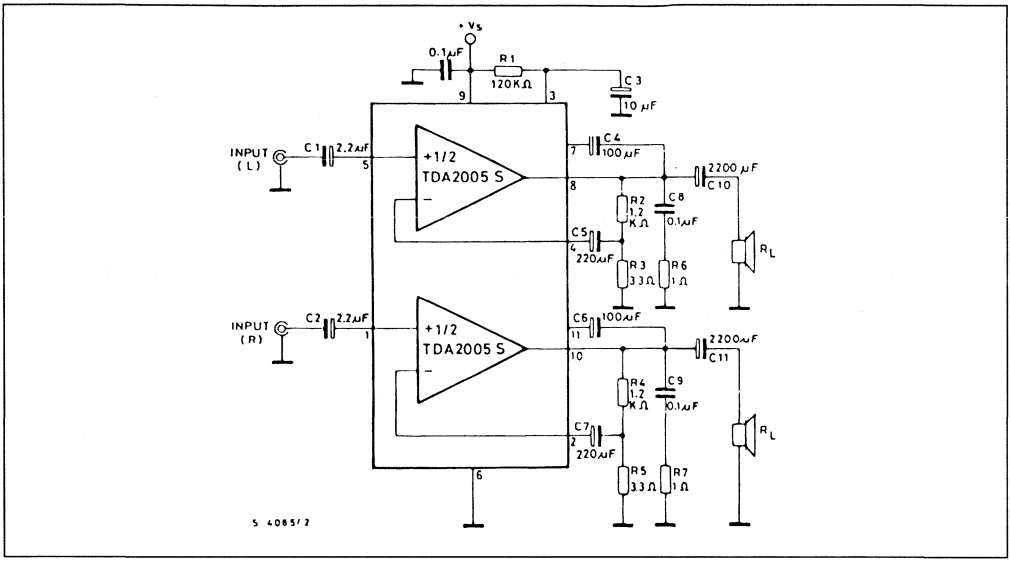
For sufficiently high gains (40 to 50 dB) it is possible to put $R_2 = R_4$ and $R_3 = 2\ R_1$, simplifing the formula in :

$$G_V = 4\ \frac{R_1}{R_2}$$

G_V (dB)	R_1 (Ω)	$R_2 = R_4$ (Ω)	R_3 (Ω)
40	1000	39	2000
50	1000	12	2000

STEREO AMPLIFIER APPLICATION (TDA2005S)

Figure 7 : Typical Application Circuit.



ELECTRICAL CHARACTERISTICS (refer to the **stereo** application circuit, T_{amb} = 25 °C, G_v = 50 dB, $R_{th\ (heatsink)}$ = 4 °C/W, unless otherwwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage			8		18	V
V_o	Quiescent Output Voltage	V_s = 14.4 V V_s = 13.2 V		6.6 6	7.2 6.6	7.8 7.2	V V
I_d	Total Quiescent Drain Current	V_s = 14.4 V V_s = 13.2 V			65 62	120 120	mA mA
P_o	Output Power (each channel)	f = 1 kHz V_s = 14.4 V	d = 10 % R_L = 4 Ω	6	6.5		W
			R_L = 3.2 Ω	7	8		W
			R_L = 2 Ω	9	10		W
			R_L = 1.6 Ω	10	11		W
		V_s = 13.2 V	R_L = 3.2 Ω	6	6.5		W
			R_L = 1.6 Ω	9	10		W
		V_s = 16 V	R_L = 2 Ω		12		W
d	Distortion (each channel)	f = 1 kHz V_s = 14.4 V P_o = 50 mW to 4 W	R_L = 4 Ω		0.2	1	%
		V_s = 14.4 V P_o = 50 mW to 6 W	R_L = 2 Ω		0.3	1	%
		V_s = 13.2 V P_o = 50 mW to 3 W	R_L = 3.2 Ω		0.2	1	%
		V_s = 13.2 V P_o = 40 mW to 6 W	R_L = 1.6 Ω		0.3	1	%

(*) For TDA2005S only.
(**) Bandwidth Filter : 22Hz to 22KHz.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
CT	Cross Talk (°)	V_s = 14.4 V R_L = 4 Ω V_o = 4 V_{rms} R_g = 5 kΩ	f = 1 kHz		60		dB
			f = 10 kHz		45		dB
V_i	Input Saturation Voltage			300			mV
V_i	Input Sensitivity	f = 1 kHz	P_o = 1 W R_L = 4 Ω R_L = 3.2 Ω		 6 5.5		mV
R_i	Input Resistance	f = 1 kHz		70	200		KΩ
f_L	Low Frequency Roll Off (– 3 dB)	R_L = 2 Ω				50	Hz
f_H	High Frequency Roll Off (– 3 dB)	R_L = 2 Ω		15			kHz
G_v	Voltage Gain (open loop)	f = 1 kHz			90		dB
G_v	Voltage Gain (closed loop)	f = 1 kHz		48	50	51	dB
ΔG_v	Closed Loop Gain Matching				0.5		dB
e_N	Total Input Noise Voltage	R_g = 10 kΩ (°°)			1.5	5	μV
SVR	Supply Voltage Rejection	R_g = 10 kΩ C_3 = 10 μF	f_{ripple} = 100 Hz V_{ripple} = 0.5 V	35	45		dB
η	Efficiency	V_s = 14.4 V R_L = 4 Ω R_L = 2 Ω V_s = 13.2 V R_L = 3.2 Ω R_L = 1.6 Ω	f = 1 kHz P_o = 6.5 W P_o = 10 W f = 1 kHz P_o = 6.5 W P_o = 100 W		 70 60 70 60		 % % % %
T_j	Thermal Shut-down Junction Temperature				145		°C

(°) For TDA2005S only.
(°°) Bandwidth Filter : 22Hz to 22KHz.

Figure 8 : Quiescent Output Voltage vs. Supply Voltage.

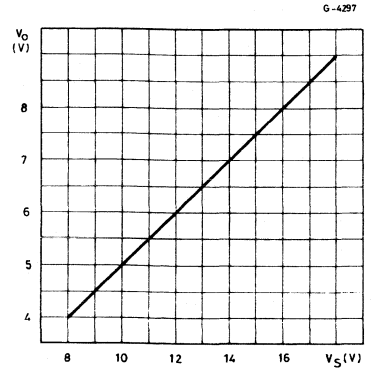


Figure 9 : Quiescent Drain Current vs. Supply Voltage.

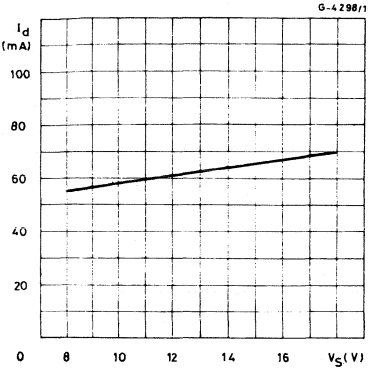


Figure 10 : Distortion vs. Output Power.

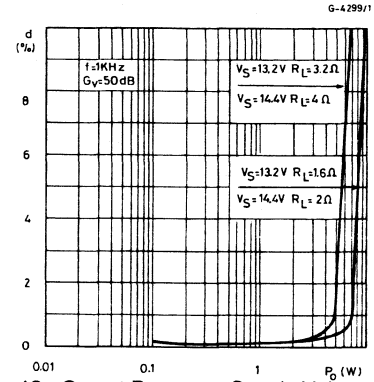


Figure 11 : Output Power vs. Supply Voltage.

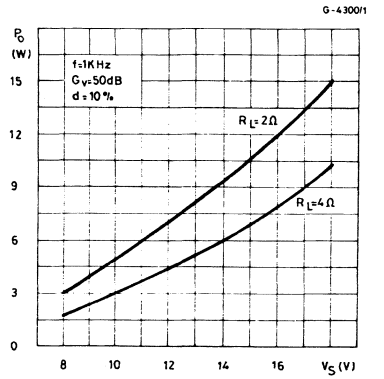


Figure 12 : Output Power vs. Supply Voltage.

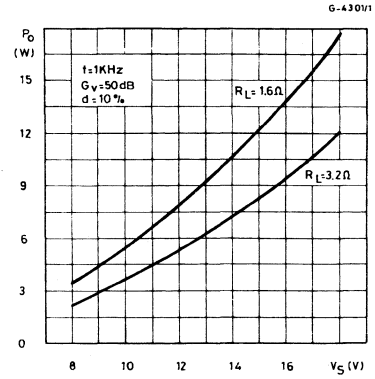


Figure 13 : Distortion vs. Frequency.

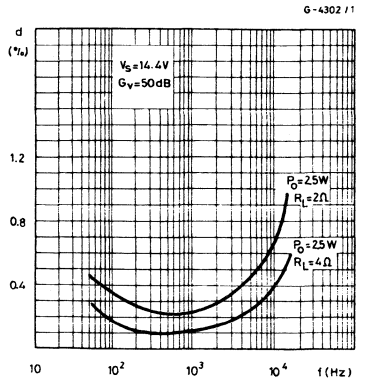


Figure 14 : Distortion vs. Frequency.

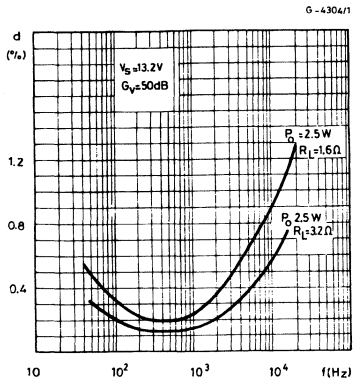


Figure 15 : Supply Voltage Rejection vs. C3.

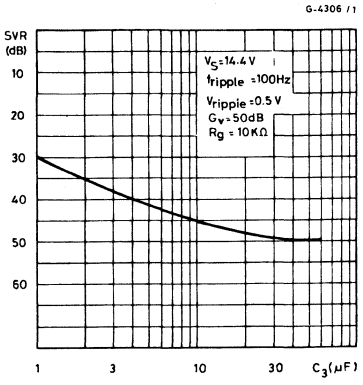


Figure 16 : Supply Voltage Rejection vs. Frequency.

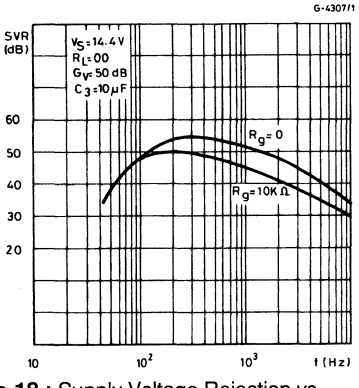


Figure 17 : Supply Voltage Rejection vs. Values of Capacitors C_2 and C_3.

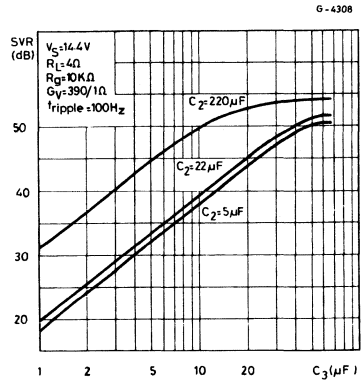


Figure 18 : Supply Voltage Rejection vs. Values of Capacitors C_2 and C_3.

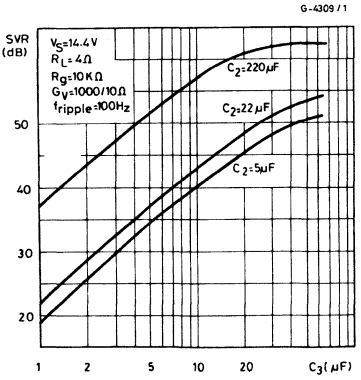


Figure 19 : Gain vs. Input Sensitivity.

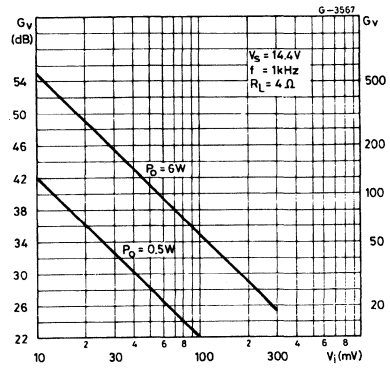


Figure 20 : Gain vs. Input Sensitivity.

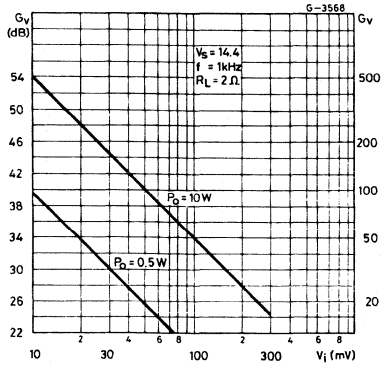


Figure 21 : Total Power Dissipation and Efficiency vs. Output Power (bridge).

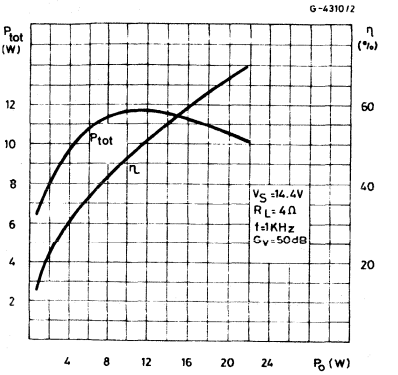
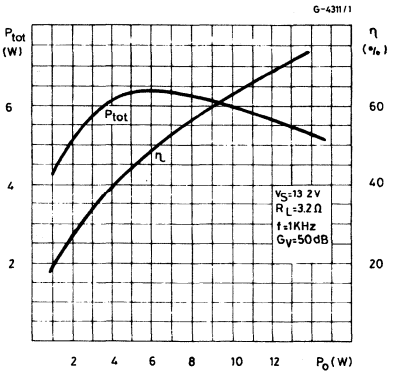


Figure 22 : Total Power Dissipation and Efficiency vs. Output Power .



APPLICATION SUGGESTION

The recommended values of the components are those shown on Bridge applicatiion circuit of fig.1. Different values can be used ; the following table can help the designer.

Component	Recommanded Value	Purpose	Larger Than	Smaller Than
R_1	120 kΩ	Optimization of the Output Symmetry	Smaller $P_{o\ max}$	Smaller $P_{o\ max}$
R_2	1kΩ	Closed Loop Gain Setting (see BRIDGE AMPLIFIER DESIGN) (*)		
R_3	2 kΩ			
R_4 and R_5	12 Ω			
R_6 and R_7	1 Ω	Frequency Stability	Danger of Oscillation at High Frequency with Inductive Loads	
C_1	2.2 µF	Input DC Decoupling	High Turn on Delay	Higher Turn on Pop Higher Low Frequency Cutoff Increase of Noise
C_2	2.2 µF	Optimization of Turn on Pop and Turn on Delay		
C_3	0.1 µF	Supply by Pass		Danger of Oscillation
C_4	10 µF	Ripple Rejection	Increase of SVR Increase of the Switch-on Time	Degradation of SVR.
C_5 and C_7	100 µF	Bootstrapping		Increase of Distortion at low Frequency
C_6 and C_8	220 µF	Feedback Input DC Decoupling, Low Frequency Cutoff		Higher Low Frequency Cutoff
C_9 and C_{10}	0.1 µF	Frequency Stability		Danger of Oscillation

(*) The closed loop gain must be higher than 32 dB.

APPLICATION INFORMATION

Figure 23 : Bridge Amplifier without Boostrap.

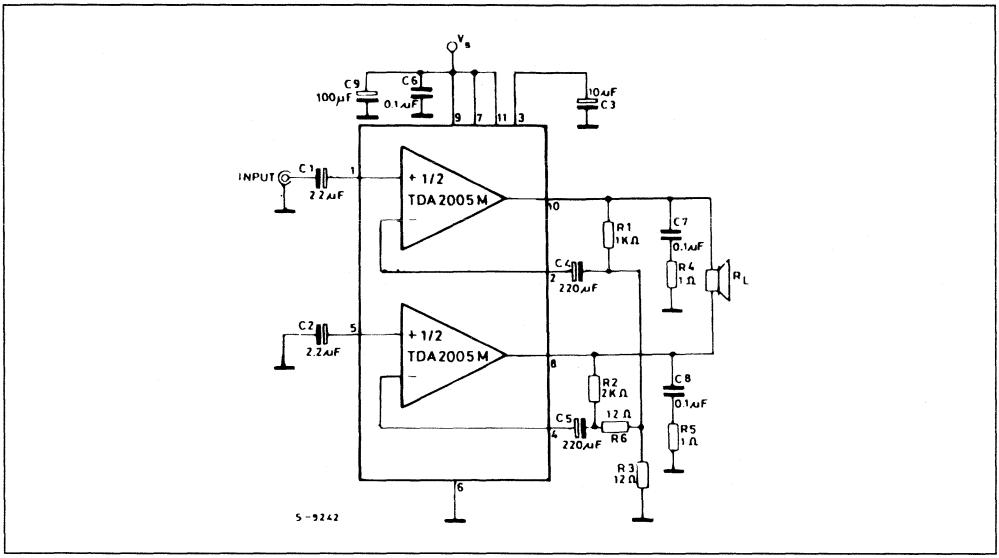


Figure 24 : P.C. Board and Components layout of the Circuit of Fig.23 (1 : 1 scale).

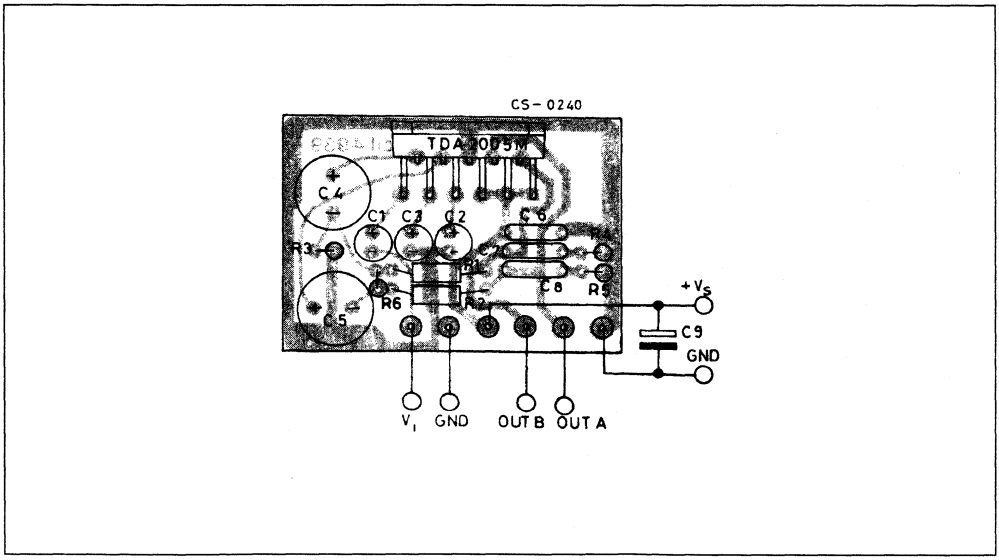


Figure 25 : Dual – Bridge Amplifier.

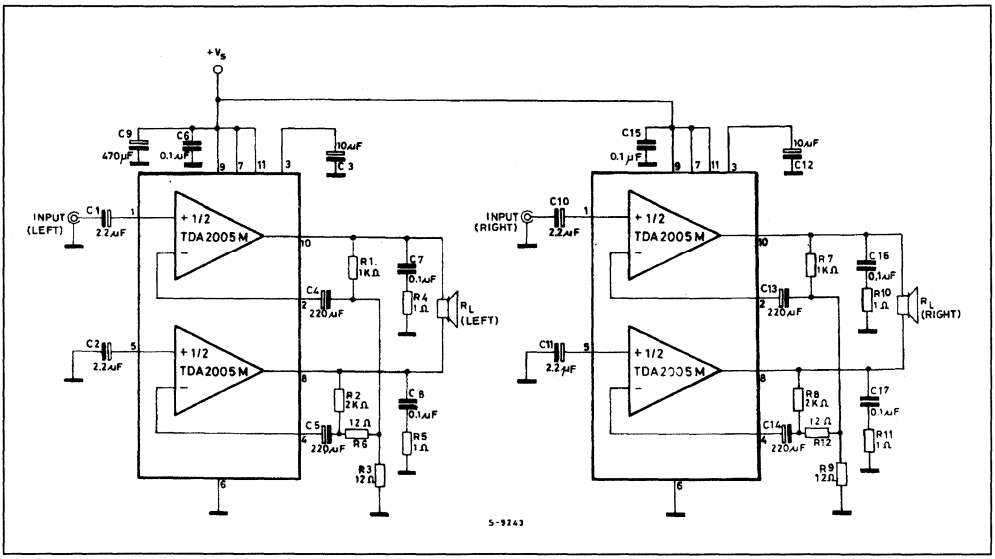


Figure 26 : P.C. Board and Components layout of the Circuit of Fig.25 (1 : 1 scale).

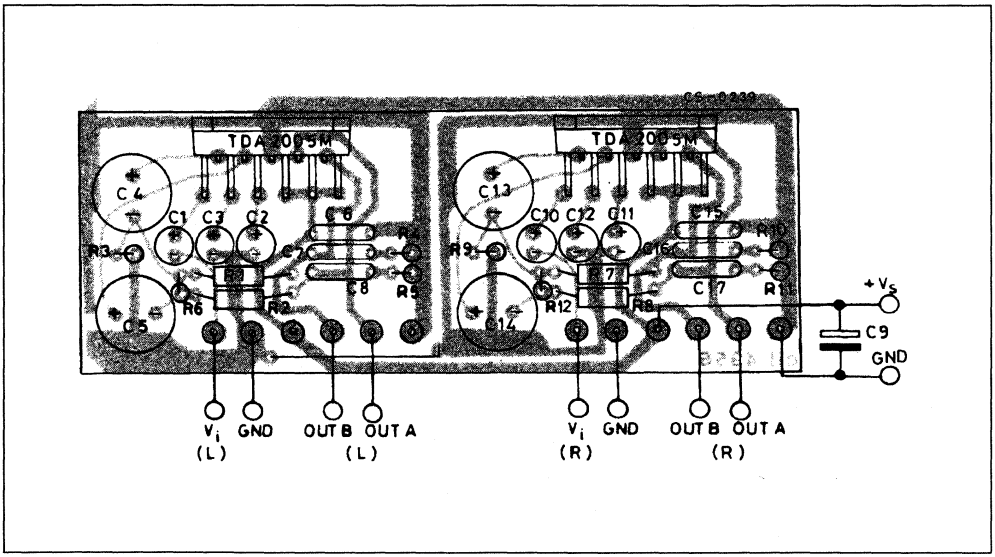


Figure 27 : Low Cost Bridge Amplifier (GV = 42dB).

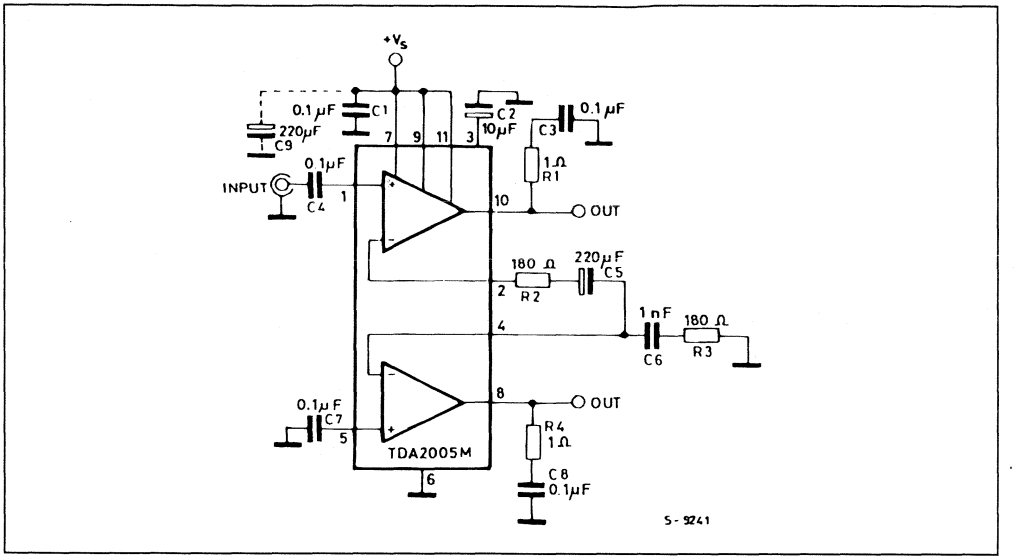


Figure 28 : P.C. Board and Components layout of the Circuit of Fig.27 (1 : 1 scale).

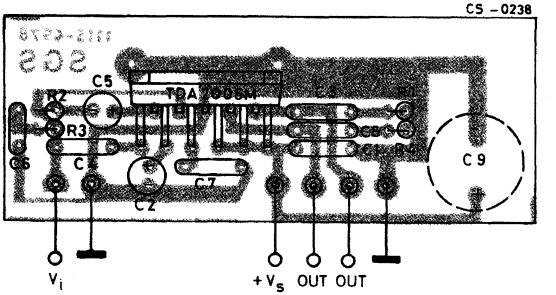


Figure 29 : 10 + 10W Stereo Amplifier with Tone Balance and Loudness Control.

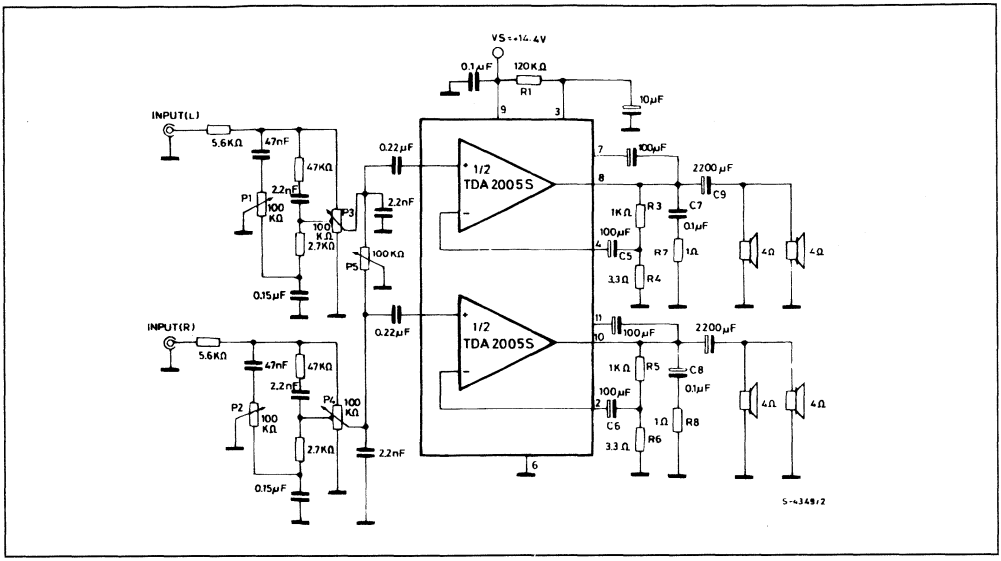


Figure 30 : Tone Control Response (circuit of Fig. 29).

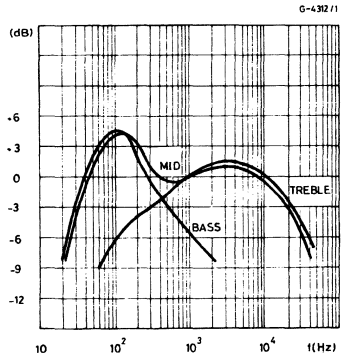


Figure 31 : 20W Bus Amplifier.

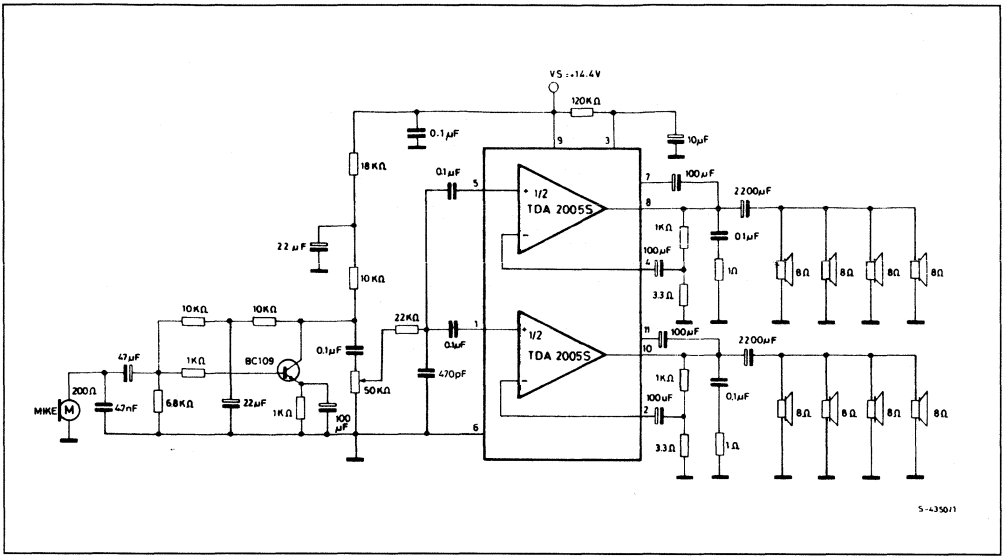


Figure 32 : Simple 20W Two Way Amplifier (Fc = 2KHz).

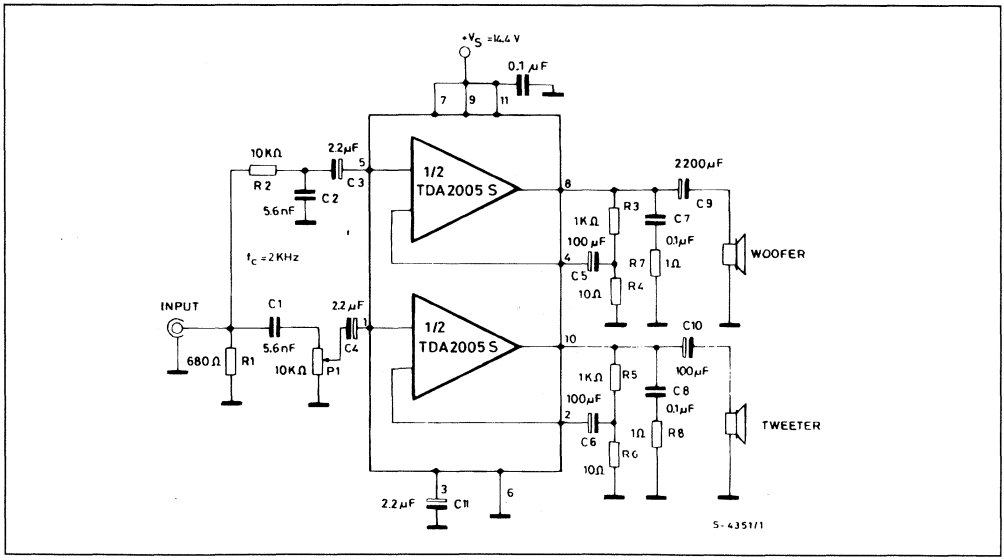


Figure 33 : Bridge Amplifier Circuit suited for Low–gain Applications (Gv = 34dB).

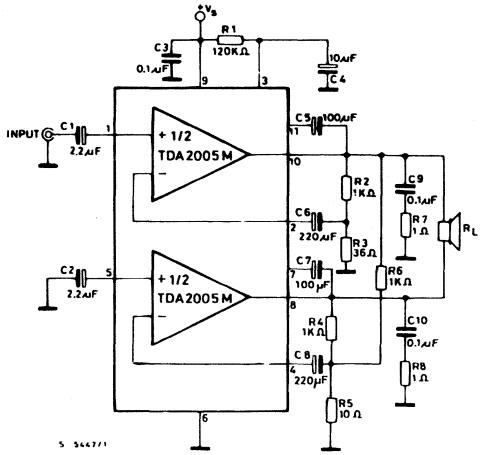
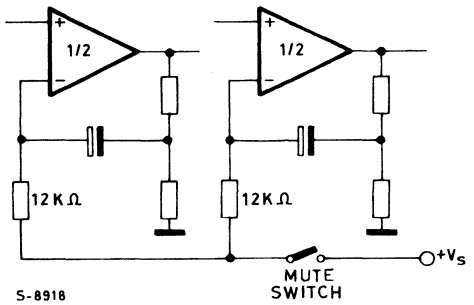


Figure 34 : Example of Muting Circuit.



BUILT–IN PROTECTION SYSTEMS

LOAD DUMP VOLTAGE SURGE

The TDA2005 has a circuit which enables it to withstand a voltage pulse train, on pin 9, of the type shown in Fig. 36.

If the supply voltage peaks to more than 40 V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held withing the limits shown.

A suggested LC network is shown in Fig. 35. With this network, a train of pulses with amplitude up to 120 V and width of 2 ms can be applied at point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18 V. For this reason the maximum operating supply voltage is 18 V.

Figure 35.

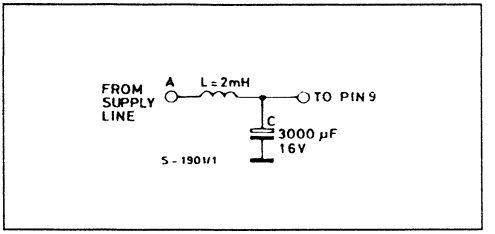
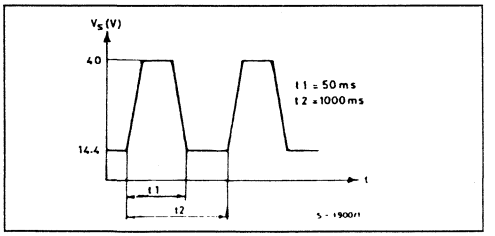


Figure 36.



SHORT CIRCUIT (AC and DC conditions)

The TDA2005 can withstand a permanent short-circuit on the output for a supply voltage up to 16 V.

POLARITY INVERSION

High current (up to 10 A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2 A fuse (normally connected in series with the supply). This feature is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

OPEN GROUND

When the ratio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA2005 protection diodes are included to avoid any damage.

INDUCTIVE LOAD

A protection diode is provided to allow use of the TDA2005 with inductive loads.

DC VOLTAGE

The maximum operating DC voltage for the TDA2005 is 18 V.

However the device can withstand a DC voltage up to 28 V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages :

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature : all that happens is that P_O (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance) ; fig. 37 shows the dissipable power as a function of ambient temperature for different thermal resistance.

LOUDSPEAKER PROTECTION

The circuit offers loudspeaker protection during short circuit for one wire to ground.

Figure 37 : Maximum allowable Power Dissipation vs. Ambient Temperature.

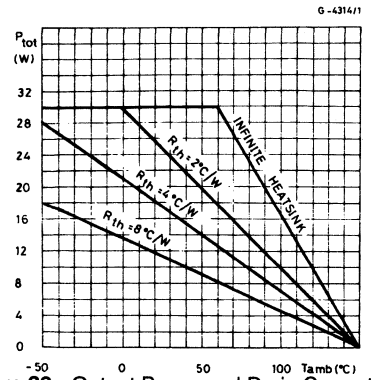


Figure 38 : Output Power and Drain Current vs. Case Temperature.

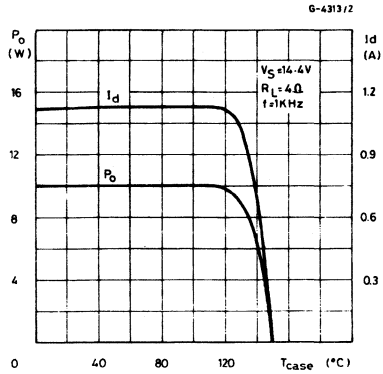
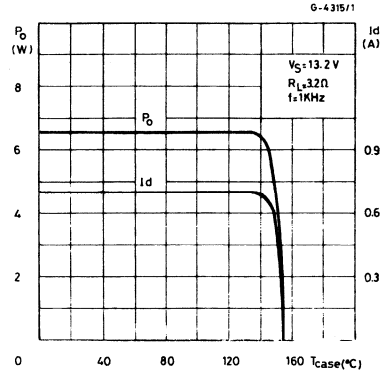


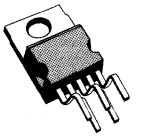
Figure 39 : Output Power and Drain Current vs. Case Temperature.



20W BRIDGE AMPLIFIER FOR CAR RADIO

PRELIMINARY DATA

- COMPACT HEPTAWATT PACKAGE
- FEW EXTERNAL COMPONENTS
- OUTPUT PROTECTED AGAINST SHORT CIRCUITS TO GROUND AND ACROSS LOAD
- DUMP TRANSIENT
- THERMAL SHUTDOWN
- LOUDSPEAKER PROTECTION
- HIGH CURRENT CAPABILITY
- LOW DISTORTION/LOW NOISE



Heptawatt

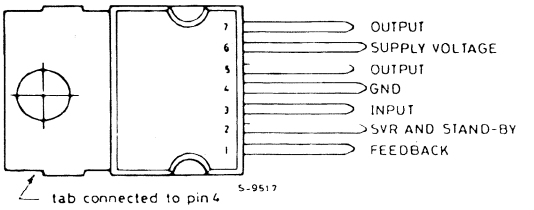
ORDER CODES : TDA7240AH
TDA7240AV

DESCRIPTION

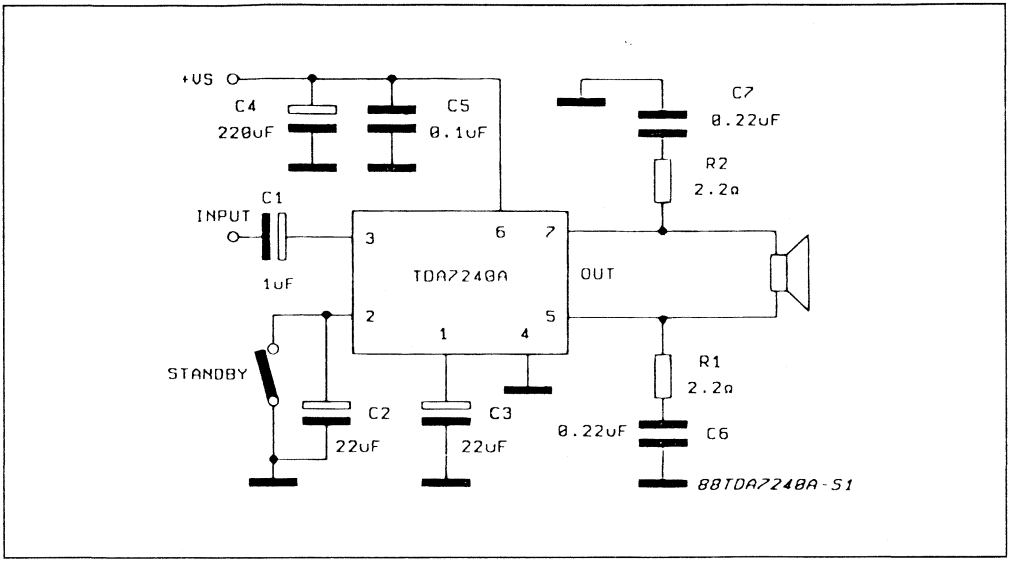
The TDA7240A is a 20W bridge audio amplifier IC designed specially for car radio applications. Thanks to the low external part count and compact Heptawatt 7-pin power package the TDA7240A occupies little space on the printed circuit board.

Reliable operation is guaranteed by a comprehensive array of on-chip protection features. These include protection against AC and DC output short circuits (to ground and across the load), load dump transients, and junction overtemperature. Additionally, the TDA7240A protects the loudspeaker when one output is short-circuited to ground.

PIN CONNECTION (top view)



TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Operating Supply Voltage	18	V
V_s	DC Supply Voltage	28	V
V_s	Peak Supply Voltage (for 50ms)	40	V
I_o (*)	Peak Output Current (non repetitive t = 0.1ms)	4.5	A
I_o (*)	Peak Output Current (repetitive f ≥ 10Hz)	3.5	A
P_{tot}	Power Dissipation at T_{case} = 70°C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

(*) Internally limited

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W

ELECTRICAL CHARACTERISTICS (refer to the circuit of fig. 1, T_{amb} = 25 °C, R_{th} (heatsink) = 4 °C/W, V_s = 14.4 V)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage					18	V
V_{os}	Output Offset Voltage					150	mV
I_d	Total Quiescent Current	R_L = 4Ω			65	120	mA
P_o	Output Power	f = 1KHz d = 10%	R_L = 4Ω	18	20		W
			R_L = 8Ω	10	12		
d	Distortion	R_L = 4Ω f = 1KHz P_o = 50mW to 12W			0.1	0.5	%
		R_L = 8Ω f = 1KHz P_o = 50 mW to 6W			0.05	0.5	
G_v	Voltage Gain	f = 1KHz		39.5	40	40.5	dB
SVR	Supply Voltage Rejection	f = 100Hz	R_g = 10KΩ	35	40		dB
E_N	Total Input Noise	(*)	R_s = 10KΩ		2	4	μV
		(**)			3		
η	Efficiency	R_L = 4Ω f = 1KHz P_o = 20W			65		%
I_{sb}	Stand-by Current				200		μA
R_i	Input Resistance	f = 1KHz		70			KΩ
V_i	Input Sensitivity	f = 1KHz P_o = 2W	R_L = 4Ω		28		mV
f_L	Low Frequency Roll Off (– 3dB)	P_o = 15W	R_L = 4Ω			30	Hz
f_H	High Frequency Roll Off (– 3dB)	P_o = 15W	R_L = 4Ω	25			KHz
A_s	Stand-by Attenuation	V_o = 2V_{rms}		70	90		dB
$V_{TH\ (pin\ 2)}$	Stand-by Threshold					1	V

Bandwidth (*) B= Curve A (**) B = 22Hz to 22 KHz

Figure 1 : Test and Application Circuit.

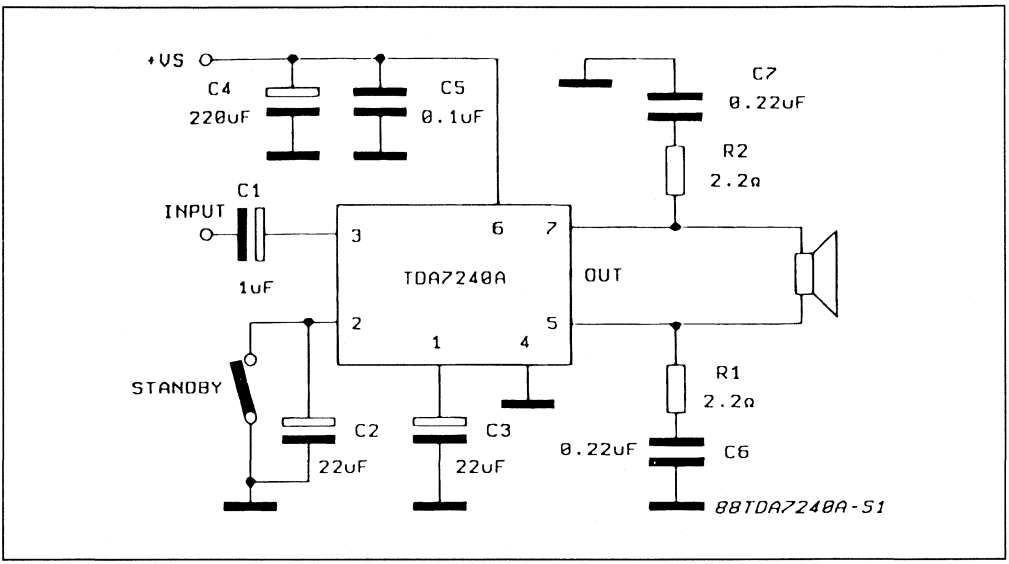
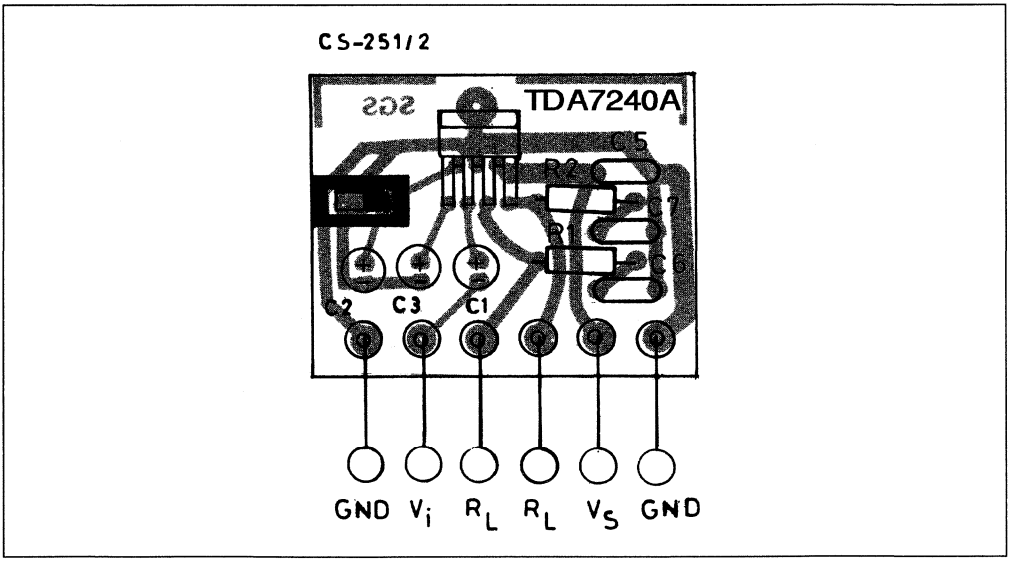


Figure 2 : P.C. Board and Components layout of the Circuit of Fig. 1.



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of Fig. 1. Different values can be used, the following table can help the designer.

Component	Recommanded Value	Purpose	Larger Than	Smaller Than
R1, R2	2.2Ω	Frequency Stability	Danger of High Frequency Oscillation	
C1	1µF	Input DC Decoupling	Higher Turn 'ON' and Stand-by Delay	Higher Turn 'ON' Pop. Higher Low Frequency Cutoff
C2	22µF	Ripple Rejection	Increase of SVR Increase of the Turn 'ON' Delay	Degradation of SVR
C3	22µF	Feedback Low Frequency Cutoff		Higher Low Frequency Cutoff
C6, C7	0.22µF	Frequency Stability		Danger of Oscillation
C4	220µF	Supply Filter		Danger of Oscillation
C5	0.1µF	Supply by Pass		Danger of Oscillation

Figure 3 : Output Power vs. Supply Voltage.

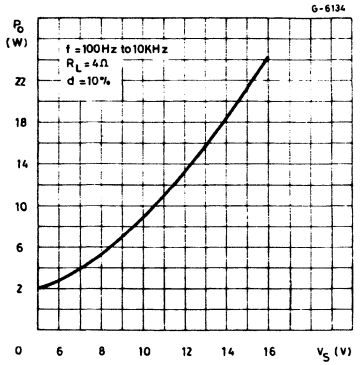


Figure 4 : Distortion vs. Output Power.

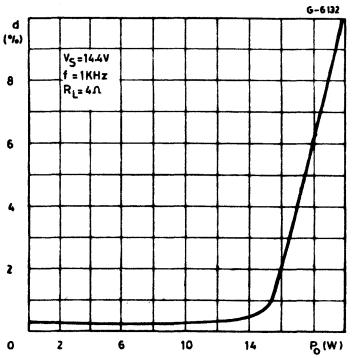


Figure 5 : Output Power vs. Supply voltage.

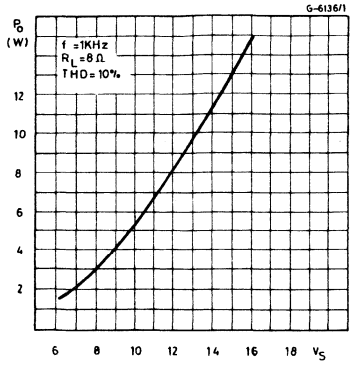


Figure 6 : Distortion vs. Output Power.

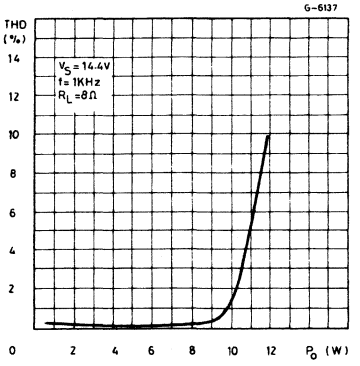


Figure 7 : Distortion vs. Frequency.

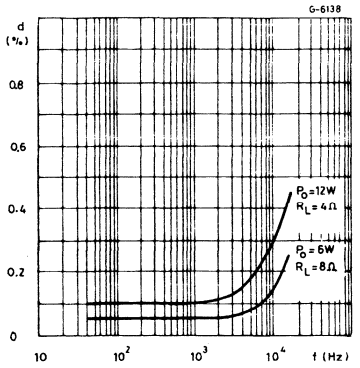


Figure 8 : Supply Voltage Rejection vs. Frequency.

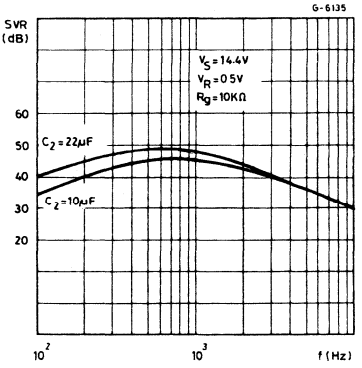


Figure 9 : Output Offset Voltage vs. Supply voltage.

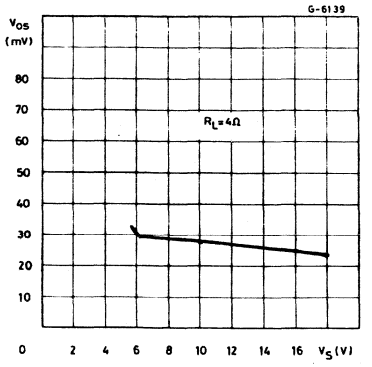


Figure 10 : Power Dissipation and Efficiency vs. Output Power.

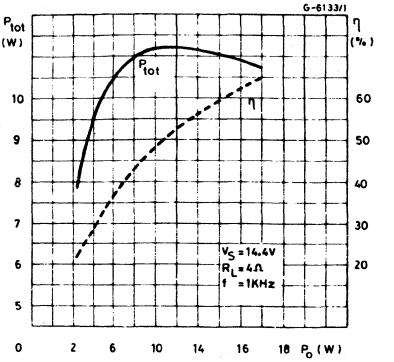
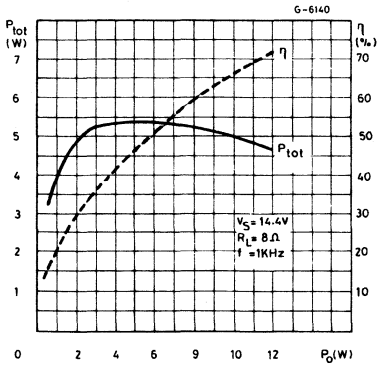


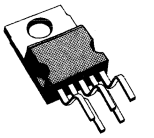
Figure 11 : Power Dissipation and Efficiency vs. Output Power.



20W BRIDGE AMPLIFIER FOR CAR RADIO

ADVANCE DATA

- VERY LOW STAND-BY CURRENT
- GAIN = 26 dB
- OUTPUT PROTECTED AGAINST SHORT CIRCUITS TO GROUND AND ACROSS LOAD
- COMPACT HEPTAWATT PACKAGE
- DUMP TRANSIENT
- THERMAL SHUTDOWN
- LOUDSPEAKER PROTECTION
- HIGH CURRENT CAPABILITY
- LOW DISTORTION/LOW NOISE



Heptawatt

ORDER CODE : TDA7241V
TDA7241H

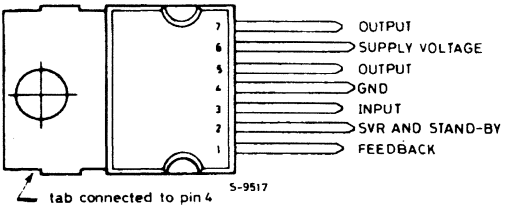
DESCRIPTION

The TDA7241 is a 20W bridge audio amplifier IC designed specially for car radio applications. Thanks to the low external part count and compact Heptawatt 7-pin power package the TDA7241 occupies little space on the printed circuit board.

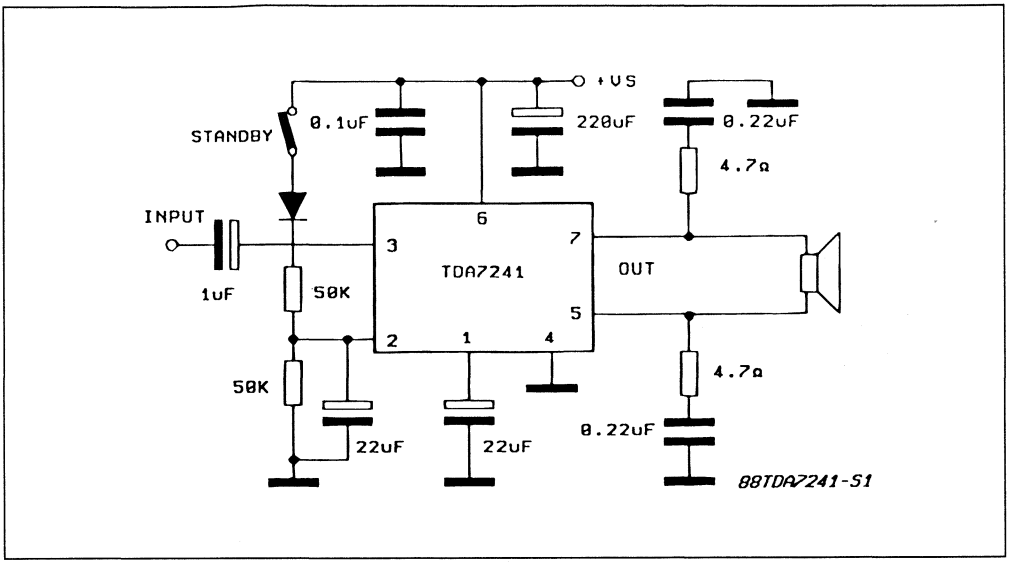
Reliable operation is guaranteed by a comprehensive array of on-chip protection features.

These include protection against AC and DC output short circuits (to ground and across the load), load dump transients, and junction overtemperature. Additionally, the TDA7241 protects the loudspeaker when one output is short-circuited to ground.

PIN CONNECTIONS (top view)



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Operating Supply Voltage	18	V
V_s	DC Supply Voltage	28	V
V_s	Peak Supply Voltage (for 50 ms)	40	V
I_o (*)	Peak Output Current (non repetitive t = 0.1 ms)	4.5	A
I_o (*)	Peak Output Current (repetitive f ≥ 10 Hz)	3.5	A
P_{tot}	Power Dissipation at T_{case} = 70 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

(*) Internally limited

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W

ELECTRICAL CHARACTERISTICS (refer to the circuit of fig. 1, T_{amb} = 25 °C, R_{th}(heatsink) = 4 °C/W, V_s = 14.4 V)

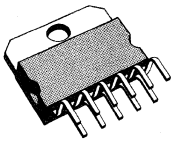
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage					18	V
V_{os}	Output Offset Voltage					150	mV
I_d	Total Quiescent Current	R_L = 4 Ω			65	120	mA
P_o	Output Power	f = 1 KHz d = 10 %	R_L = 4 Ω	18	20		W
			R_L = 8 Ω	10	12		
d	Distortion	R_L = 4 Ω P_o = 50 mW to 12 W	f = 1 KHz		0.1	0.5	%
		R_L = 8 Ω P_o = 50 mW to 6 W	f = 1 KHz		0.05	0.5	
G_v	Voltage Gain	f = 1 KHz			26		dB
SVR	Supply Voltage Rejection	f = 100 KHz		45	52		dB
E_n	Total Input Noise	(*)	R_s = 10 KΩ		2	4	μV
		(**)			3		
η	Efficiency	R_L = 4 Ω P_o = 20 W	f = 1 KHz		65		%
I_{sb}	Stand-by-current				1		μA
R_i.	Input Resistance	f = 1 kHz		70			KΩ
V_i	Input Sensitivity	f = 1 kHz P_o = 2 W	R_L = 4 Ω		140		mV
f_L	Low Frequency Roll Off (– 3 dB)	P_o = 15 W	R_L = 4 Ω			30	Hz
f_H	High Frequency Roll Off (– 3 dB)	P_o = 15 W	R_L = 4 Ω	25			KHz
A_s	Stand-by Attenuation	V_o = 2 V_{rms}		70	90		dB
V_{TH} (pin. 2)	Stand-by Threshold					1	V

Bandwidth (*) B = Curve A (**) B = 22 Hz to 22 KHz

22W BRIDGE FULLY PROTECTED CAR RADIO AMPLIFIER

ADVANCE DATA

- NO AUDIBLE POP DURING MUTE AND STANDBY OPERATIONS
- MUTING TTL COMPATIBLE
- VERY LOW CONSUMPTION STANDBY
- PROGRAMMABLE TURN ON DELAY
- DIFFERENTIAL INPUT
- SHORT CIRCUIT PROTECTIONS :
  RL SHORT – OUT TO GROUND – OUT TO VS
- OTHER PROTECTIONS :
  - Load Dump Voltage Surge
  - Loudspeaker DC Current
  - Very Inductive Load
  - Overrating Temperature
  - Open Ground



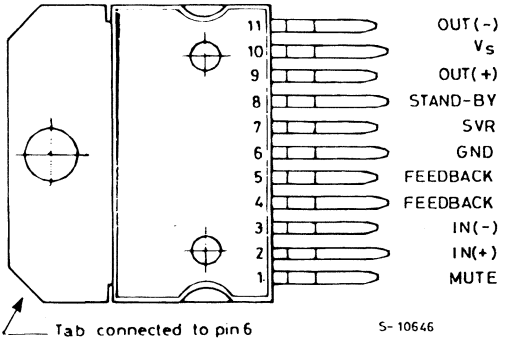
Multiwatt–11

ORDER CODE : TDA7256

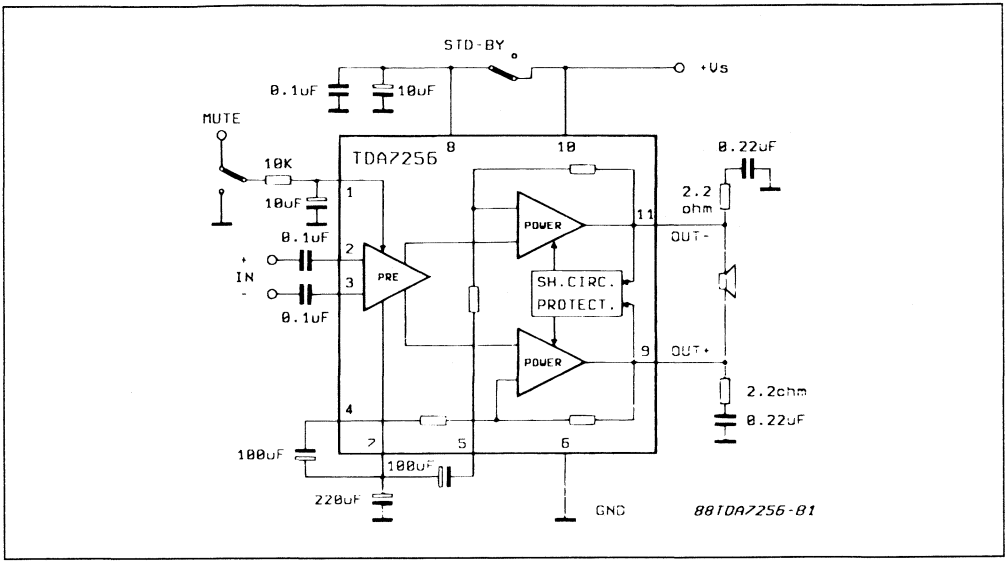
DESCRIPTION

The TDA7256 is a class B dual fully protected bridge power amplifier, designed for car radio applications. A high current capability allows to drive low impedance loads (up to 2Ω)

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Operating Supply Voltage	18	V
V_s	DC Supply Voltage	28	V
V_s	Peak Supply Voltage (for 50 ms)	40	V
I_O	Output Peak Current (no repetitive t = 0.1 ms)	Internally Limited	
I_O	Output Peak Current Repetitive f > 10 Hz	5.5	A
P_{tot}	Power Dissipation at T_{case} = 70 °C	36	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	2.2	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 14.4 V, R_L = 4 Ω, f = 1 kHz, T_{amb} = 25 °C) (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		8		18	V
I_o	Total Quiescent Drain Current			80		mA
R_i	Input Resistance			70		kΩ

MUTING FUNCTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Muting Attenuation	V_{ref} = 1 Vrms f = 100 Hz to 10 kHz	60			dB
	Muting-on Threshold Voltage	Pin 1	2.4			V
	Muting-off Threshold Voltage	Pin 1			0.8	V
	Stand-by Attenuation	V_{ref} = 1 V_{rms} f = 100 Hz to 10 kHz	60			dB
	Stand-by Quiescent Drain Current				100	µA
V_{os}	Output Offset Voltage				150	mV
P_o	Output Power	d = 10 % R_L = 4 Ω R_L = 3.2 Ω R_L = 2 Ω		22 26 28		W W W
THD	Distortion	P_o = 50 mW to 13 W		0.05		%
G_v	Voltage Gain (CL)			36		dB
e_N	Total Input Noise Voltage	R_g = 10 kΩ B = 22 Hz to 22 kHz		3	10	µV
SVR	Supply Voltage Rejection (closed loop)	R_g = 10 kΩ V_r = 1 V_{rms} f = 300 Hz	45	58		dB
T_{SD}	Thermal Shut Down Junction Temperature			145		°C

Figure 1 : Test and Application Circuit.

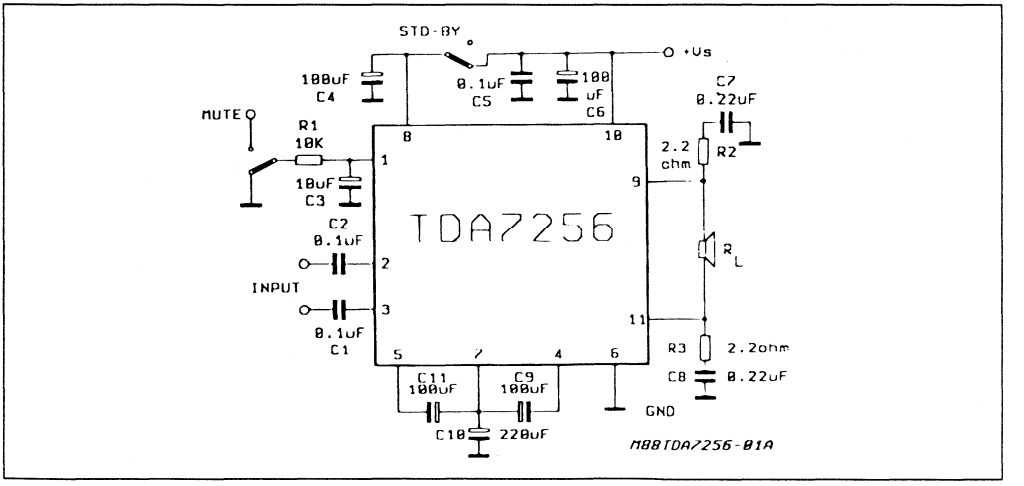


Figure 2 : Output Power vs. Supply voltage.

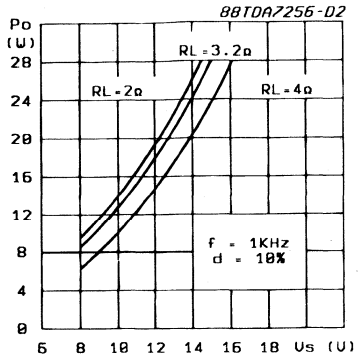


Figure 3 : Distortion vs. Output Power.

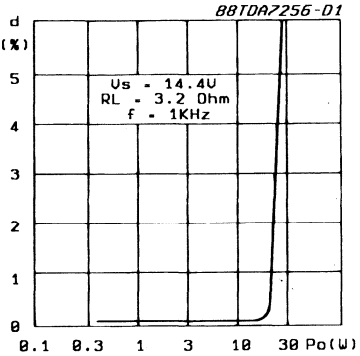


Figure 4 : Distortion vs. Frequency.

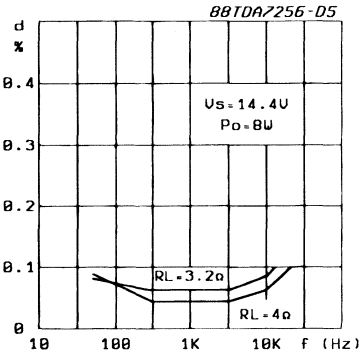


Figure 5 : Supply Voltage Rejection vs. Frequency.

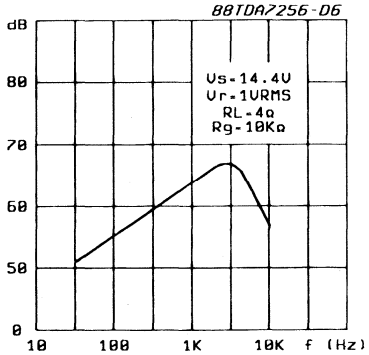


Figure 6 : Common Mode Rejection vs. Frequency.

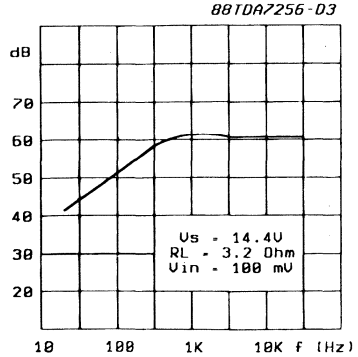


Figure 7 : Quiescent Current vs. Supply voltage.

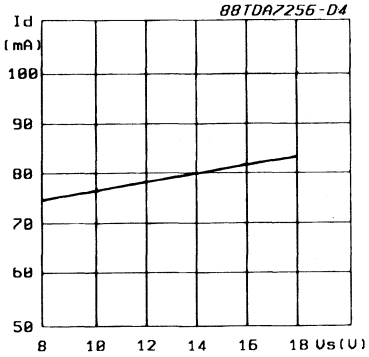
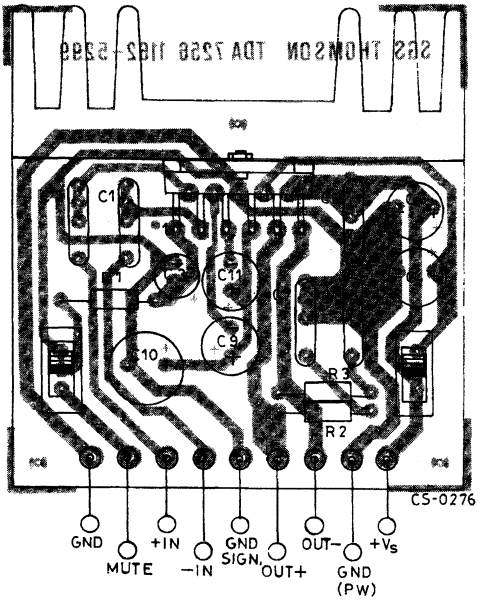
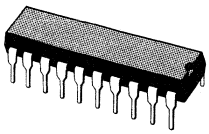


Figure 8 : P.C. and layout of the Fig.1 (1 : 1 scale).



HIGH EFFICIENCY AUDIO PWM DRIVER

- HIGH EFFICIENCY
- P_o = 30 W WITH POWER MOS BRIDGE
- LOW DISTORTION
- SINGLE SUPPLY OPERATION
- MUTING FACILITY
- THERMAL AND SHORT-CIRCUIT PROTECTION
- DUMP PROTECTION



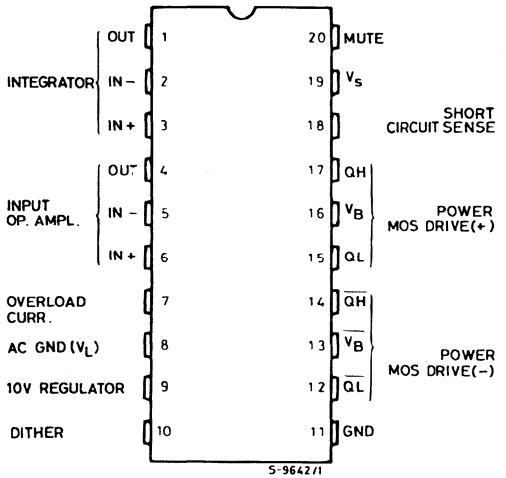
DIP - 20
(Plastic 0.4)

ORDER CODE : TDA7260

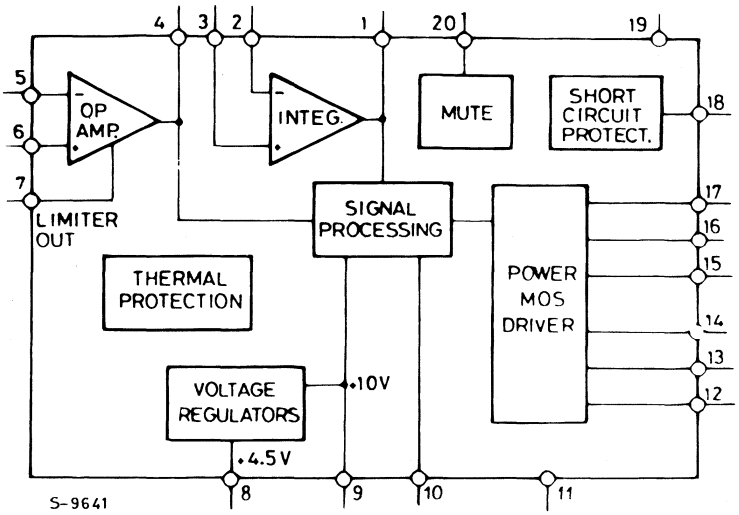
DESCRIPTION

The TDA7260 is a new type of audio driver mainly intended for use in car radio applications. In conjunction with four POWER MOS in bridge configuration it can deliver 30W (d 3% R_L = 2 Ω). The device acts in "class D" as a pulse width modulation circuit. That permits a very high efficiency (> 80% at rated output power) so no heatsinks are needed. Moreover, a built-in limiter reduces the clipping effects. The TDA7260 is a monolithic integrated circuit in a 20 lead dual in line plastic package.

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	30	V
V_s	Peak Supply Voltage (50 ms)	40	V
V_{IN}	Input Voltage	10	V
V_D	Differential Input Voltage	± 6	V
I_P	Peak Output Current	300	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80	°C/W

TEST CIRCUITS

Figure 1.

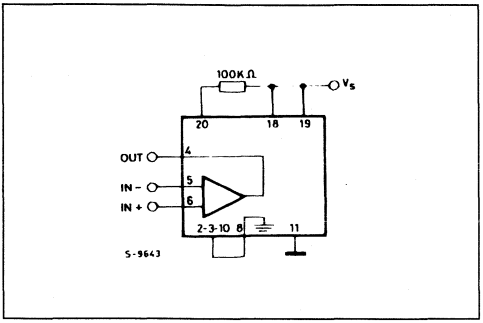


Figure 2.

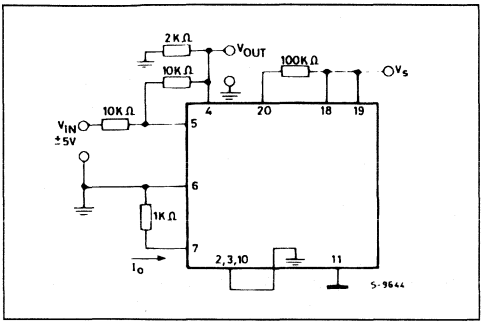


Figure 3.

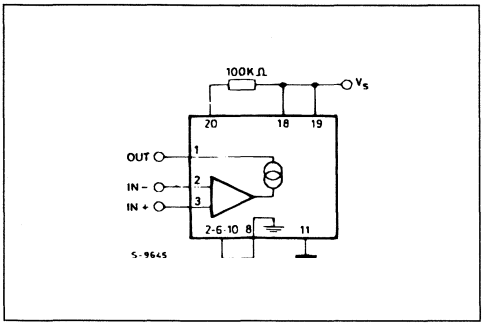


Figure 4.

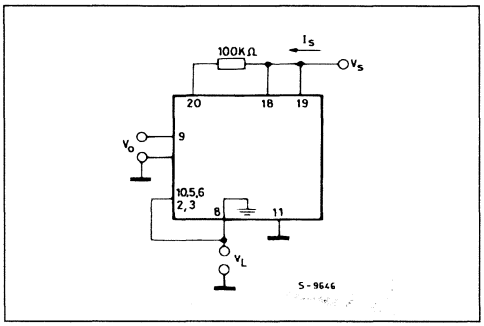


Figure 5.

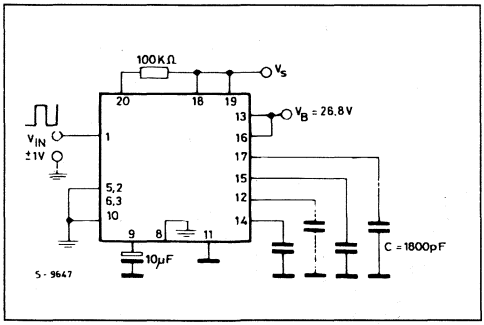
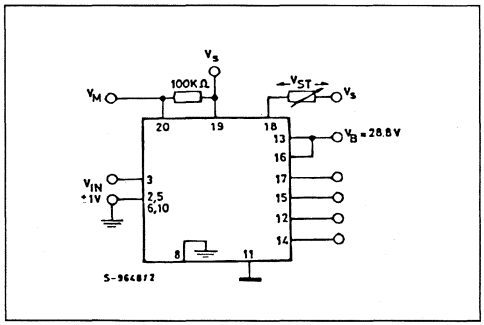


Figure 6.



ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, V_s = 14.4 V unless otherwise specified, refer to test circuit)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
OP AMP							
V_{os}	Input Offset Voltage				± 4	mV	1
I_b	Input Bias Current			120	300	nA	1
I_{of}	Input Offset Current				± 50	nA	1
G_v	Open Loop Voltage Gain		80			dB	1
d	Total Harmonic Distortion	f = 1 kHz A_v = 1		0.005		%	1
BW	Unity Gain Bandwith		0.8	1.8		MHz	1
CMRR	Common Mode Rejection	V_{IN} = 1 V f = 1 kHz	70	90		dB	1
SVR	Supply Voltage Rejection	V_r = 1 V f = 1 kHz	80	100		dB	1
E_n	Input Noise Voltage	B = 20 kHz		1		mV	1
I_n	Input Noise Current	B = 20 kHz		20		nA	1
SR	Slew Rate			0.8		V /ms	1
V_O	Output Swing	R_L = 2 KΩ A_v = 1	± 2.6		± 3.2	V	2
R_{IN}				100		kΩ	1
I_7	Overload Indicator Current			240		mA	2
INTEGRATOR							
V_{os}	Input Offset Voltage				± 4	mV	3
I_b	Input Bias Current			0.5	2.5	µA	3
I_{of}	Input Offset Current				± 250	nA	3
I_o	Output Current Swing Sink Source	 ΔV_{IN} = ± 1 V R_L = 0	 0.4 0.4	 1 1		 mA mA	3
V_o	Output Voltage Swing	ΔV_{IN} = ± 1 V R_L = 5 kΩ	± 3			V	3
CMRR	Common Mode Rejection	V_{IN} = 1 V f = 1 kHz	70	90		dB	3
SVR	Supply Voltage Rejection	V_r = 1 V f = 1 kHz	80	100		dB	3
R_{IN}			100			kΩ	3
BW	Unity Gain Bandwith			4		MHz	3
G_n	Forward Transconductance			30		mA/V	3
REGULATORS							
V_o	Output Stabilized Voltage			10		V	4
SVR	Supply Voltage Rejection	f = 1kHz V_r = 1 V	60	70		dB	4
V_I	Ground Voltage			4.5		V	4

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SYSTEM SPECIFICATION							
V_s	Operating Supply Voltage Range	See Fig. 24		(10.5 to 16)		V	
I_s	Supply Current	V_{IN} = 0		30	60	mA	4
V_{tm}	Mute Threshold Voltage (*)	V_{IN} = 0	3	4	5.5	V	6
V_{tmh}	Mute Threshold Hysteresis	V_{IN} = 0		0.5		V	6
$V_{o\,H}$	Output Swing (QH, $\overline{QH}$),	I = 70 mA	25			V	6
$V_{o\,H}$	Output Swing ($\overline{QL}$, QL)	I = 70 mA	10.8			V	6
$V_{o\,L}$	Output Swing (QH, $\overline{QH}$)	I = 70 mA			2.8	V	6
$V_{o\,L}$	Output Swing ($\overline{QL}$, QL)	I = 70 mA			2.8	V	6
V_{st}	Overload Sense Threshold		0.2		0.4	V	6
V_{om}	Muted Outputs	I = 70 mA Mute or Overload Condition			2.8	V	6
V_x	Gate Crossover Voltage	f = 1 kHz		2		V	5
COMPLETE SYSTEM							
I_o	Supply Current	V_{IN} = 0 $R_L = \infty$		90		mA	7
V_{of}	Output Offset Voltage	V_{IN} = 0		5		mV	7
CMRR	Common Mode Ripple Rejection	V_{IN} = 0.5 V f = 100 Hz		60		dB	7
SVR	Supply Voltage Ripple Rejection	ΔV_R = 0.5 V f = 100 Hz		60		dB	7
G_V	Voltage Gain	P_o = 1 W f = 1 kHz		12		dB	7
E_n	Output Noise Voltage	B = 20 kHz V_{IN} = 0		150		µV	7
P_o	Output Power	d = 2 % f = 1 kHz		32		W	7
d	Total Harmonic Distortion	f = 1 kHz Vo = 2 V		0.4		%	7
f_s	Switching Frequency	V_{IN} = 2 V $V_{10} = V_8$	70	125		kHz	7
f_d	Dither Frequency			20		Hz	7
η	Efficiency	P_o = 32 W f = 1 kHz		85		%	7

(*) Device on for V_{pin} 20 higher than V_{tm}.

Figure 7 : Application Circuit.

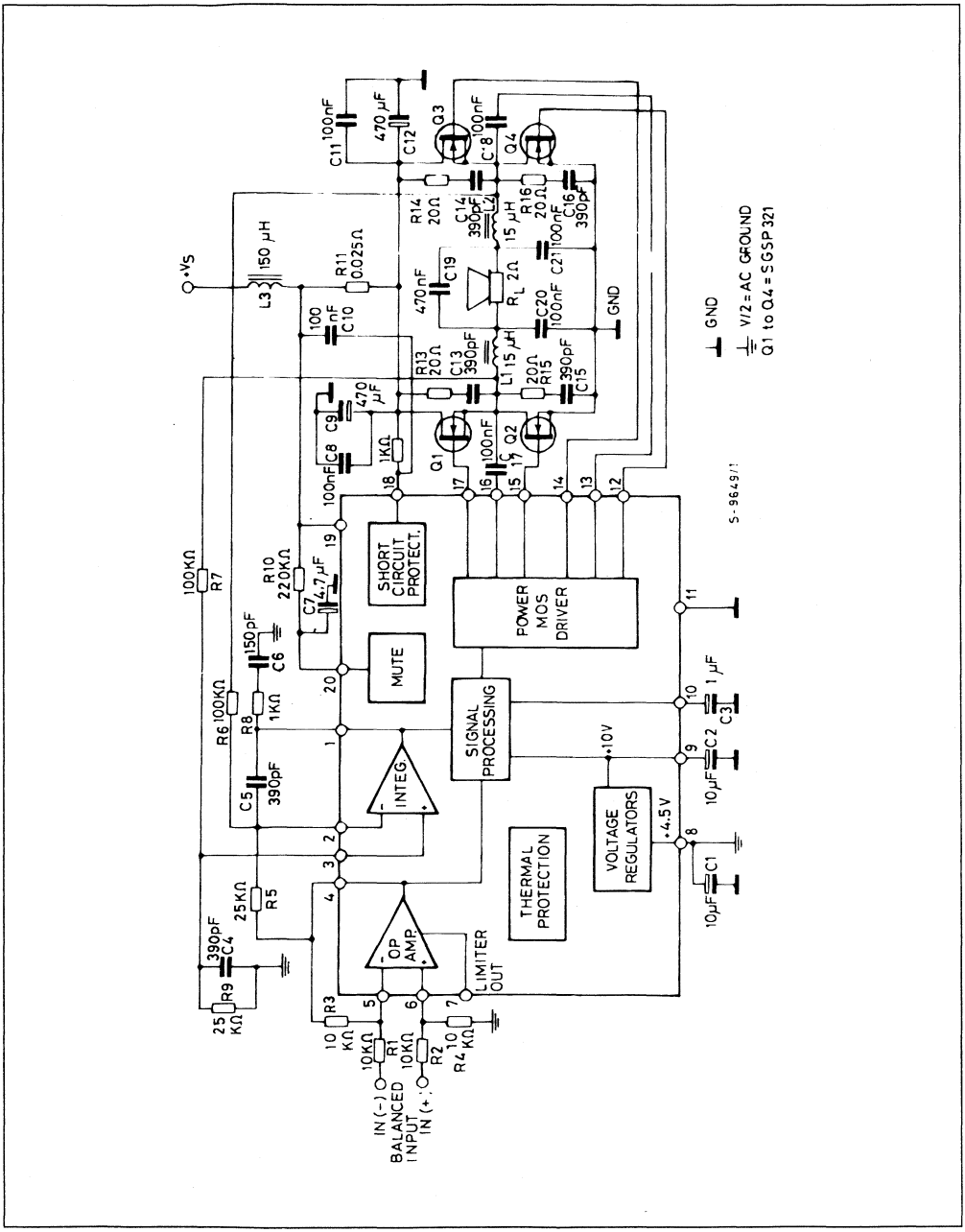


Figure 7a : P.C. Board and Components Layout of the Circuits of Fig. 7 (1 : 1 scale).

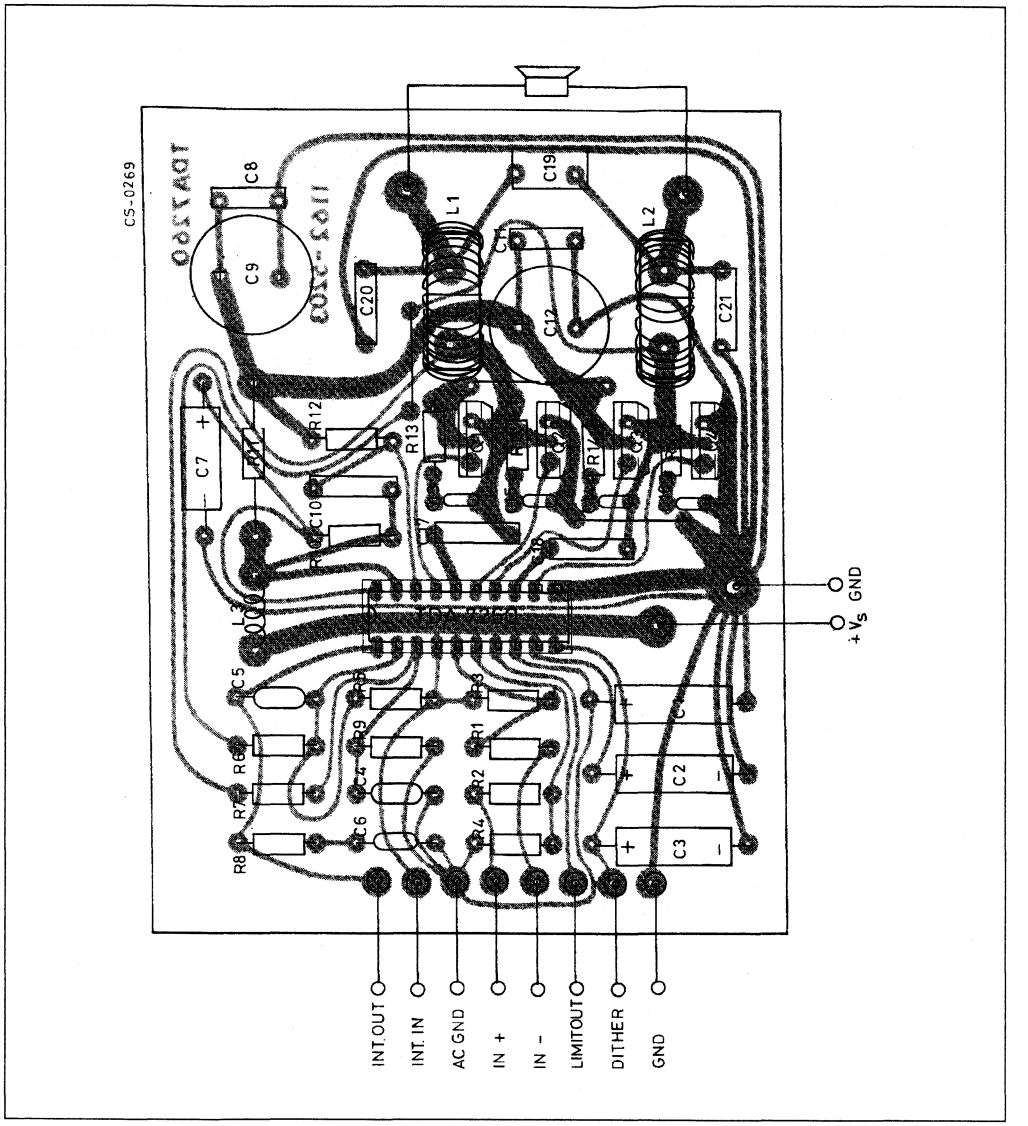


Figure 8 : Quiescient Current vs. Supply Voltage.

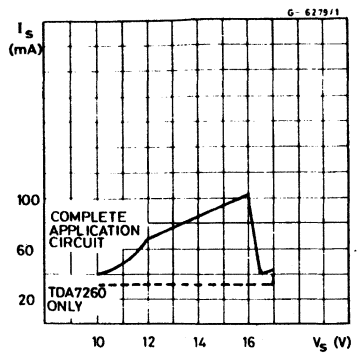


Figure 9 : Distortion vs. Output Power.

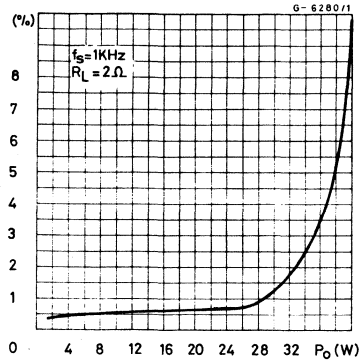


Figure 10 : Distortion vs.Frequency.

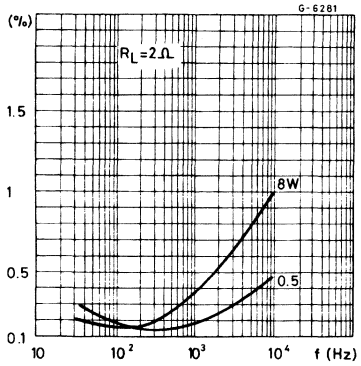


Figure 11 : Frequency Response.

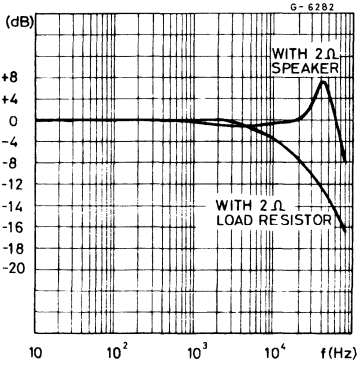


Figure 12 : Dither Frequency Versus $C_{(PIN\ 10)}$.

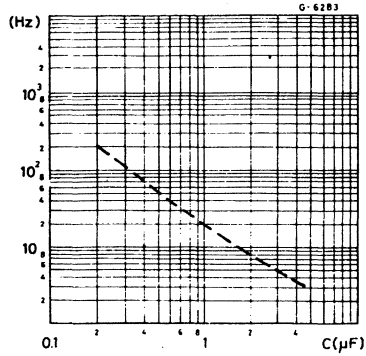


Figure 13 : Efficiency vs. Output Power.

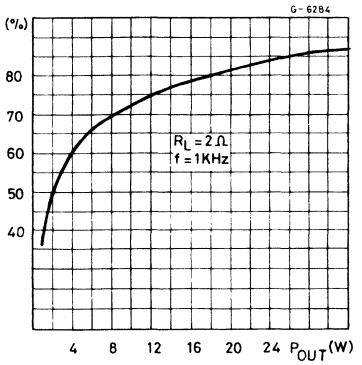


Figure 14 : Power Dissipation vs. Output Power.

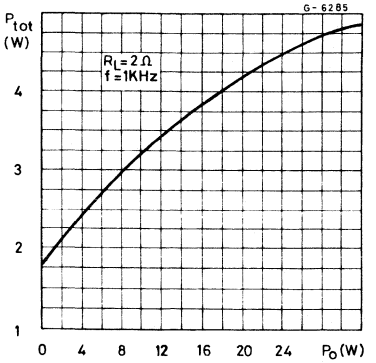


Figure 15 : Suggested Application Circuit Using the TDA7232 Preamplifier/Compressor.

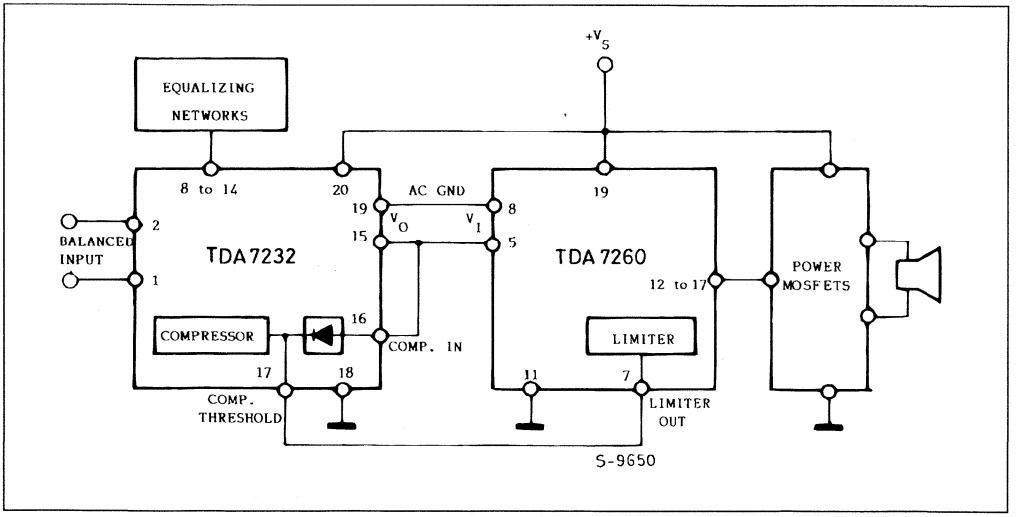


Figure 16 : 25 W Application Circuit.

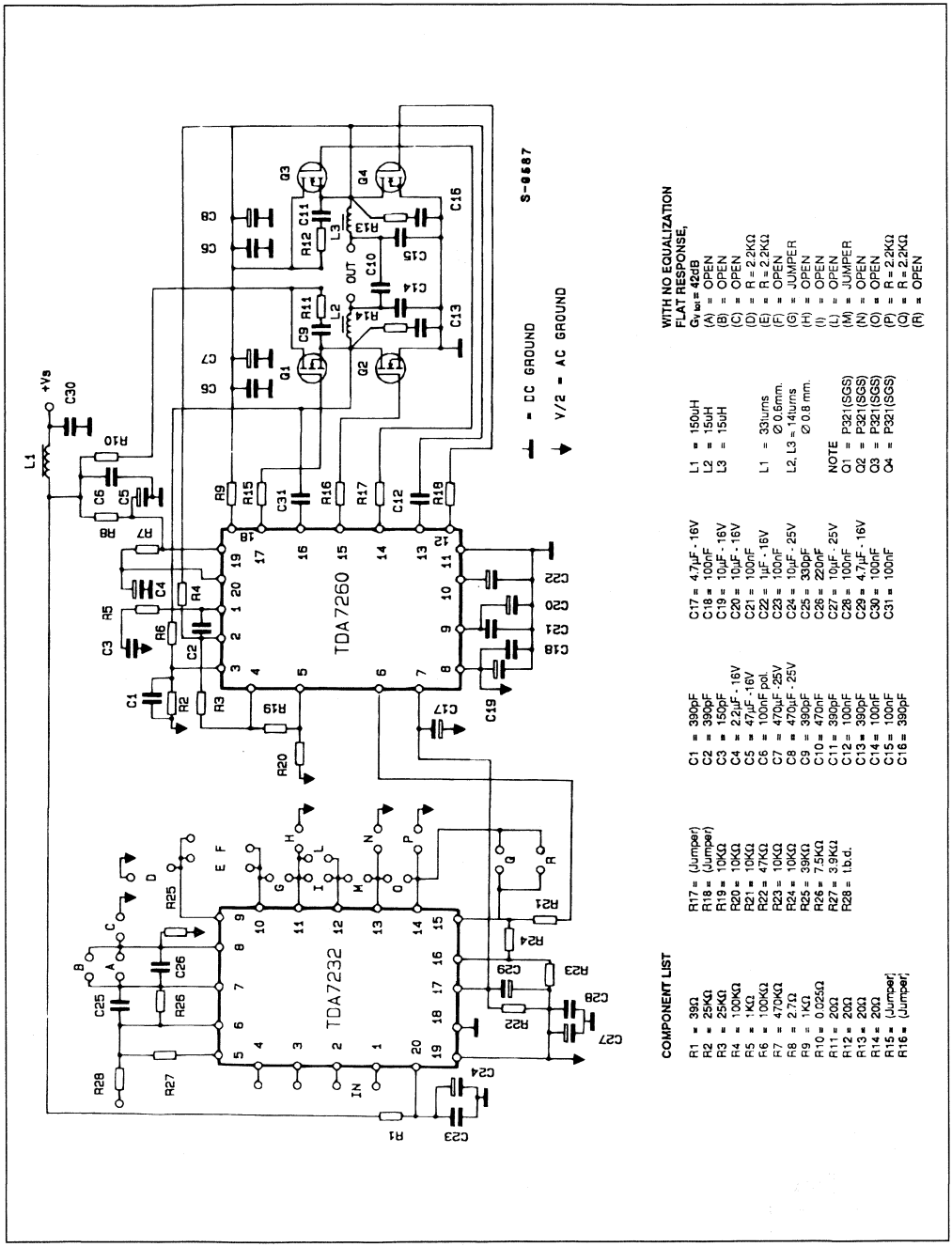
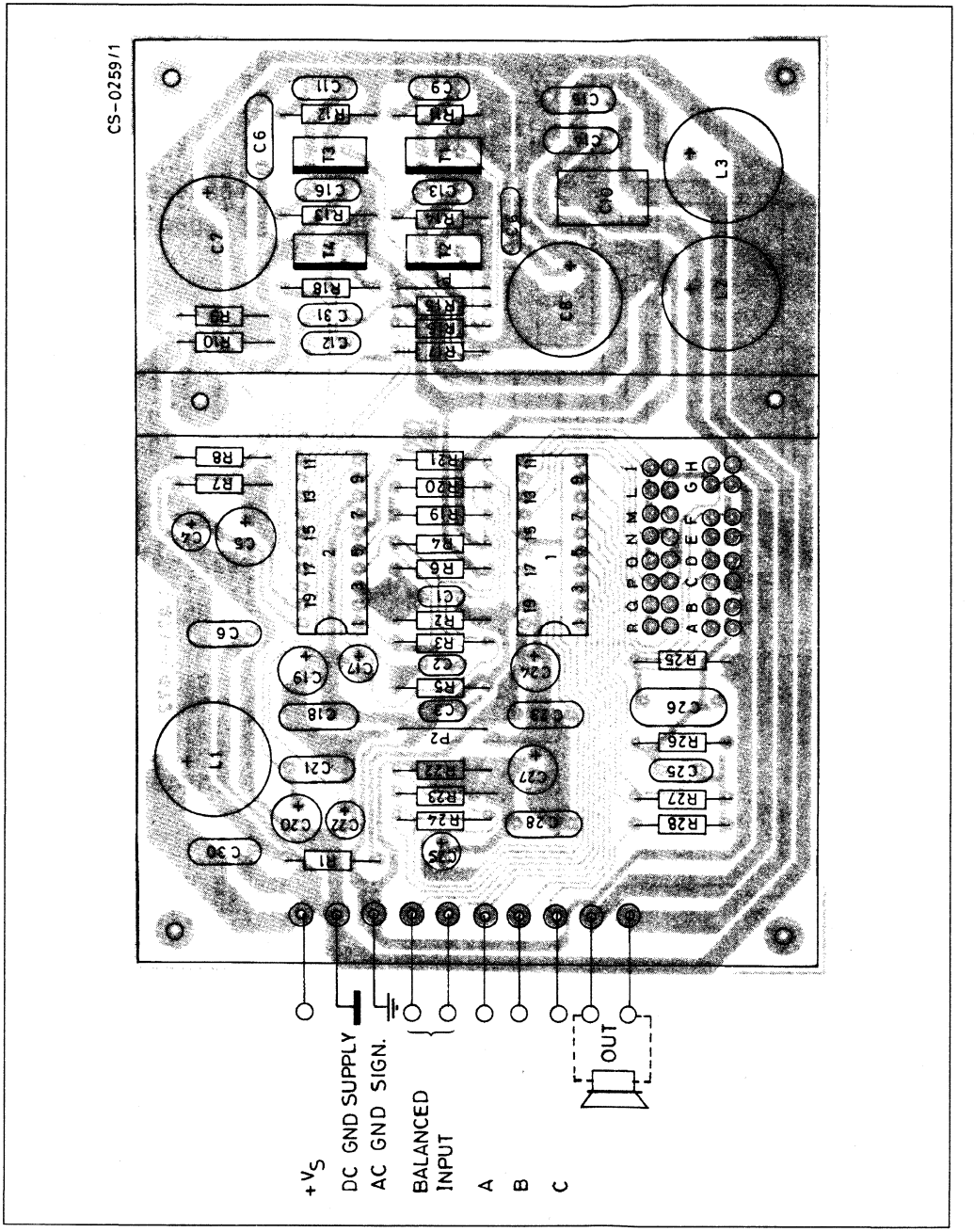
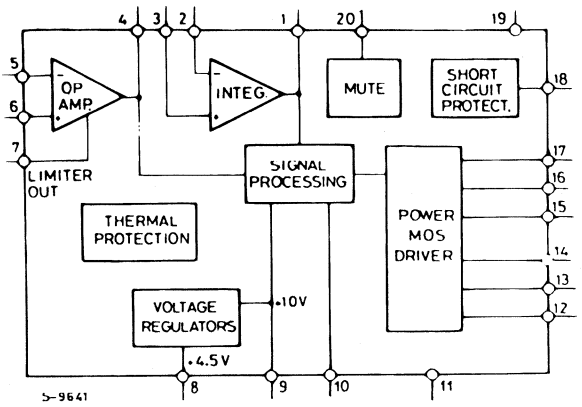


Figure 17 : P.C. Board and Components Layout of the Circuit of Fig. 16 (1 : 1 scale).



APPLICATION INFORMATION

Figure 18 : Block Diagram.



CIRCUIT DESCRIPTION

BLOCK DIAGRAM. Fig. 18 shows the circuit block diagram. Following are described the single circuit blocks and their functions.

VOLTAGE REGULATOR. It generates two values of reference voltage, accessible even on external pins. 10 V is the voltage that supplies all the analogic internal blocks. 4,5 V (V1) is the voltage value which stands for ground of the signal inside the chip.

INPUT AMPLIFIER, INTEGRATOR, COMPARATOR WITH HYSTERESIS, N-FET BLOCK DRIVER. These components implement the control system main loop, together with the external four power devices. The TSM (two state modulation) system is used.

The input amplifier is utilized in differential configuration, and refers the input signal to V1 voltage; in such way the chip turns to general use. On the input amplifier acts a dynamic limiter circuit, with intervention proportional to supply voltage avoiding overload and aliasing at lower V_S (Fig. 19).

Figure 19 : Duty Cycle Input Dynamic Limitation.

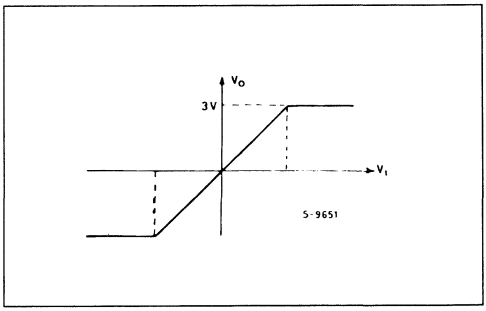
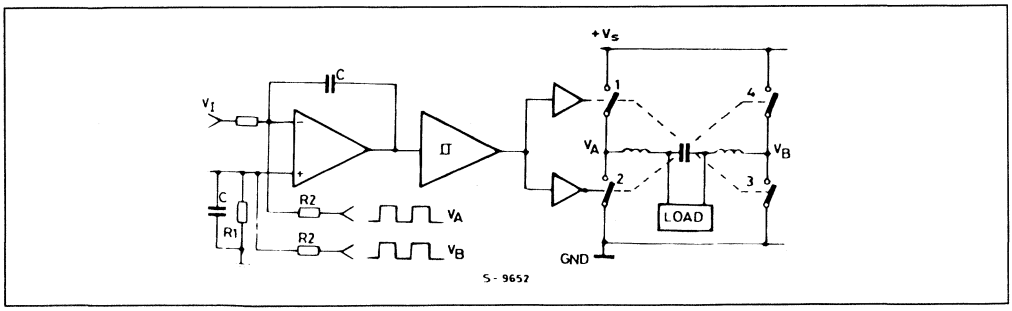


Figure 20 : Free Running Oscillator Principle.

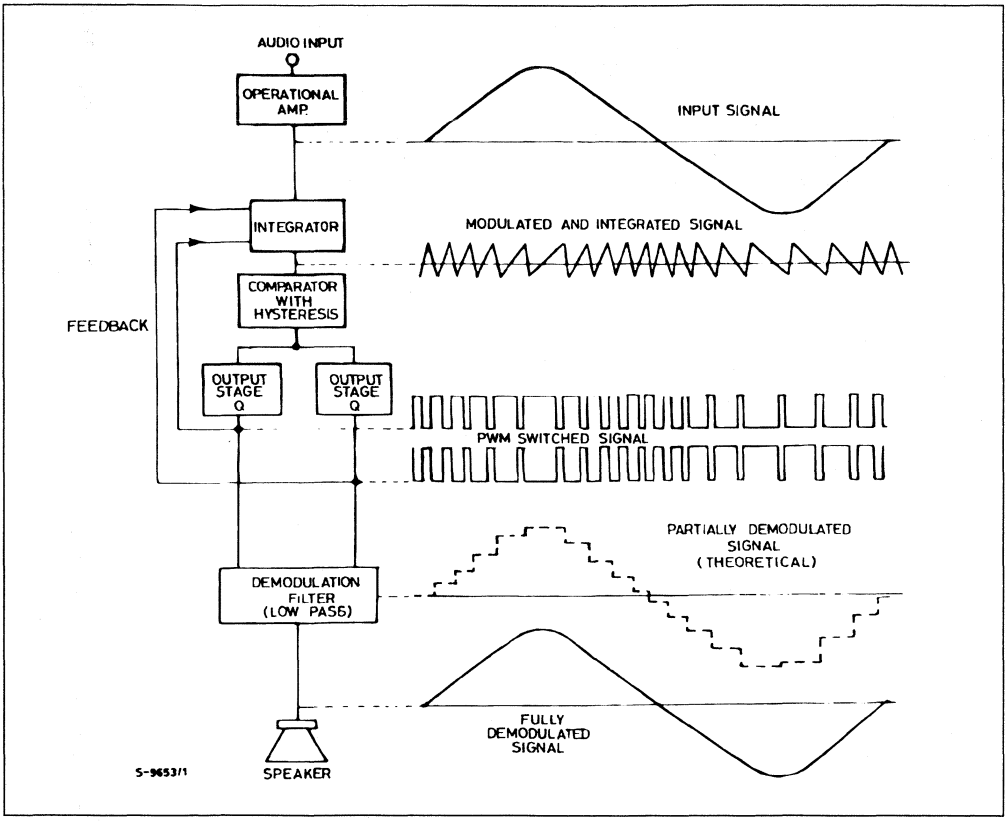


A signal for supplying an external compressor stage (i.e. TDA7232) is available.

For the effective control loop the feedback signal is taken from switched points of external power bridge (before LC output demodulation filter) and sent to the integrator (see Fig. 20).

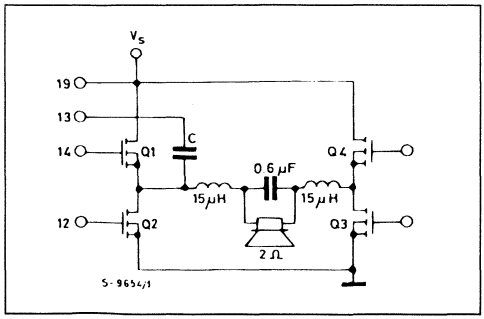
The triangle waveform at the integrator outpout drives the comparator with a hysteresis, and this supplies the correct time-intervals to the driving stages (Fig. 21).

Figure 21.



When an audio signal is introduced to the integrator, it generates an offset which varies the duty cycle and frequency of the switching output (with no audio signal the duty cycle is 50%). The bridge POWER MOS with the drain connected to the supply voltage, are driven in boostrap. The choice of MOS device is suggested by the high commutation speed and in order to reduce the chip dissipation. The Mosfets SGSP321 can be succesfully used. The LC filter on the bridge output demodulates the signal and reconstructs the sine wave on the speaker (see Fig. 22).

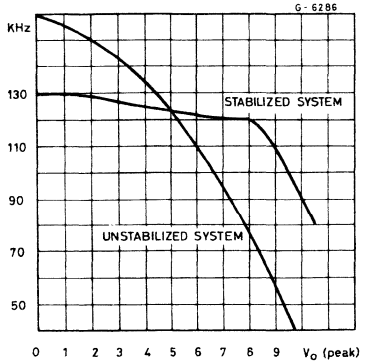
Figure 22.



SWITCHING FREQUENCY STABILIZER. It consists of a block which stabilizes the witching frequency of the system; it receives the supply voltage and the input signal amplitude as inputs, and accomplishes its function by varying the histeresis thresholds of the comparator. The purpose of such stabilizer is to reduce the range of the switching frequency (40KHz < F_{sw} < 200 KHz) avoiding greather variations versus supply voltage, input signal, output current. (Fig. 23).

DITHER OSCILLATOR. It is a low-frequency oscillator. Its frequency (20Hz typ.) is set by an external capacitor; at this value it determines a frequency switching modulation of about 10% around its nominal value, in order to minimize the problem of the spurious irradiations of the harmonics at the switching frequency (EMI).

Figure 23.



MUTE.It is a protection circuit which shuts the system off when the supply voltage is lower than 10.5 V and higher than 16 V. The switching-on is further delayed by an external capacitor. In mute condition the outputs are low (Figs. 24,25).

SHORT CIRCUIT PROTECTION. It is a comparator having an offset which senses the current drawn by the power stage by a voltage drop across an external resistor (internal V_{TH} = 250 mV): it acts on the mute circuit.

THERMAL AND DUMP PROTECTIONS. It shuts the device off when the junction temperature rises above 150 °C, and it has a hysteresis of above 20 °C typ. It acts on the mute circuit.

The device is protected against supply overvoltages (V_S = 40 V, t = 50 ms).

Figure 24.

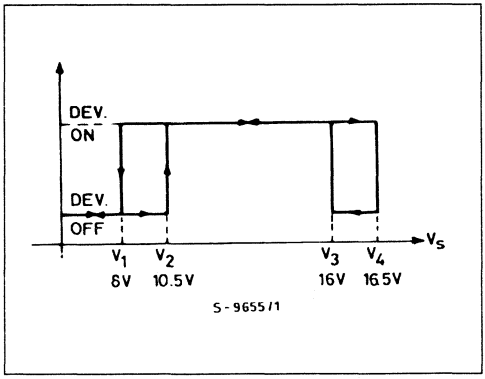
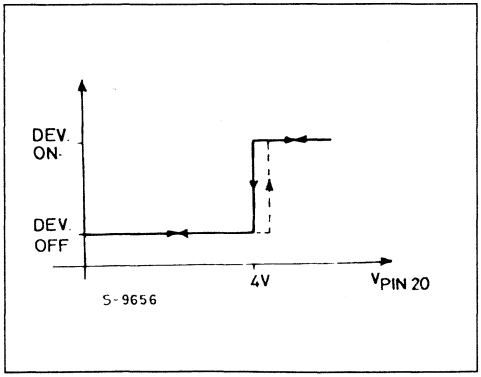


Figure 25.



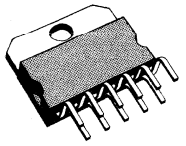
SGS-THOMSON MICROELECTRONICS

TDA7350

BRIDGE – STEREO AMPLIFIER FOR CAR RADIO

ADVANCE DATA

- VERY FEW EXTERNAL COMPONENTS
- NO BOUCHEROT CELLS
- NO BOOTSTRAP CAPACITORS
- HIGH OUTPUT POWER
- NO SWITCH ON/OFF NOISE
- VERY LOW STAND–BY CURRENT (100μA)
- FIXED GAIN
- PROGRAMMABLE TURN–ON DELAY
- OUTPUT AC–DC SHORT CIRCUIT TO GROUND AND TO SUPPLY VOLTAGE
- VERY INDUCTIVE LOADS
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GROUND



Multiwatt–11

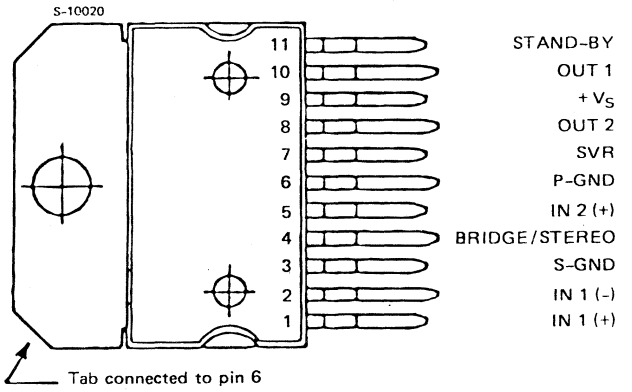
ORDER CODE : TDA7350

DESCRIPTION

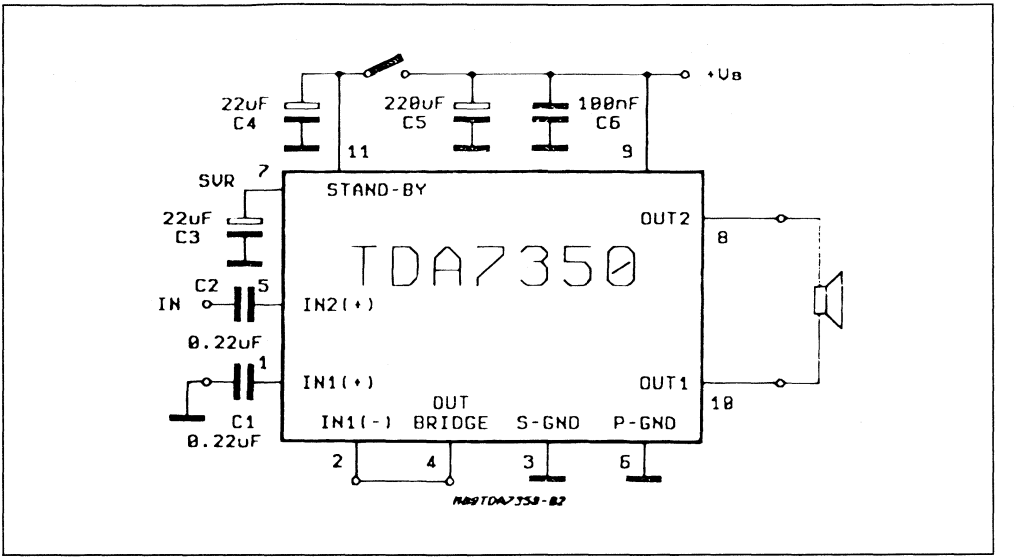
The TDA7350 is a new technology class AB Audio Power Amplifier in Multiwatt ® package designed for car radio applications. Thanks to the fully complementary PNP/NPN output configuration the high power performance of the TDA7350 are obtained without bootstrap capacitors.

A delayed turn–on mute circuit eliminates audible on/off noise, and a novel short circuit protection system prevents spurious intervention with highly indutive loads

PIN CONNECTION (top view)



APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Operating Supply Voltage	18	V
V_s	DC Supply Voltage	28	V
V_s	Peak Supply Voltage (for t = 50 ms)	40	V
I_O	I_{OUT} Peak (non rep. t = 100 µs)	5	A
I_O	I_{OUT} Peak (rep. freq. > 10 Hz)	4	A
P_{tot}	Power Dissipation at T_{case} = 80 °C	40	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuits, T_{amb} = 25 °C, V_s = 14.4V, f = 1 kHz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		8		18	V
I_d	Total Quiescent Drain Current	Stereo Configuration			120	mA
A_{SB}	Stand-by Attenuation		60	80		dB
I_{SB}	Stand-by Current				110	µA

STEREO

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
P_o	Output Power (each channel)	d = 10 % R_L = 1.6 Ω R_L = 2 Ω R_L = 3.2 Ω R_L = 4 Ω	7	12 11 8 6.5		W
d	Distortion	0.1 to 4 W R_L = 3.2 Ω			0.5	%
SVR	Supply Voltage Rejection	R_s = 0 to 10 kΩ f = 100 Hz	45	50		dB
CT	Crosstalk	f = 1 kHz f = 10 kHz	45	55 50		dB
R_i	Input Resistance		30	50		kΩ
G_v	Voltage Gain		27	29	31	dB
G_v	Voltage Gain Match				1	dB
E_{IN}	Input Noise Voltage	R_g = 50 Ω (*)		1.5		µV
		R_g = 10 kΩ (*)		2.0		µV
		R_g = 50 Ω (**)		2.0		µV
		R_g = 10 kΩ (**)		2.7		µV

BRIDGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
P_o	Output Power	d = 10 % R_L = 4 Ω R_L = 3.2 Ω	16	20 22		W
		d = 0.5 % R_L = 4 Ω			18	W
d	Distortion	R_L = 4 Ω f = 1 kHz P_o = 0.1 W to 10 W		0.15	1	%
V_{OS}	Output Offset Voltage				250	mV
SVR	Supply Voltage Rejection	R_s = 0 to 10 kΩ f = 100 Hz	45	50		dB
R_i	Input Resistance			50		kΩ
G_v	Voltage Gain		33	35	37	dB
E_{IN}	Input Noise Voltage	R_g = 50 Ω (*)		2.0		µV
		R_g = 10 kΩ (*)		2.5		µV
		R_g = 50 Ω (**)		2.7		µV
		R_g = 10 kΩ (**)		3.2		µV

(*) Curve A ; (**) 22Hz to 22KHz

Figure 1 : STEREO Test and Application Circuit.

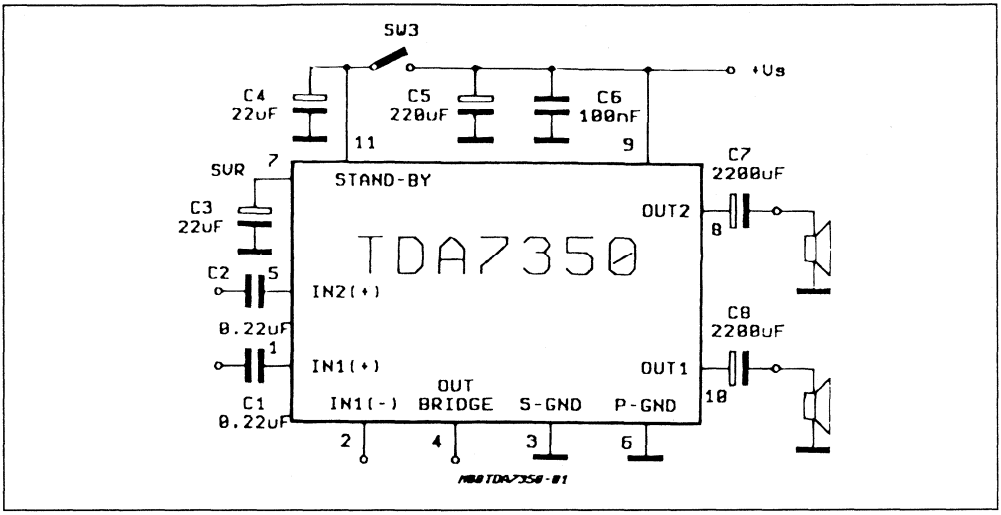


Figure 2 : P.C. and layout (stereo) of the Fig.1 (1:1 scale).

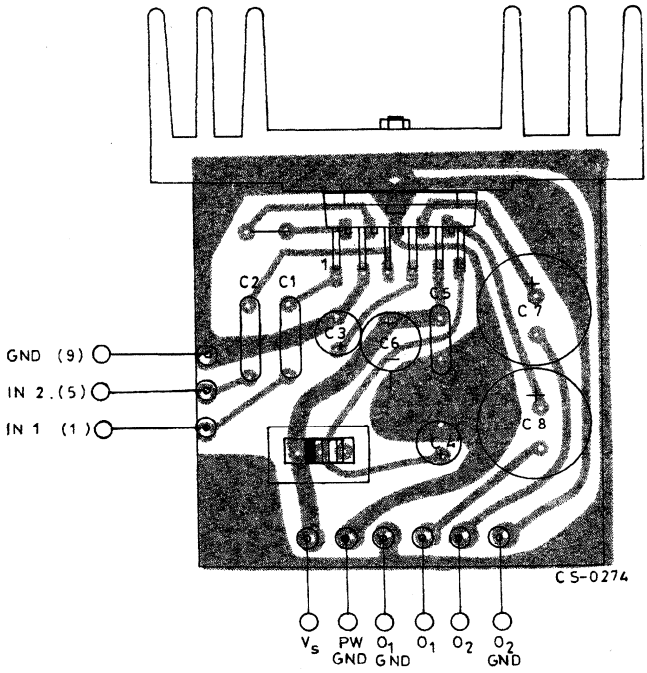


Figure 3 : BRIDGE Test and Application Circuit.

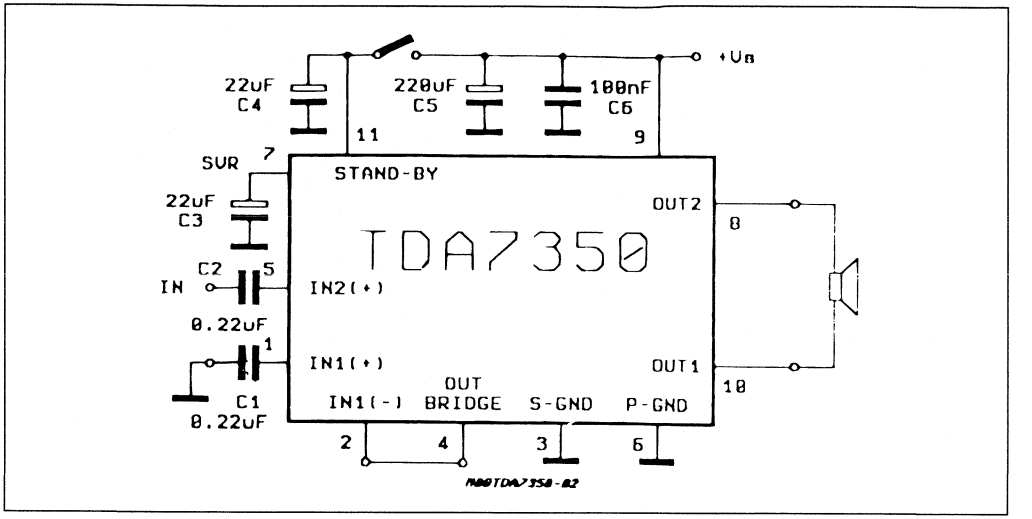


Figure 4 : P.C. and layout (bridge) of the Fig.3 (1 : 1 scale).

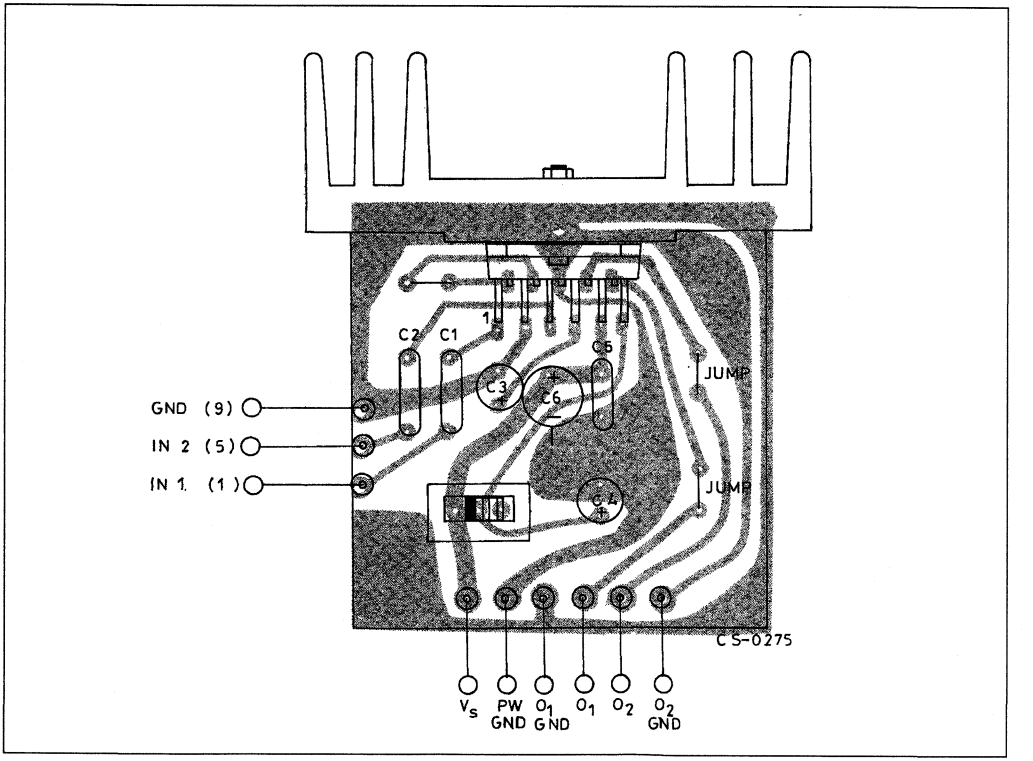


Figure 5 : Output Power Versus V_S (stereo)

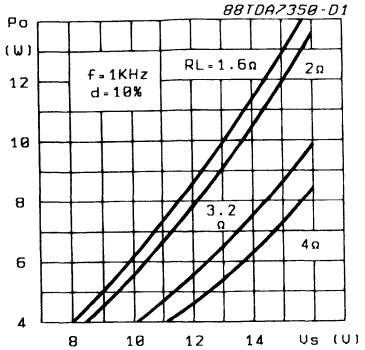


Figure 6 : P_{OUT} Versus Frequency (stereo)

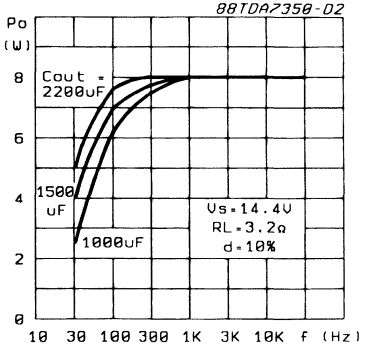


Figure 7 : P_{OUT} Versus Frequency (stereo)

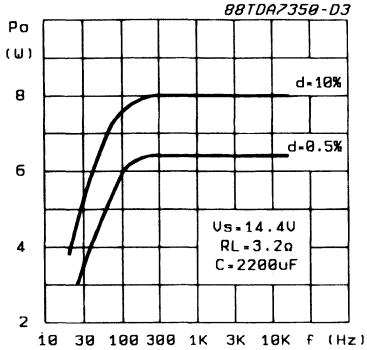


Figure 8 : Crosstalk vs Frequency (stereo)

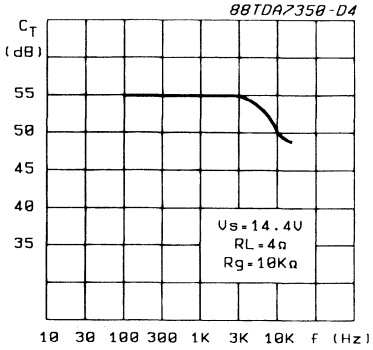


Figure 9 : SVR Versus C_{SVR} (stereo)

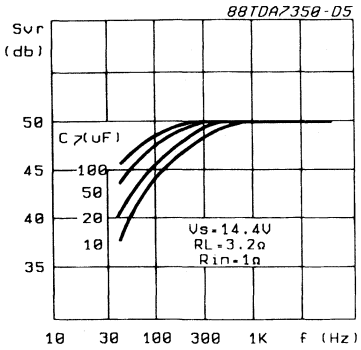


Figure 10 : Output Power Versus V_S (bridge)

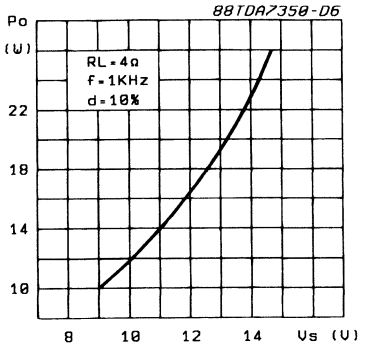


Figure 11 : Quiescent Current Versus V_S

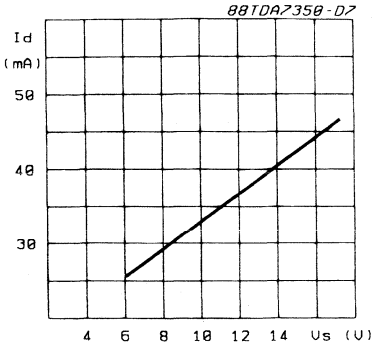


Figure 12 : Dissipated Power & Efficiency vs. P_O (stereo)

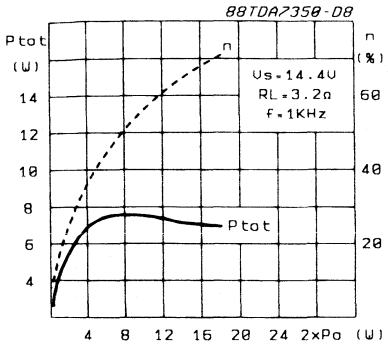
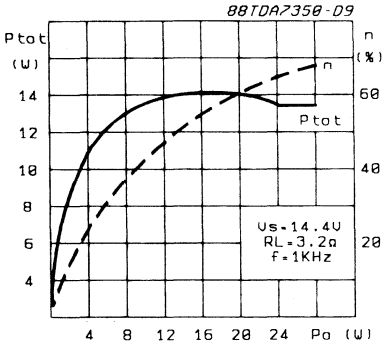


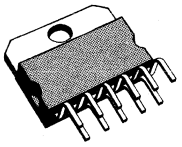
Figure 13 : Dissipated Power & Efficiency vs. P_O (bridge)



STEREO / BRIDGE AMPLIFIER WITH CLIPPING DETECTOR

ADVANCE DATA

- VERY FEW EXTERNAL COMPONENTS
- NO BOUCHEROT CELLS
- NO BOOTSTRAP CAPACITORS
- HIGH OUTPUT POWER
- NO SWITCH ON/OFF NOISE
- VERY LOW STAND–BY CURRENT
- FIXED GAIN
- PROGRAMMABLE TURN–ON DELAY
- CLIPPING DETECTION
- OUTPUT AC–DC SHORT CIRCUIT TO GROUND AND TO SUPPLY VOLTAGE
- VERY INDUCTIVE LOADS
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GROUND



Multiwatt–11

ORDER CODE : TDA7360

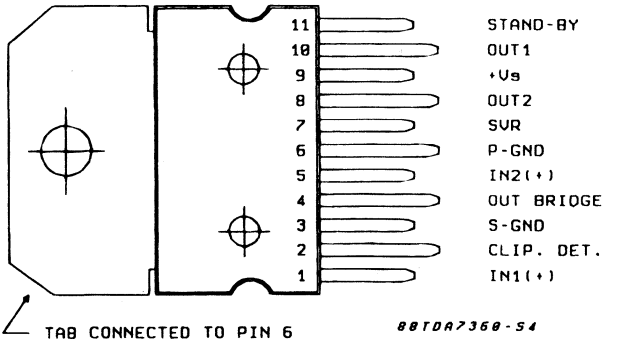
DESCRIPTION

The TDA7360 is a new technology class AB Audio Power Amplifier in Multiwatt package designed for car radio applications. Thanks to the fully complementary PNP/NPN output configuration the higher performances of the TDA7360 are obtained without bootstrap capacitors.

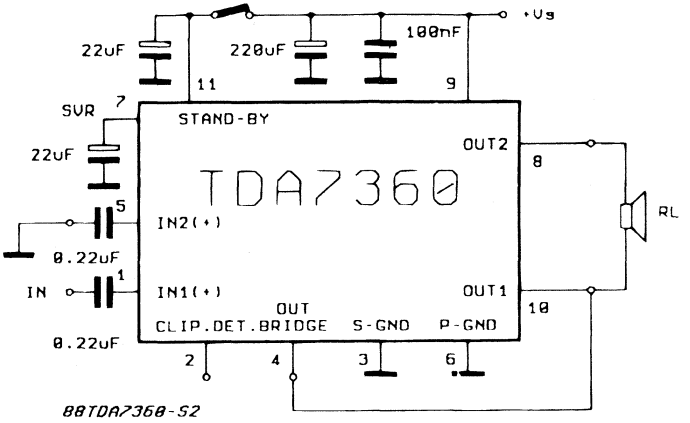
A delayed turn–on mute circuit eliminates audible on/off noise, and a novel short circuit protection system prevents spurious intervention with highly inductive loads

The device provides a circuit for the detection of clipping in the output stages. The output, an open collector, is able to drive systems with automatic volume control.

PIN CONNECTION (top view)



APPLICATION CIRCUIT (bridge)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
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V_s	DC Supply Voltage	28	V
V_s	Peak Supply Voltage (for t = 50 ms)	40	V
I_O	I_{OUT} Peak (non rep. t = 100 µs)	4.5	A
I_O	I_{OUT} Peak (rep. freq. > 10 Hz)	3.5	A
P_{tot}	Power Dissipation at T_{case} = 80 °C	40	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_{amb} = 25 °C, V_s = 14.4V, f = 1 kHz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		8		18	V
I_d	Total Quiescent Drain Current	Stereo Configuration		60		mA
ASB	Stand-by Attenuation		60	80		dB
I_{SB}	Stand-by Current				100	µA
I_{CO}	Clip Detector Current Average	d = 1 %		– 1		mA
dt_{co}	Distortion Threshold for Clip Detect. Output			0.5		%

STEREO

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
P_o	Output Power (each channel)	d = 10 % R_L = 1.6 Ω R_L = 2 Ω R_L = 3.2 Ω R_L = 4 Ω	7	12 11 8 6.5		W W W W
d	Distortion	f = 1 kHz 4 Ω 100 mW to 4 W		0.05		%
SVR	Supply Voltage Rejection	R_s = 0 to 10 kΩ f = 100 Hz		55		dB
CT	Crosstalk	f = 1 kHz f = 10 kHz		60 55		dB dB
R_i	Input Resistance			50		kΩ
G_v	Voltage Gain			20		dB
G_v	Voltage Gain Match.				1	dB
E_{in}	Input Noise voltage	22 Hz to 22 kHz R_g = 50 Ω R_g = 10 kΩ		3 3.5		µV µV

BRIDGE

Symbol	Parameter	Test Conditons	Min.	Typ.	Max.	Unit
V_{OS}	Ouput Offset Voltage				250	mV
P_o	Output Power	d = 10 % R_L = 4 Ω R_L = 3.2 Ω	16	20 22		W W
		d = 0.5 % R_L = 4 Ω		18		W
d	Distortion	R_L = 4 Ω f = 1 kHz P_o = 0.1 to 10 W		0.05		%
SVR	Supply Voltage Rejection	R_s = 0 to 10 kΩ f = 300 Hz to 3.5 kHz		55		dB
R_i	Input Resistance			50		kΩ
G_v	Voltage Gain			26		dB
E_{in}	Input Noise Voltage	22 Hz to 22 kHz R_g = 50 Ω R_g = 10 kΩ		6 7		µV µV

APPLICATION INFORMATION

The TDA7360 is equipped with an internal circuit able to detect the output stage saturation providing a proper current sinking into a proper open collector out. (pin 2) when a certain distortion level is reached on each output.
This particular function allows compression facility whenever the amplifier is overdriven, obtaining high quality sound at all listening levels.

Figure 1 : Dual Channel Distortion Threshold Detector.

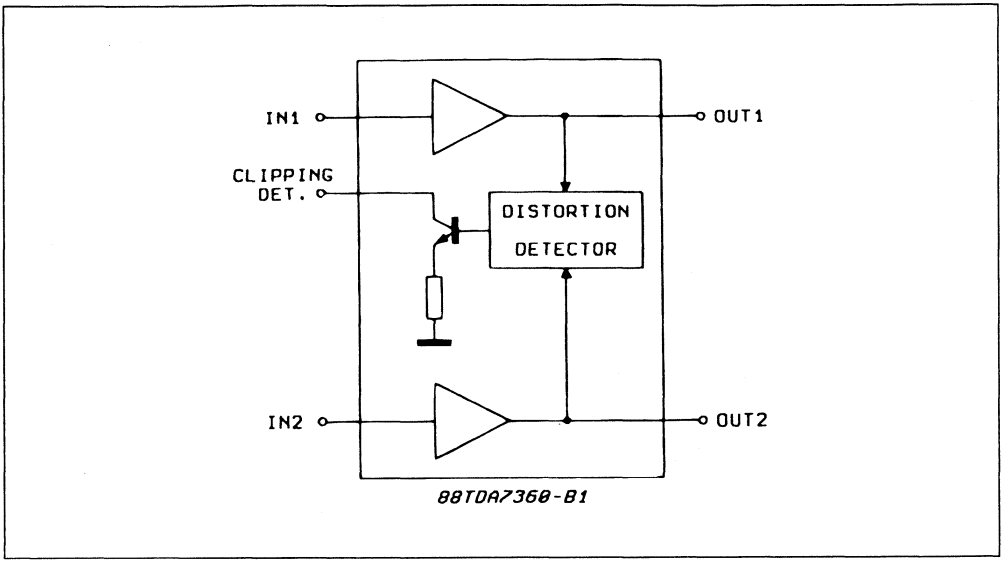


Figure 2 : Output from the Clipping Detector Pin. Versus Signal Distortion.

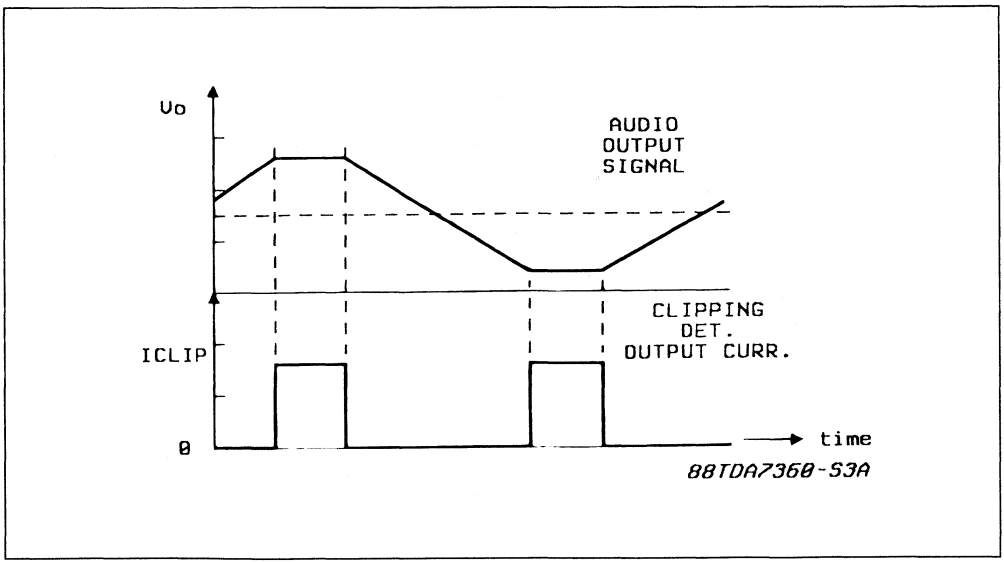


Figure 3 : Stereo Test and Application Circuit.

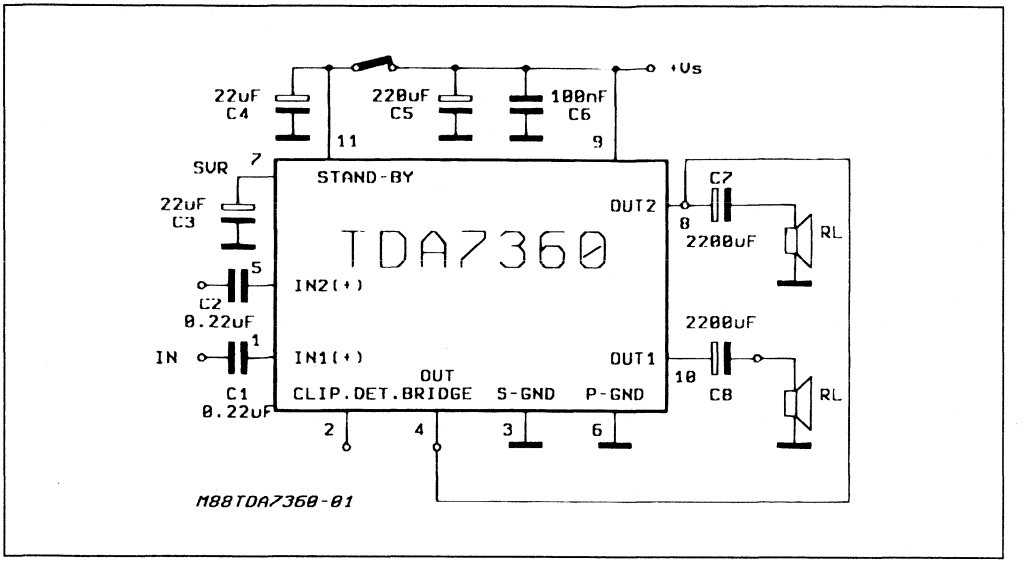


Figure 4 : P.C. and layout (stereo) of the Fig.3 (1 : 1 scale).

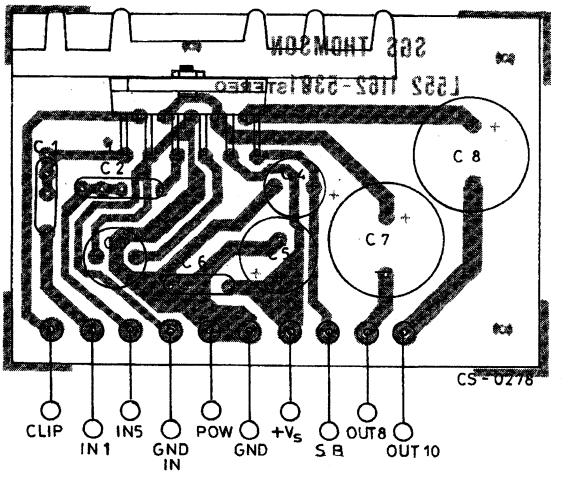


Figure 5 : Bridge Test and Application Circuit.

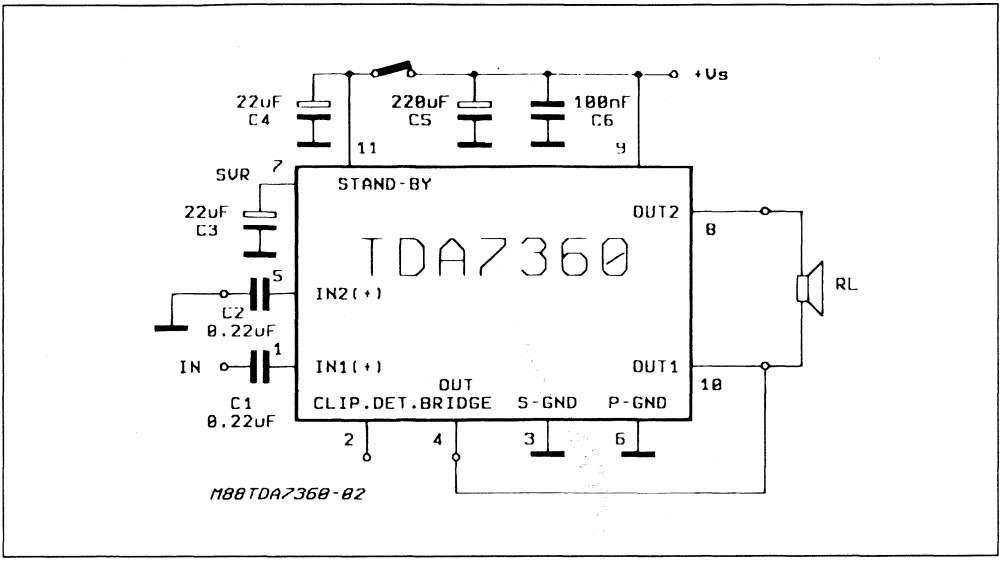
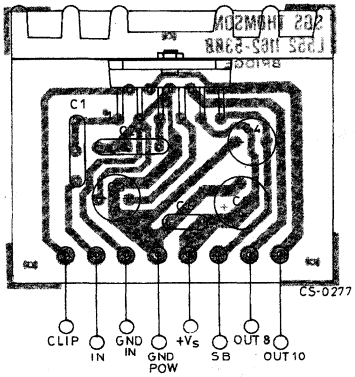


Figure 6 : P.C. and layout (bridge) of the Fig.5 (1 : 1 scale).



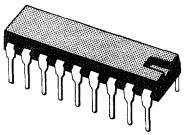
SGS-THOMSON

SGS-THOMSON MICROELECTRONICS

LM1837

DUAL LOW NOISE TAPE PREAMPLIFIER WITH AUTOREVERSE

- PROGRAMMABLE TURN-ON DELAY
- TRANSIENT-FREE MUTING AND POWER-UP NO POPS
- LOW-NOISE 0.6 μV/ CCIR/ARM
- HIGH POWER SUPPLY REJECTION – 95 dB
- LOW DISTORTION 0.03 % AND HIGH SLEW RATE – 6 V/μs
- SHORT CIRCUIT PROTECTION
- INTERNAL DIODES FOR DIODE SWITCHING APPLICATIONS



DIP18
(Plastic)

ORDER CODE : LM1837

DESCRIPTION

The LM1837 is a dual autoreversing high gain tape preamplifier for applications requiring optimum noise performance. It has forward (left, right) and reverse (left, right) inputs which are selectable through a high impedance logic pin. It is an ideal choice for a tape playback amplifier when a combination of low noise, autoreversing, good power supply rejection, and no power-up transients are desired. The application also provides transient-free muting with a single pole grounding switch.

PIN CONNECTION (top view)

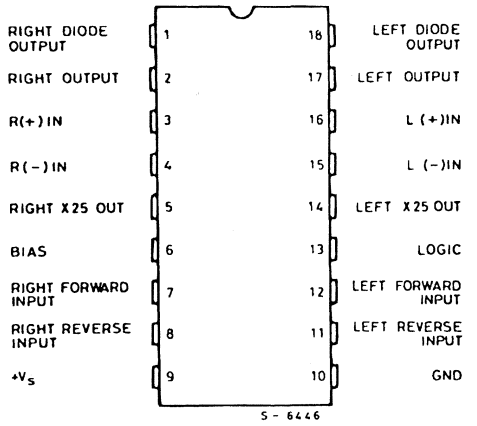
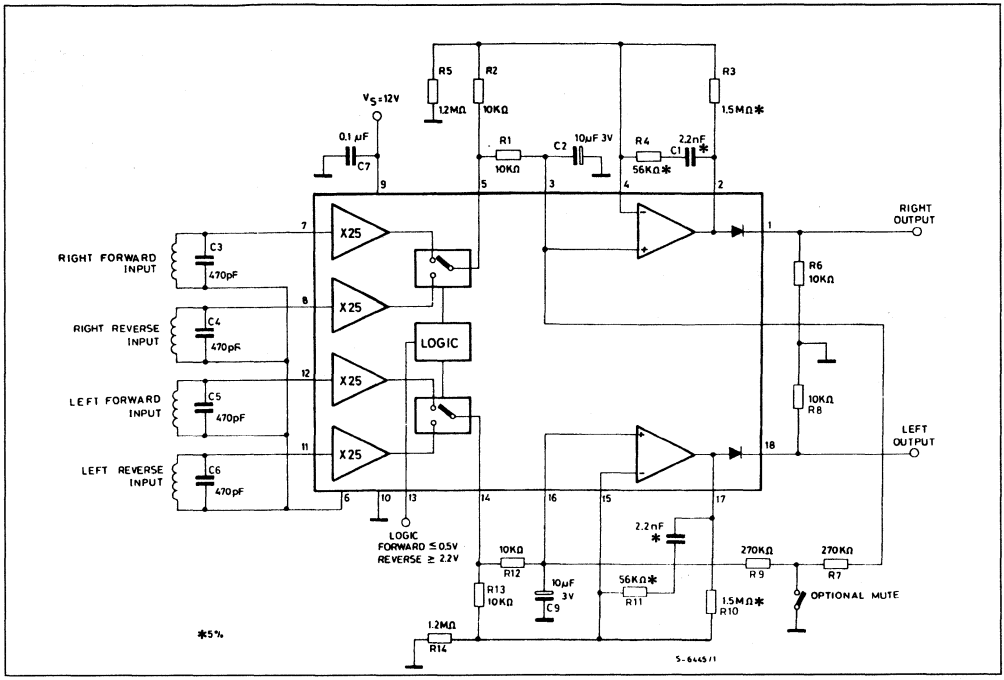
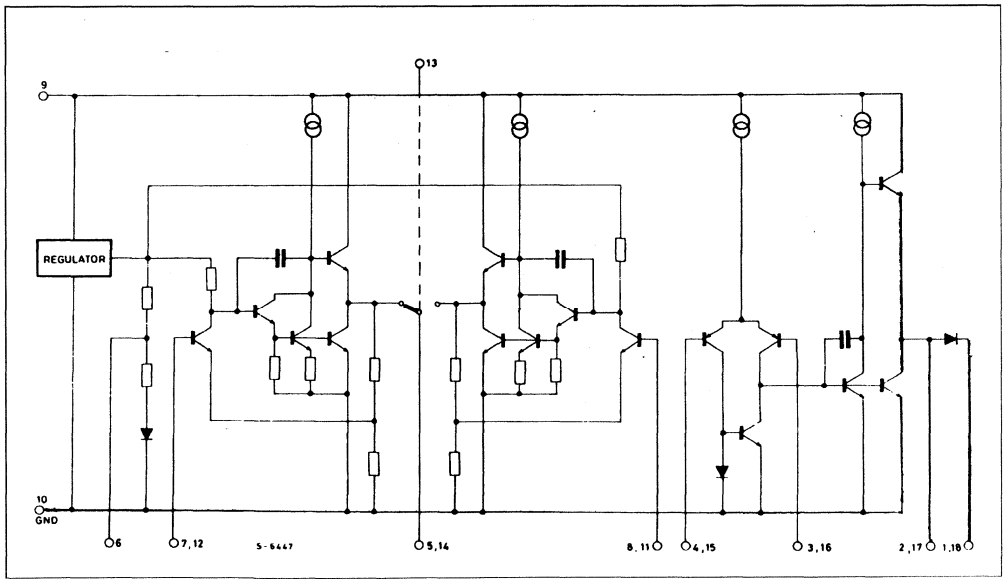


Figure 1 : Autoreversing Tape Playback Application.



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage Voltage on Pins 1 and 18	18 18	V V
P_{tot}	Package Dissipation	1390	mW
T_{stg}	Storage Temperature	– 65 to 150	°C
T_{op}	Operating Temperature Minimum Voltage on any Pin	0 to 70 – 0.1	°C V

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	90	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, V_S = 12 V, see test circuits)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	R5 removed from circuit for low voltage operation	4		18	V
I_S	Supply Current	V_S = 12 V		9	15	mA
d	Total Harmonic Distortion	f = 1 KHz V_i = 0.3 mV Pins 2 and 17, See Test Circuit		0.03		%
	THD + Noise (note 1)	f = 1 KHz V_o = 1 V Pins 2 and 17, See Test Circuit		0.1	0.25	%
SVR	Power Supply Rejection	Input Ref. f = KHz, 1 Vrms	80	95		dB
C_S	Channel Separation (note 2) Left to Right Forward to Reverse	f = 1 KHz, Output = 1 Vrms Output to Output	 40 40	 60 60		 dB dB
S/N	Signal-to-noise (note 3)	Unweighted 32 Hz - 12.74 KHz (note 1) CCIR/ARM (note 4) A Weighted CCIR, Peak (note 5)		 58 62 64 52		 dB dB dB dB
e_N	Noise	Output Voltage CCIR/ARM (note 4)		120	200	µV

INPUT AMPLIFIERS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_b	Input Bias Current Input Impedance AC Gain AC Gain Imbalance	f = KHz	 150 27	0.5 28 ± 0.15	2 29 ± 0.5	µA KΩ dB dB
V_O	DC Output Voltage		2.1	2.5	2.9	V
V_O	Output Voltage Mismatch	Pins 5 and 14	– 200	30	200	mV
I_{O+}	Output Source Current	Pins 5 and 14	2	10		mA
I_{O-}	Output Sink Current	Pins 5 and 14	300	600		µA

ELECTRICAL CHARACTERISTICS (continued)

LOGIC LEVEL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Forward				0.5	V
	Reverse		2.2			V
	Logic Pin Current			2	6	µA
	DC Voltage Change at Pins 5 and 14	Change Logic State	– 100	20	100	mV

OUTPUTS AMPLIFIERS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Closed Loop Gain	Stable Operation	5			V/V
G_v	Open Loop Voltage Gain	DC		100		dB
	Gain Bandwidth Product			5		MHZ
	Slew Rate			6		V/µs
V_{OS}	Input Offset Voltage			2	5	mV
I_{OS}	Input Offset Current			20	100	nA
I_i	Input Blas Current			250	500	nA
I_O+	Output Source Current	Pin 2 or 17	2	10		mA
I_O-	Output Sink Current	Pin 2 or 17	400	900		µA
V_O	Output Voltage Swing	Pin 2 or 17		11		Vp-p
	Output Diode Leakage	Voltage on Pins 1 and 18 = 18 V		0	10	µA

Note : 1 Measured with an average responding voltmeter using the filter circuit in figure 4. This simple filter is approximately equivalent a "brick wall" filter with a passband of 20 Hz to 20 KHz (see Application Hints). For 1 KHz THD the 400 Hz high pass filter on the distortion analyser is used.

2 Channel separation can be measured by applying the input signal through transformers to simulate a floating source (see Application Hints). Care must be taken to shield the coils from extraneous signal. Actual production test techniques simulate this floating source with a more complex op amp circuit.

3 The numbers are referred to an output level of 160 mV at pins 2 and 17 using the circuit figure 2. This corresponds.

4 Measured with an average responding voltmeter using the Dolby lab's standard CCIR filter having a unity gain reference 2 KHz.

5 Measured using the Rhode-Schwartz psophometer, mode UPGR.

Figure 2 : Test Circuit.

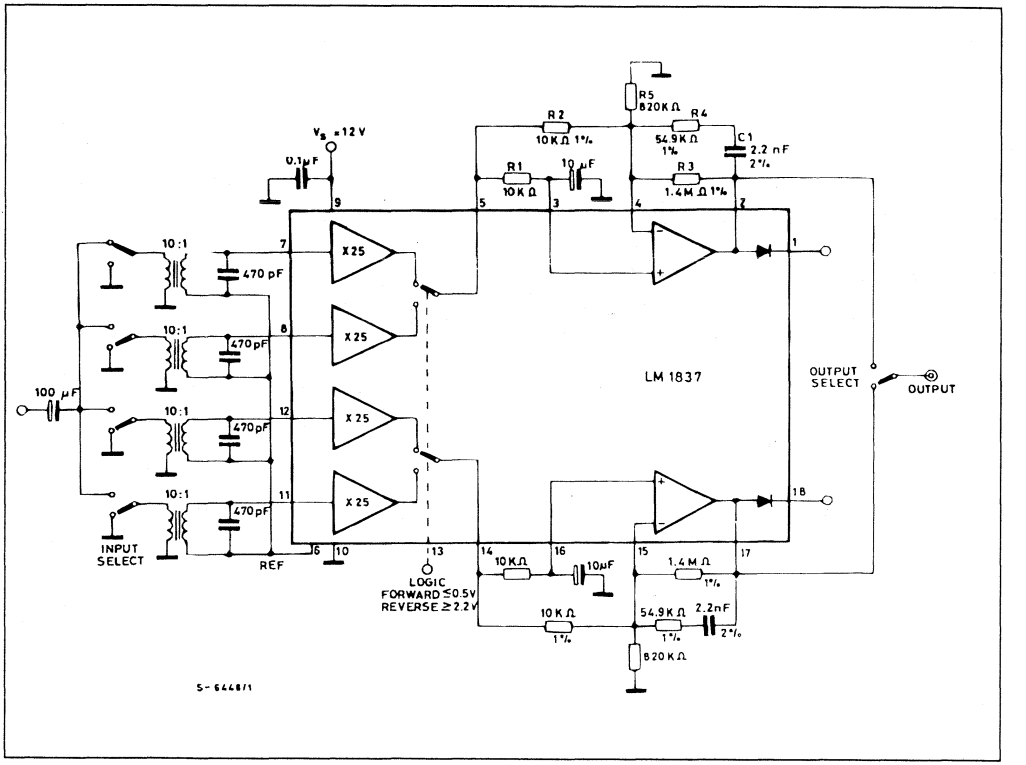


Figure 3 : Input Amplifier Distortion vs. Input Level.

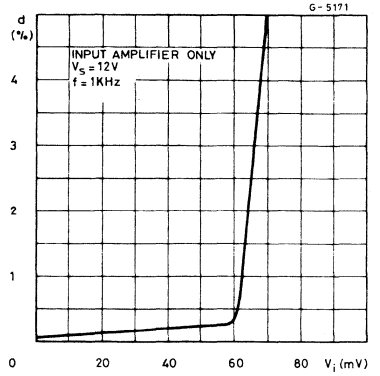


Figure 4 : Input Amplifier Gain and Phase vs. Frequency.

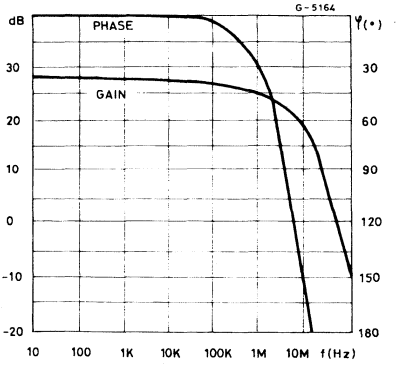


Figure 5 : Output Amplifier Open Loop Gain and Phase vs. Frequency.

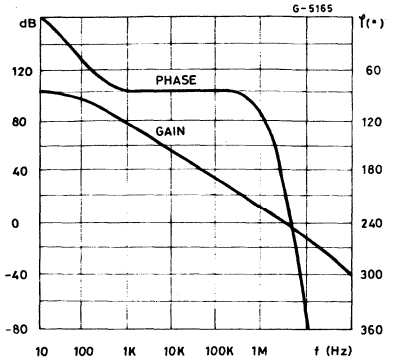


Figure 6 : Noise Voltage vs. Frequency..

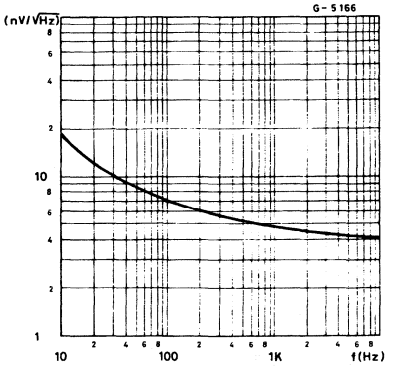


Figure 7 : Noise Current vs. Frequency.

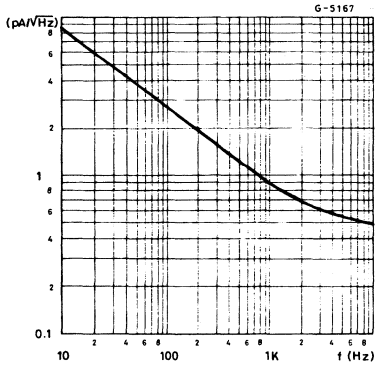


Figure 8 : Total Harmonic Distortion vs. Frequency.

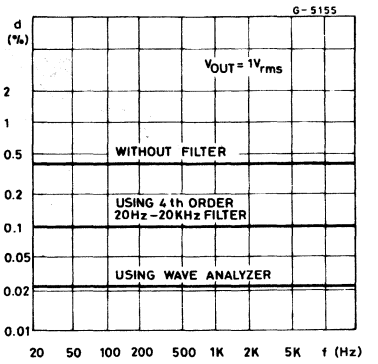


Figure 9 : Turn-on Delay vs. Component Values and Gain.

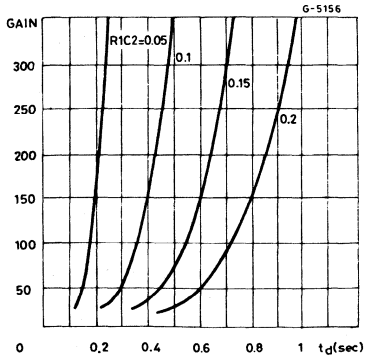


Figure 10 : 10 SVR vs. Frequency.

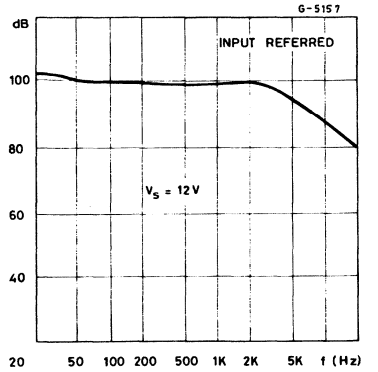


Figure 11 : SVR vs. Supply Voltage.

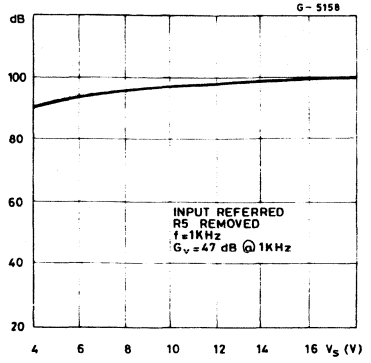


Figure 12 : Is vs. Vs.

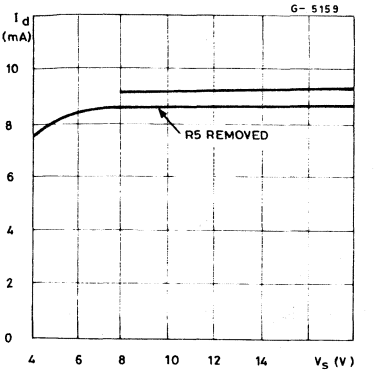


Figure 13 : Right to Left Channel Separation vs. Frequency.

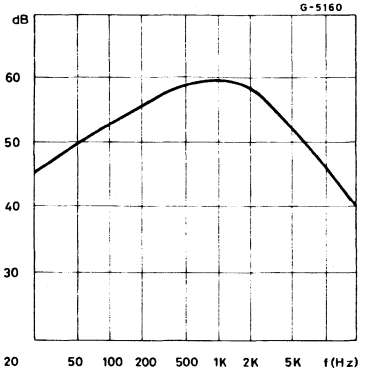


Figure 14 : Forward to Reverse Channel Separation vs. Frequency.

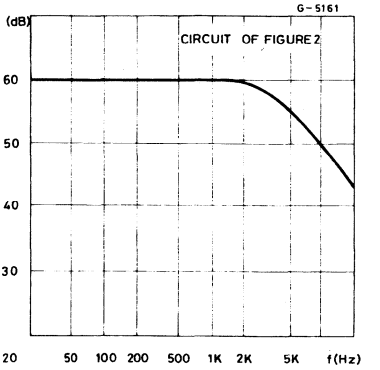


Figure 15 : Input Amplifier DC Output Voltage vs. Temperature (pins 5, 4).

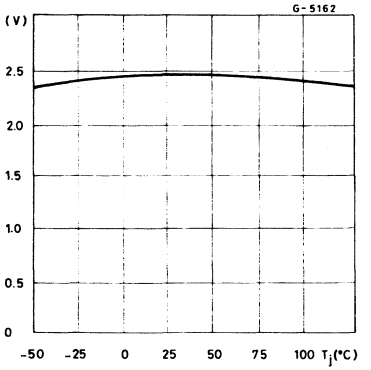


Figure 16 : Frequency Response of Test Circuit.

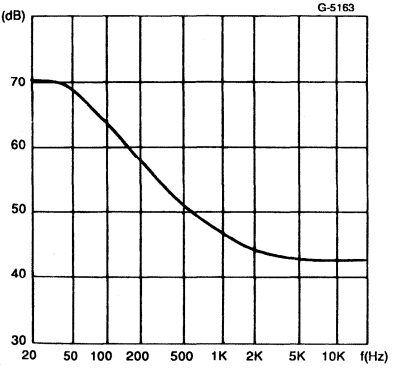
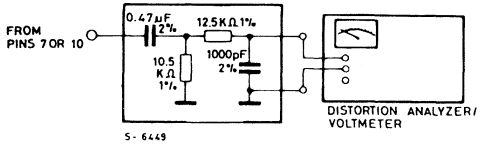


Figure 17 : Simple 32 Hz - 12740 Hz Filter and Meter.



APPLICATION INFORMATION

EXTERNAL COMPONENTS (figures 1 and 18)

Component	Normal Range of Value and Function
R1, C2 and R12, C9	2KΩ - 40 KΩ, 0.1 µF - 10 µF (low leakage). Set turn-on delay and second amplifier's low frequency pole. Leakage current in C2 results in DC offset between the amplifier's inputs and therefore this current should be kept low. R1 is set equal to R2 such that any input offset voltage due to bias current is effectively cancelled. An input offset voltage is generated by the input offset current multiplied by the value of these resistors.
R2, R3 and R13, R10	2 KΩ - 40 KΩ, 500 KΩ - 10 KΩ. Set the DC and frequency gain of the output amplifier. The total input offset voltage will also be multiplied by the DC gain of this amplifier. They are therefore essential to keep the input offset voltage specification in mind when employing high DC gain in the output amplifier ; i. e., 5 mV x 400 = 2 V offset at the output.
R4, C1 and R11, C8	10 KΩ - 200 KΩ, 470 pF to 10 nF. Set tape playback equalization characteristics in conjunction with R3 (calculations for the component values are included in the application (hints section).
R6, R8	2 KΩ - 47 KΩ. Blas the output diode in DC switching applications. These resistors can be excluded if diode switching is not desired.
C3...C6	100 pF - 1000 pF. Often used to resonate with tape head in order to compensate for tape playback losses including tape head gap and eddy current. For a typical cassette tape head, the resonant frequency selected is usually between 13 KHz and 17 kHz.
R5, R14	100 KΩ - 10 MΩ. Increase the output DC bias voltage from the nominal 2.5 V value (see application information).
R7, R9	Optionally used for tape muting. The use of these resistor can also provide "no-pop" turn-off if desired (see application information)

Figure 18 : Autoreversing Tape Plyback Application.

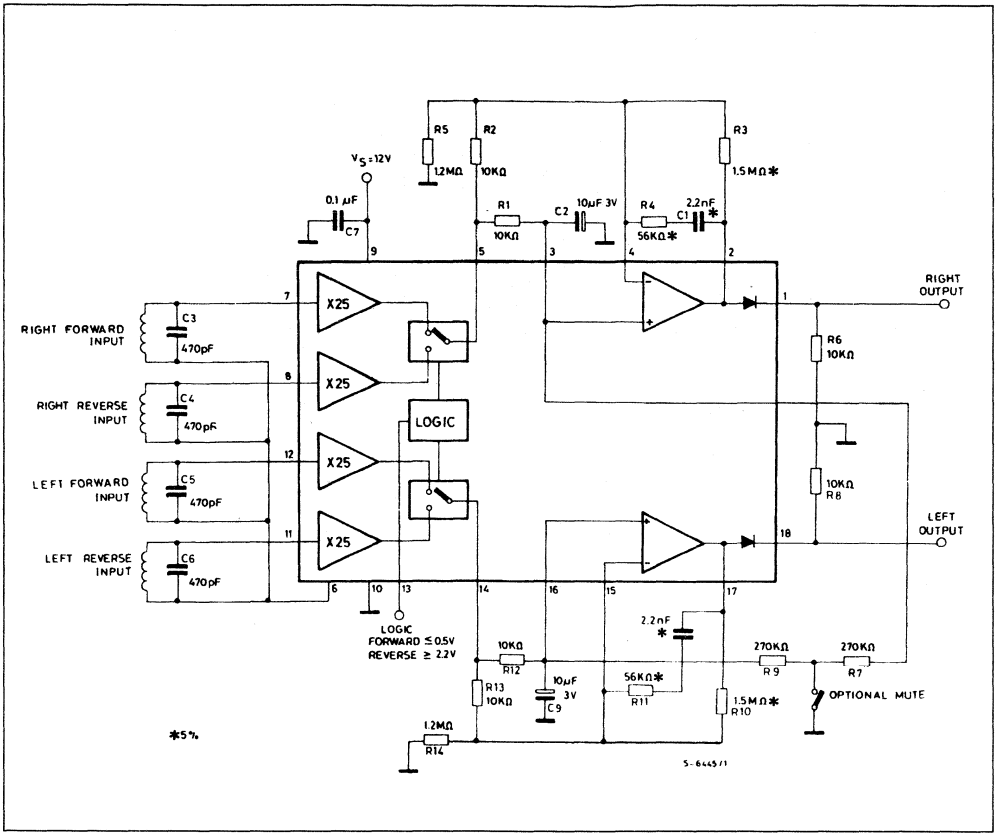
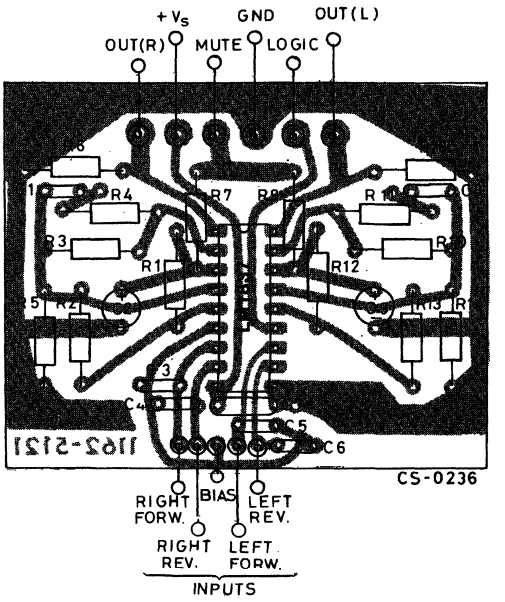


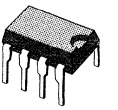
Figure 19 : P. C. Board and Components Layout of the Circuit of fig. 18 (1 : 1 scale)



TDA2320A

MINIDIP STEREO AMPLIFIER

- WIDE SUPPLY VOLTAGE RANGE (3 to 36 V)
- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW CURRENT CONSUMPTION (0.8 mA)
- VERY LOW DISTORTION
- NO POP-NOISE
- SHORT CIRCUIT PROTECTION



MINIDIP
(Plastic)

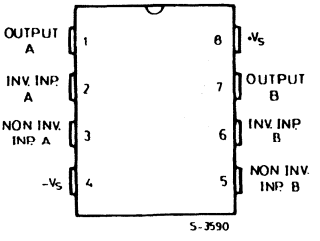
ORDER CODE : TDA2320A

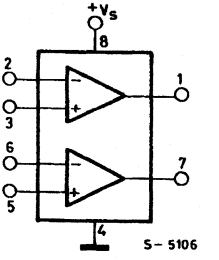
DESCRIPTION

The TDA2320A is a stereo class A preamplifier intended for application in portable cassette players and high quality audio systems.

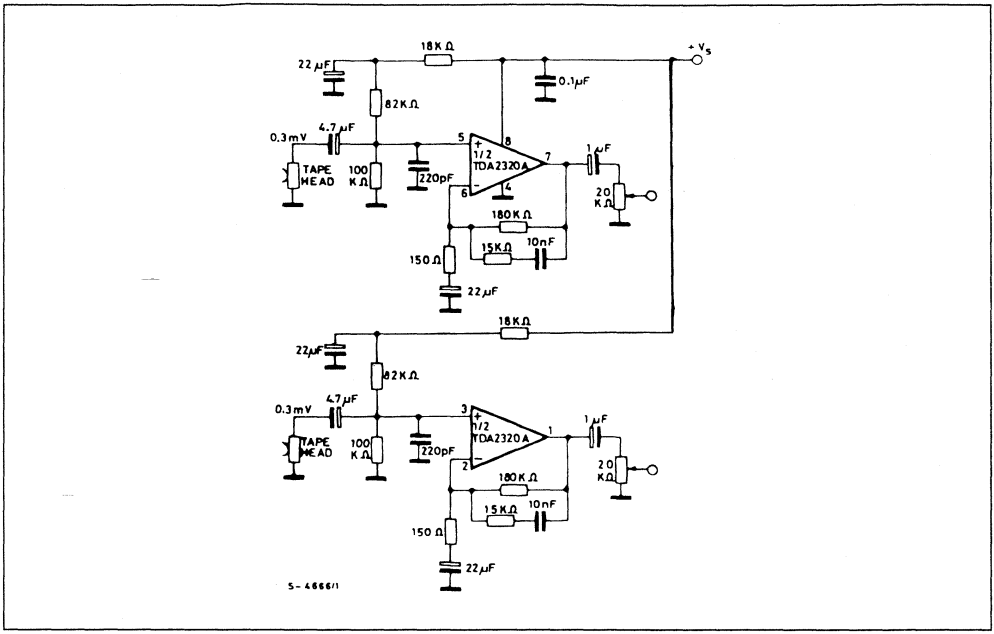
The TDA2320A is a monolithic integrated circuit a 8 lead minidip.

CONNECTION AND BLOCK DIAGRAM (top view)

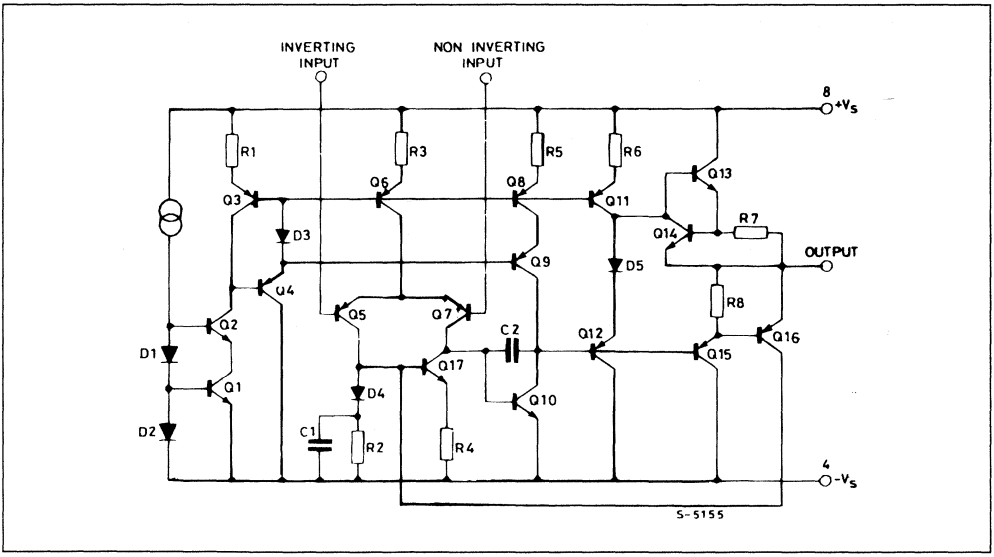




TYPICAL APPLICATION : Stereo Preamplifier for Cassette Players.



SCHEMATIC DIAGRAM (one section)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	36	V
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	400	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	200	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuits, V_s = 15 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage (*)			3		36	V
I_s	Supply Current (*)				0.8	2	mA
I_b	Input Bias Current				150	500	nA
V_{os}	Input Offset Voltage	R_g < 10 kΩ			1	5	mV
I_{os}	Input Offset Current				10	50	nA
G_v	Open Loop Voltage Gain	V_s = 15 V	f = 333 Hz		80		dB
			f = 1 kHz		70		
			f = 10 kHz		50		
		V_s = 4.5 V	f = 1 kHz		70		
V_o	Output Voltage Swing (*)	f = 1 kHz	V_s = 15 V		13		V_{pp}
		R_L = 600 Ω	V_s = 4.5 V		2.5		
B	Gain-bandwidth Product	f = 20 kHz		1.5	2.5		MHz
BW	Power Bandwidth (*)	V_o = 5 Vpp d = 1 %		40	70		kHz
SR	Slew Rate (*)			1	1.6		V/μs
d	Distortion (*)	V_o = 2 V	f = 1 kHz		0.03		%
		G_v = 20 dB	f = 10 kHz		0.08		
e_N	Total Input Noise Voltage (**)	Curve A	R_g = 50 Ω		1		μV
			R_g = 600 Ω		1.1	1.4	
			R_g = 5 kΩ		1.5		
		B = 22 Hz to 22 kHz	R_g = 50 Ω		1.3		μV
			R_g = 600 Ω		1.5		
			R_g = 5 kΩ		2		
		f = 1 kHz	R_g = 600 Ω		9		nV/√Hz
C_s	Channel Separation (**)	f = 1 kHz			100		dB
SVR	Supply Voltage (**) Rejection	f = 100 Hz			80		dB

(*) Test circuit of fig.1.
(**) Test circuit of fig.2.

TEST CIRCUITS

Figure 1.

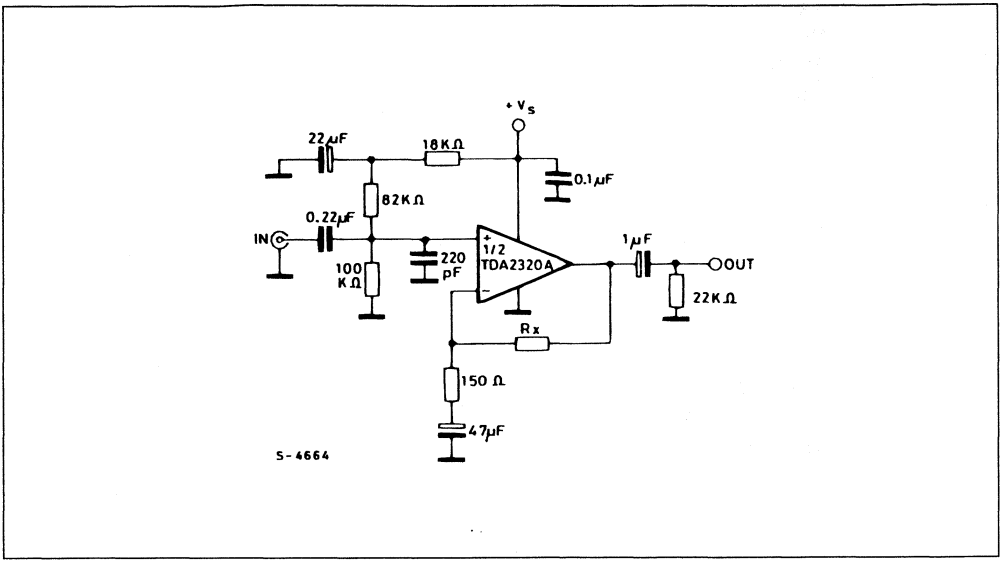


Figure 2.

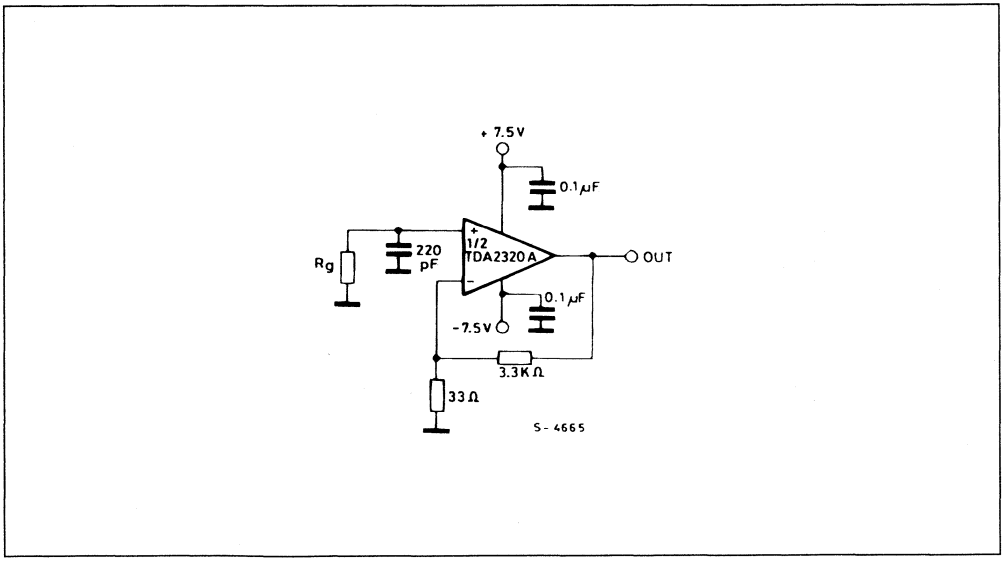


Figure 3 : Supply Current vs. Supply Voltage.

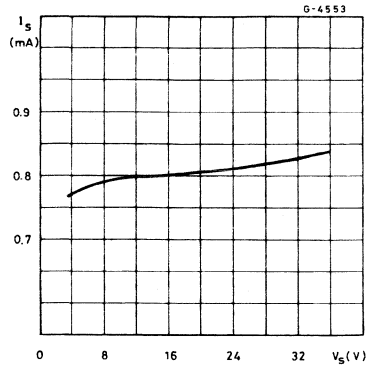


Figure 4 : Supply Current vs. Ambient Temperature.

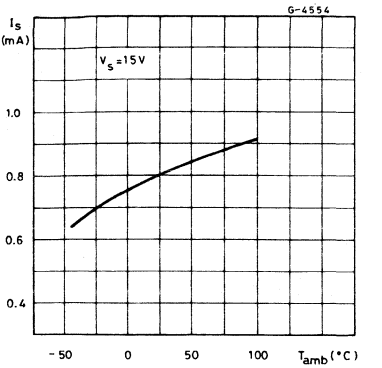


Figure 5 : Output Voltage Swing vs. Load Resistance.

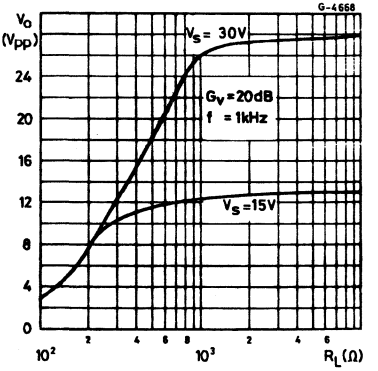


Figure 6 : Power Bandwidth.

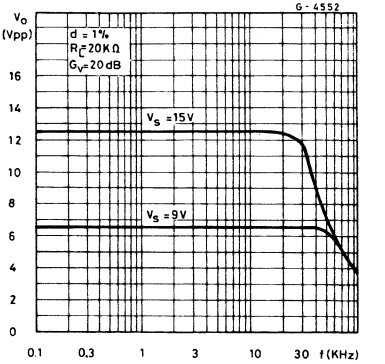


Figure 7 : Total Harmonic Distortion vs. Output Voltage.

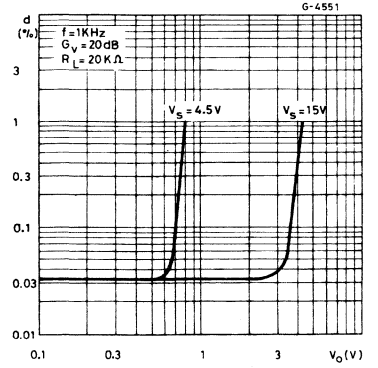


Figure 8 : Total Input Noise vs. Source Resistance.

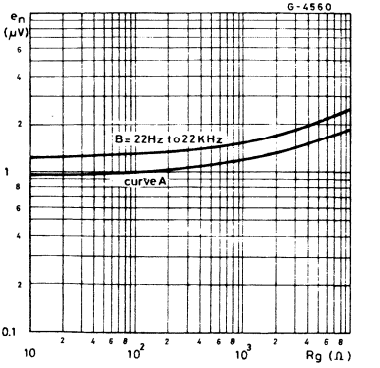


Figure 9 : Noise Density vs. Frequency.

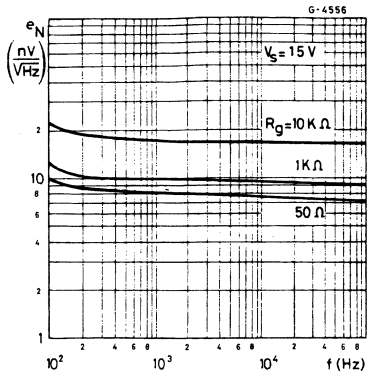


Figure 10 : RIAA Preamplifier Response (circuit of fig.12).

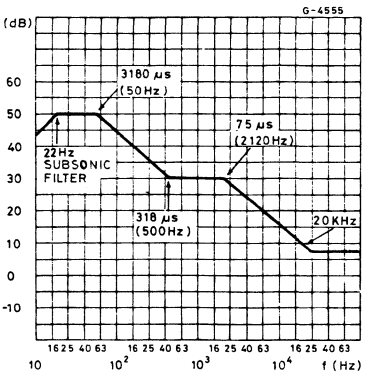
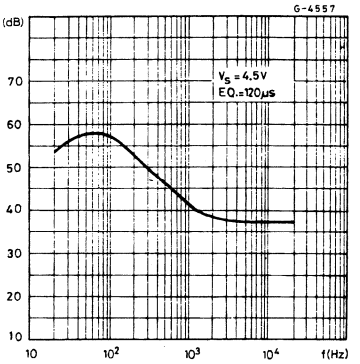


Figure 11 : Tape Preamplifier Frequency Response (circuit of fig.14).



APPLICATION INFORMATION

Figure 12 : Stereo RIAA Preamplifier.

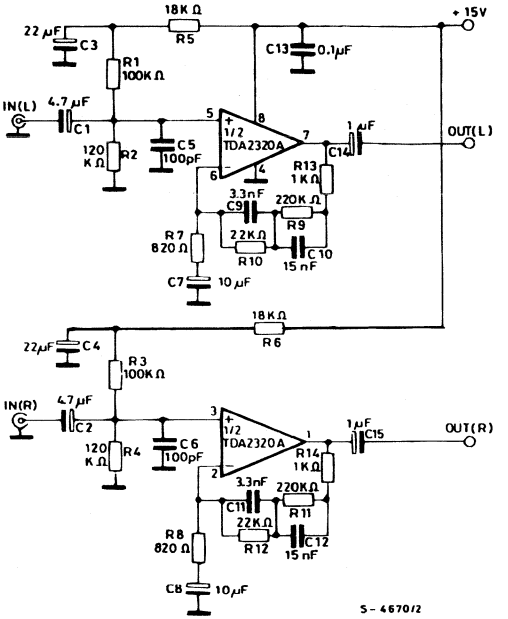


Figure 13 : P.C. Board and Components layout of the Circuit of fig.12.

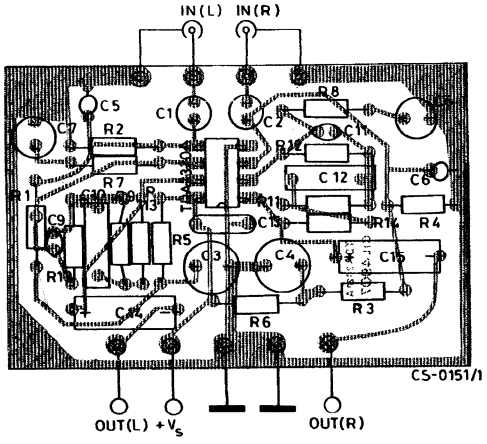


Figure 14 : Stereo Preamplifier for Walkman Cassette Players.

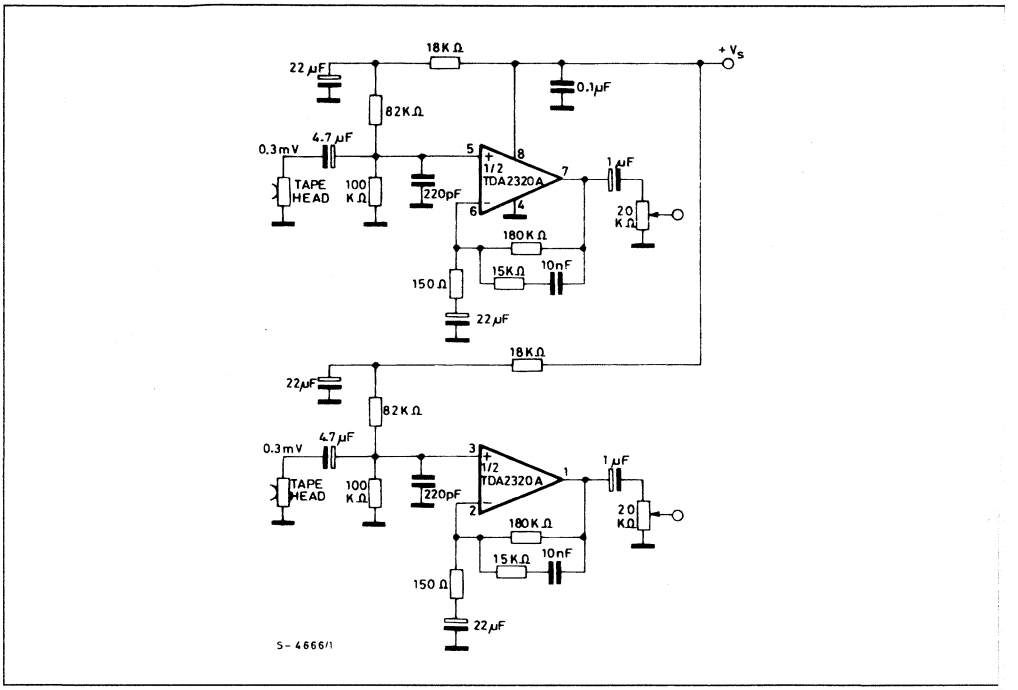


Figure 15 : Second Order 2 KHz Butterworth Crossover.

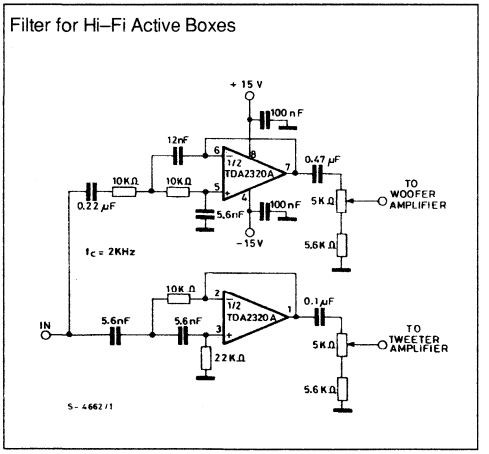


Figure 16 : Frequency Response (circuit of fig.15).

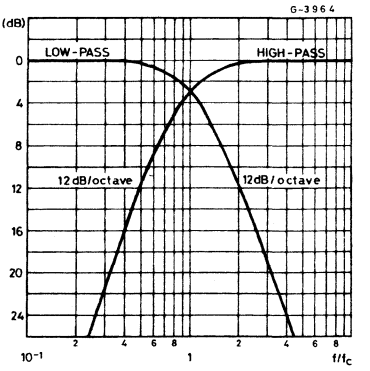


Figure 17 : Third Order 2.8 KHz Bessel Crossover.

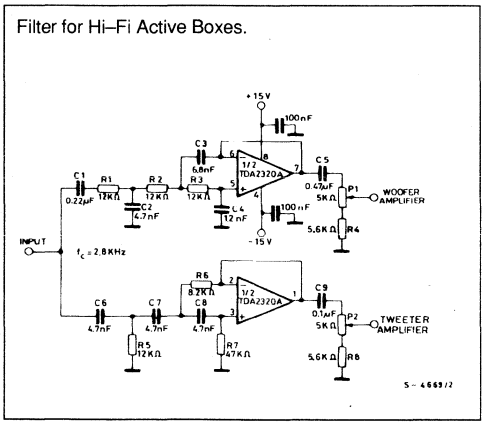


Figure 18 : Frequency Response (circuit of fig.16).

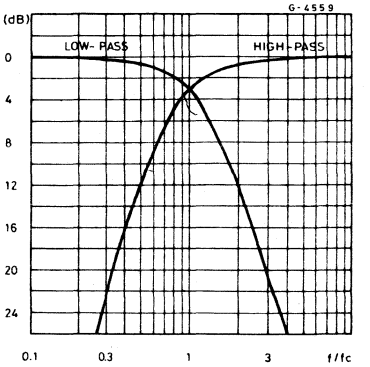
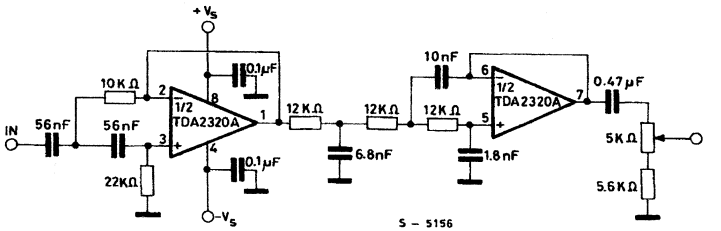
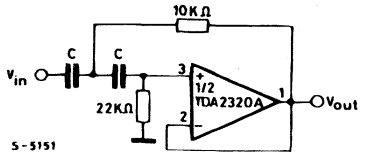


Figure 19 : 200 Hz to 2 KHz Active Bandpass Filter for Midrange Speakers.



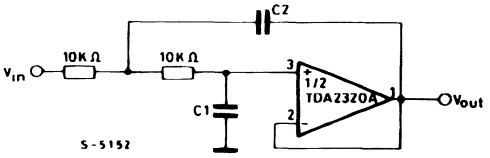
APPLICATION INFORMATION (continued)

Figure 20 : Subsonic Filter.



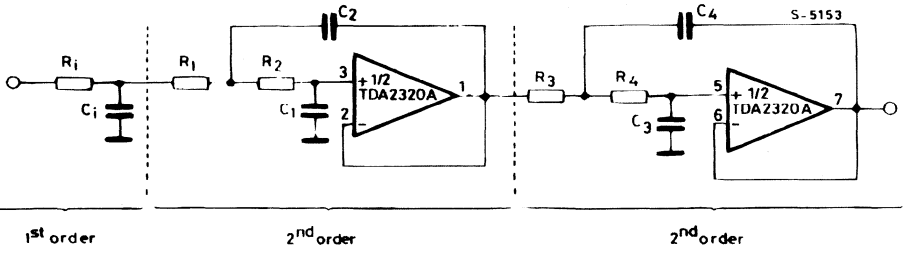
f_c (Hz)	C (μF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

Figure 21 : High–cut Filter.



f_c (kHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

Figure 22 : Fifth Order 3.4 KHz Low–pass Butterworth Filter.



For f_c = 3.4 KHz and R_i = R1 = R2 = R3 = R4 = 10 KΩ, we obtain :

$$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33 \text{ nF} \qquad C3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45 \text{ nF}$$

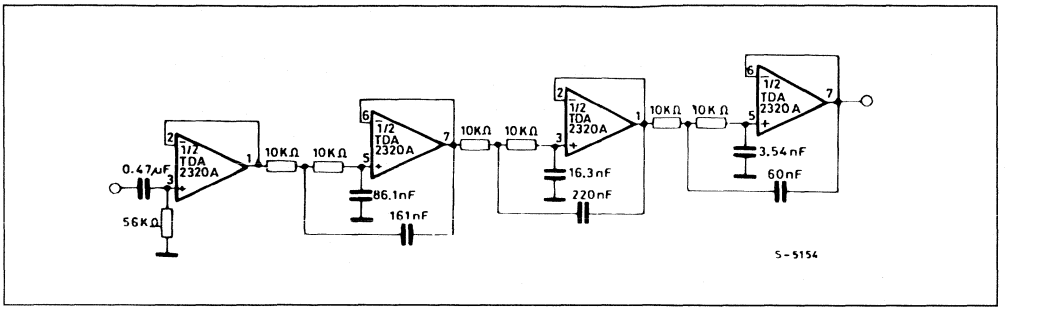
$$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97 \text{ nF} \qquad C4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2,\pi f_c} = 15.14 \text{ nF}$$

$$C2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20 \text{ nF}$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

APPLICATION INFORMATION (continued)

Figure 23 : Sixth–pole 355 Hz Low–pass Filter (chebychev type).



This is a 6-pole Chebychev type with ±0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ±0.25 dB ripple and does not exceed 1/2 dB at 0.9 fc.

Figure 24 : Three Band Tone Control.

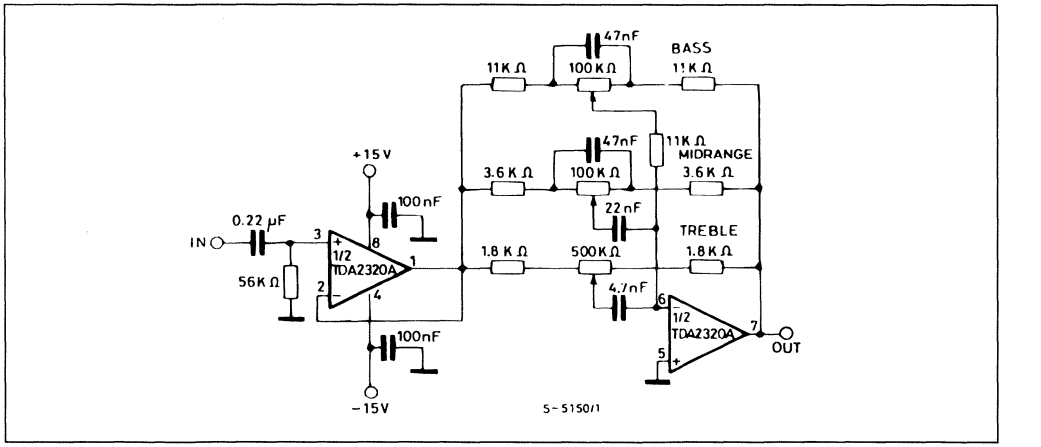
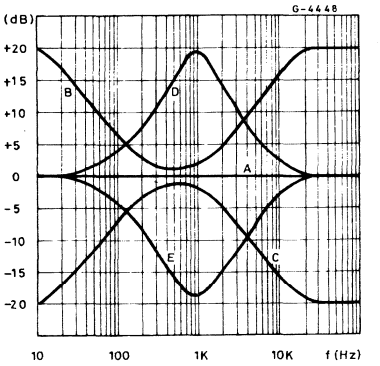


Figure 25 : Frequency Response of the Circuit of Fig.24.

A : all controls flat
B : bass & treble boost, mid flat
C : bass & treble cut, mid flat
D : mid boost, bass & treble flat
E : mid cut, bass & treble flat

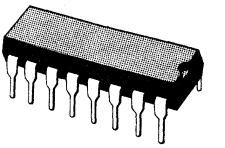


SGS-THOMSON MICROELECTRONICS

TDA3410

DUAL LOW NOISE TAPE PREAMPLIFIER WITH AUTOREVERSE

- VERY LOW NOISE
- HIGH GAIN
- LOW DISTORTION
- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE
- SVR = 120 dB
- LARGE OUTPUT VOLTAGE SWING
- TAPE AUTOREVERSE FACILITY
- SHORT-CIRCUIT PROTECTION



DIP-16
(Plastic 0.4)

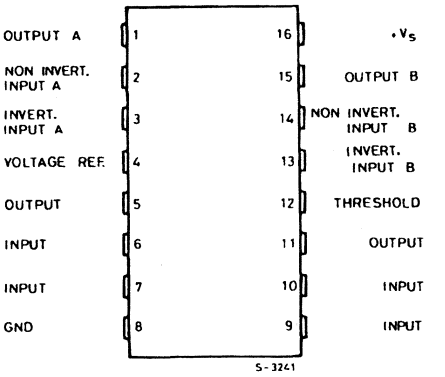
ORDER CODE : TDA3410

DESCRIPTION

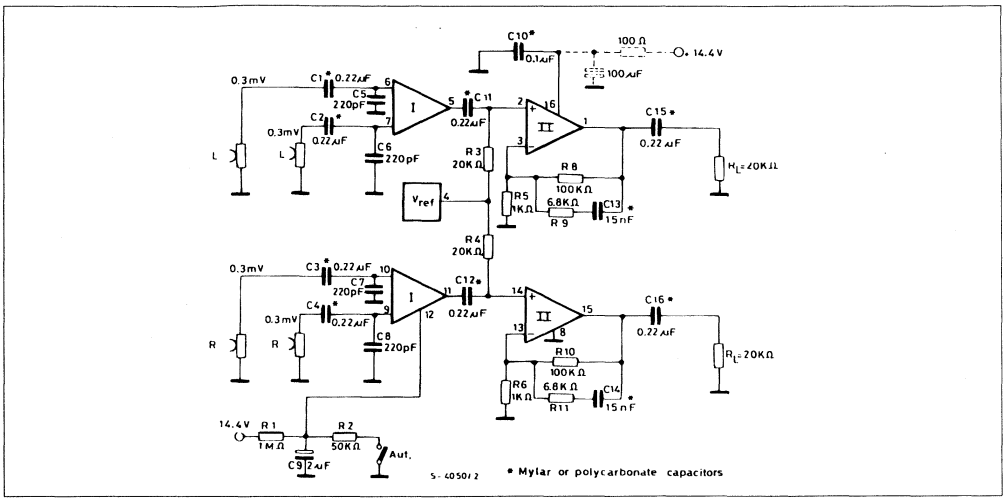
The TDA3410 is a dual preamplifier with tape autoreverse facility for the amplification of low level signals in applications requiring very low noise performance, as stereo cassette players. Each channel consists of two independent amplifiers. The first has a fixed gain of 30 dB while the second one is an operational amplifier optimized for high quality audio application.

The TDA3410 is a monolithic integrated circuit in a 16-lead dual in-line plastic package.

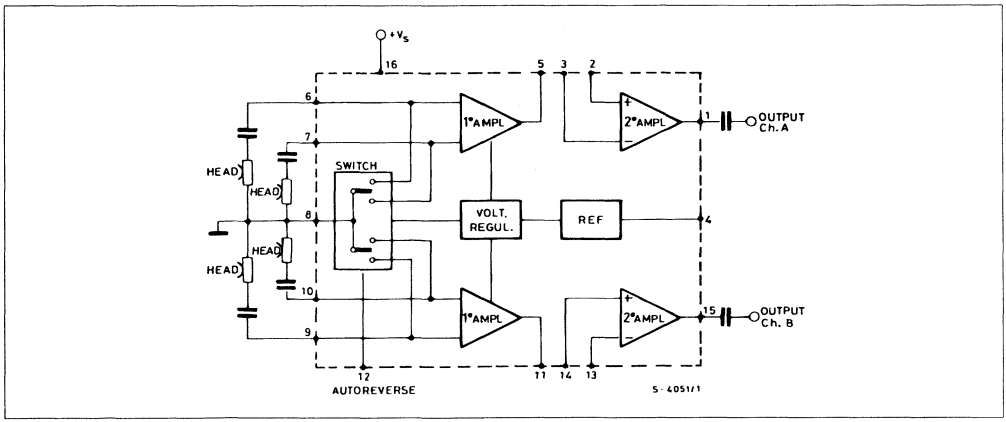
PIN CONNECTION (top view)



STEREO PREAMPLIFIER FOR AUTOREVERSE CASSETTE PLAYERS



BLOCK DIAGRAM



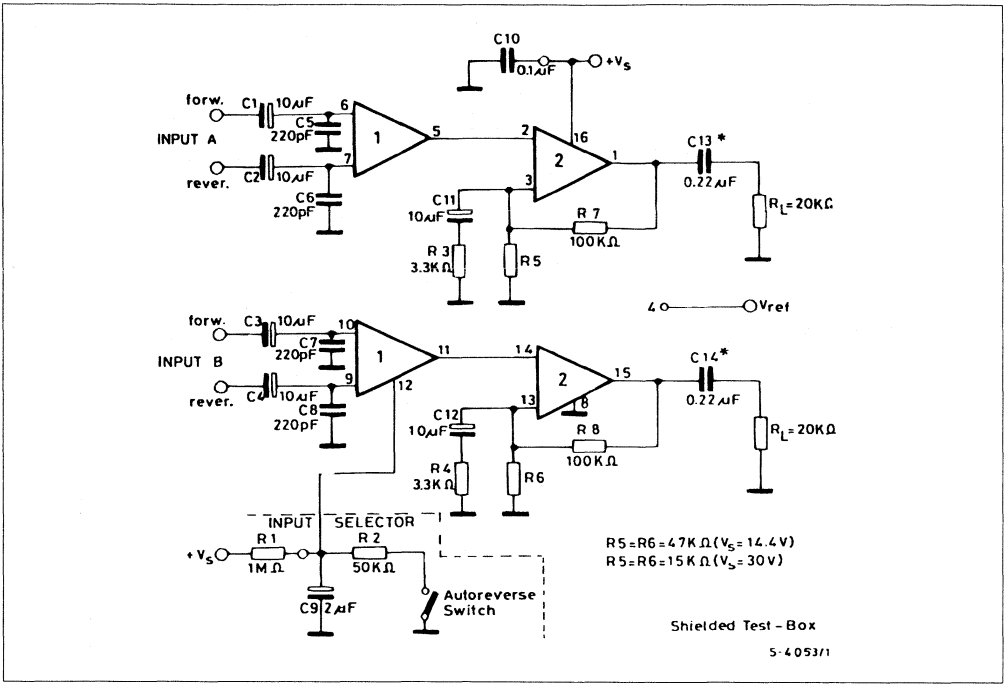
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	36	V
P_{tot}	Total Power Dissipation at T_{amb} = 60°C	600	mW
T_j, T_{stg}	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	150	°C/W

TEST CIRCUIT (Flat Gain - G_v = 60 dB)



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 14.4V, G_v = 60dB, refer to the test circuit, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_s	Supply Current	V_s = 8V to 30V		10		mA
I_o	Output Current (pins 1-15)	Source Sink V_s = 8V to 30V		10 1		mA mA
G_v	Closed Loop Gain	f = 20Hz to 20KHz		60		dB
R_i	Input Resistance	f = 1KHz	50	80		kΩ
R_o	Output Resistance (pins 1-15)	f = 1KHz		50		Ω
THD	Total Harmonic Distortion	V_o = 300mV f = 1KHz f = 10KHz		0.05 0.05		% %
V_o	Output Voltage Swing (pins 1-15)	Peak to Peak V_s = 14.4V V_s = 30V		12 28		V V
V_o	Output Voltage (pins 1-15)	d = 0.5% V_s = 14.4V f = 1KHz V_s = 30V		4 8		V_{rms} V_{rms}
e_n	Total Input Noise (°)	R_g = 50Ω R_g = 600Ω R_g = 5kΩ		0.25 0.4 1.3	 0.6 	µV µV µV
S/N	Signal to Noise Ratio (°)	V_{in} = 0.3mV R_g = 600Ω V_{in} = 1mV R_g = 0		57 73		dB dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CS	Channel Separation	f = 1KHz		60		dB
CT(°°°)	Cross-talk (differential input)	f = 1KHz		80		dB
SVR	Supply Voltage Rejection (°°)	f = 1KHz R_g = 600Ω		120		dB
SVR (°°)	Of Reference Voltage (pin 4)	f = 1KHz R_g = 600Ω		100		dB
V_{ref}	Reference Voltage (pin 4)			55		mV
R_{ref}	Ref. Voltage Output Resistance (pin 4)			100		Ω
$\frac{\Delta V_{ref}}{\Delta T}$	Voltage Temperature Coefficient			10		µV/°C

(°) The weighting filter used for the noise measurement has a curve A frequency response.
(°°) Referred to the input.
(°°°) Between a disabled input and an input ON.

ELECTRICAL CHARACTERISTICS (refer test circuit, V_s = 30V)

AMPLIFIER N° 1

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_v	Gain (pins 6 to 5)		29	30	30.5	dB
d	Distortion	V_o = 300mV f = 1KHz f = 10KHz		0.05 0.05		%
e_n	Total Input Noise (°)	R_g = 600Ω		0.4		µV
Z_o	Output Impedance (pin 5)	f = 1KHz		100		Ω
I_o	Output Current (pin 5)			1		mA
V_5	DC Output Voltage (pin 5)	V_s = 10V	1.3	2	2.7	V

AMPLIFIER N° 2

G_v	Open Loop Voltage Gain (pins 2 to 1)			100		dB
I_B	Input Bias Current			0.2		µA
V_{os}	Input Offset Voltage			2		mV
I_{os}	Input Offset Current			0.05		µA
BW	Small Signal Bandwidth	G_v = 30dB		150		KHz
e_n	Total Input Noise (°)	R_g = 600Ω		2		µV
R_i	Input Impedance	f = 1KHz (open loop)	150	500		kΩ

AUTOREVERSE

P_{in}	V_{12} < 2V	V_{12} > 4.5V
6 – 10	OFF	ON
7 – 9	ON	OFF

(°) The weighting filter used for the noise measurement has a curve A frequency response.

Figure 1 : Total Input Noise vs. Source Resistance (curve A).

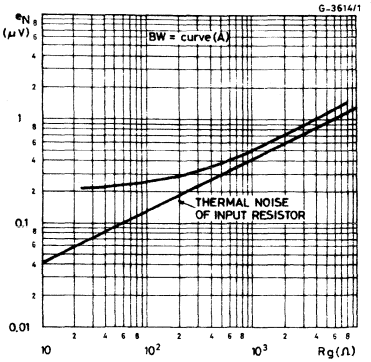


Figure 2 : Total Input Noise vs. Source Resistance (BW = 22 Hz to 22 KHz).

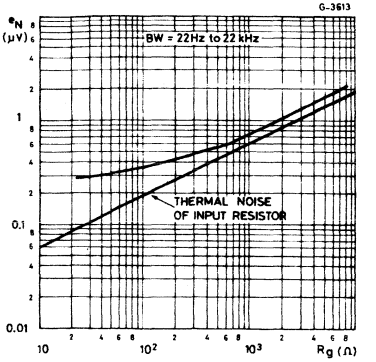


Figure 3 : Total Harmonic Distorsion vs. Output Voltage.

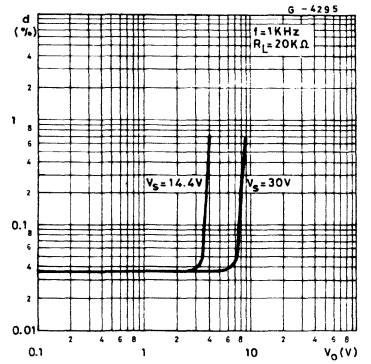


Figure 4 : Very Low Noise Stereo Preamplifier for Car Cassette Players (with Gap Loss Correction and autoreverse function).

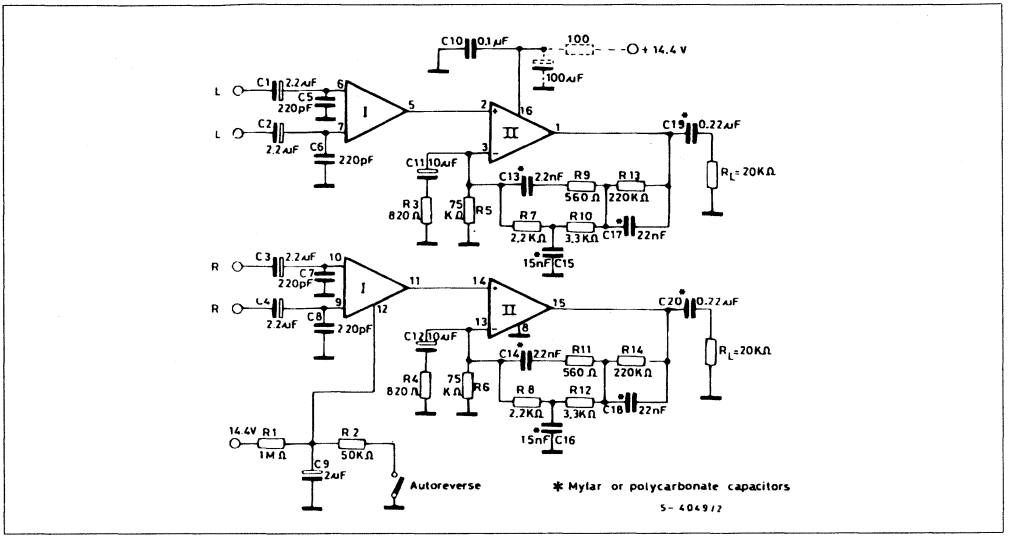


Figure 5 : Frequency Response.

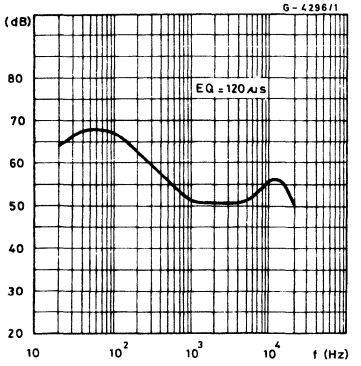


Figure 6 : P.C. Board and Component Lay-out for the Circuit of Figure 4.

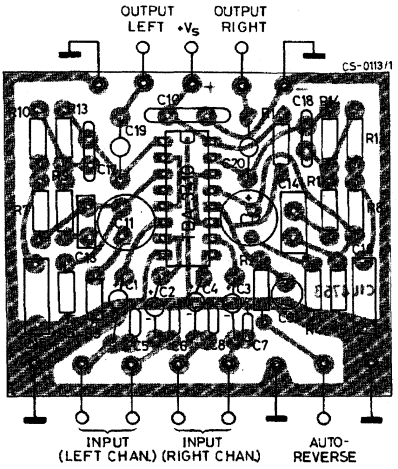


Figure 7 : Stereo Preamplifier for Car Cassette Players, with Low Value Capacitors (Autoreverse function).

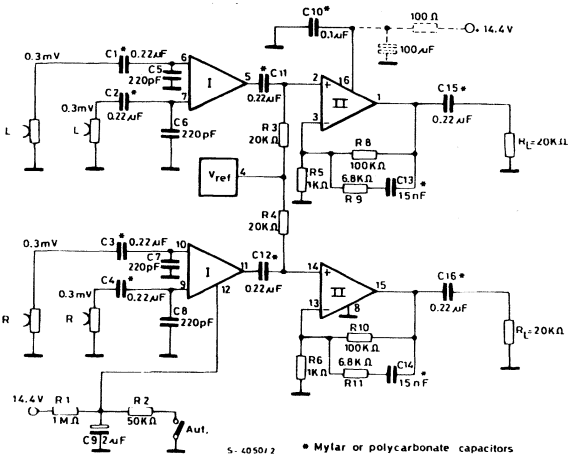
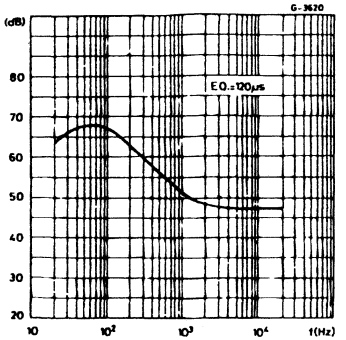
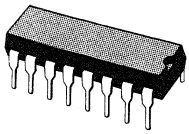


Figure 8 : Frequency Response.

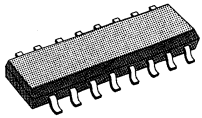


DUAL VERY LOW NOISE PREAMPLIFIER

- VERY LOW NOISE
- HIGH GAIN
- LOW DISTORTION
- SINGLE SUPPLY OPERATION
- LARGE OUTPUT VOLTAGE SWING
- SHORT-CIRCUIT PROTECTION



DIP-16
(Plastic 0.4)



SO-16J

ORDER CODES : TDA3420 (DIP-16)
TDA3420D (SO-16)

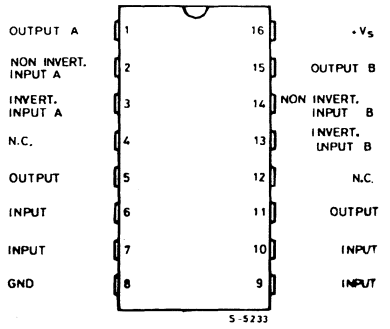
DESCRIPTION

The TDA3420 is a dual preamplifier for applications requiring very low noise performance, **as stereo cassette players** and quality audio systems. Each channel consists of two independent amplifiers.

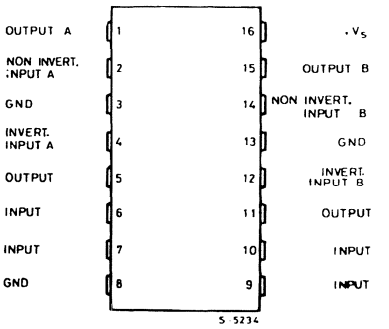
The first one has a fixed gain while the second one is an operational amplifier for audio application.

The TDA3420 is available in two packages : 16-lead dual in-line plastic and 16-lead micropackage.

PIN CONNECTIONS (top views)

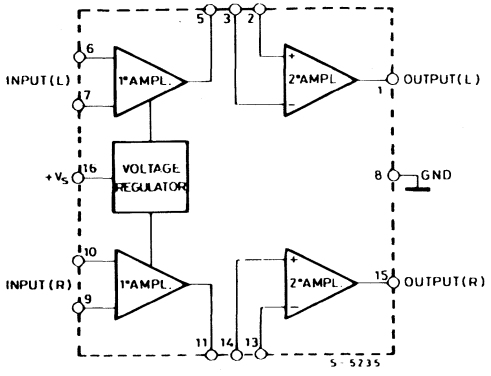


DIP



SO-16

BLOCK DIAGRAM (pin numbers refer to the DIP)



ABSOLUTE MAXIMUM RATINGS

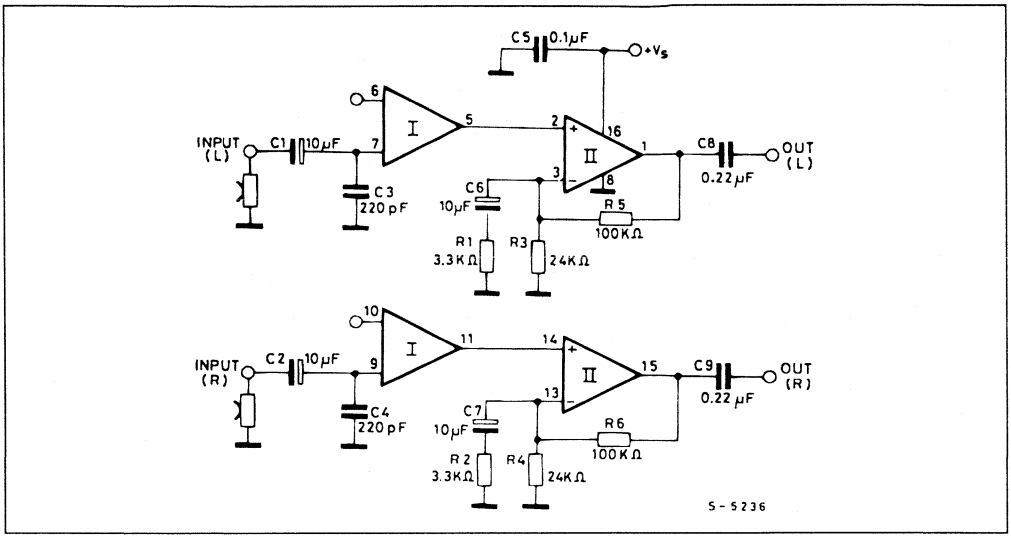
Symbol	Parameter	Value	Unit
V_s	Supply Voltage	20	V
P_{tot}	Total Power Dissipation at T_{amb} = 70°C DIP-16 SO-16	550 400	mW mW
T_j, T_{stg}	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

Symbol	Parameter		DIP-16	SO-16
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	150°C/W	200°C/W (*)

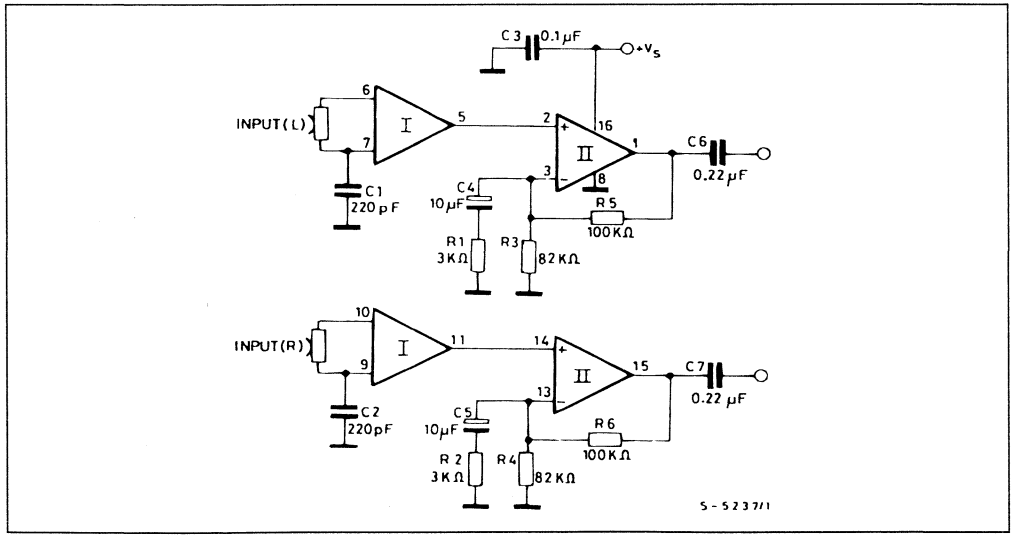
* The thermal resistance is measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

Figure 1 : Test Circuit.



Note : Pin numbers refer to DIP.

Figure 2 : Test Circuit without Input Capacitors.



Note : Pin numbers refer to the DIP.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 14.4V, G_v = 60dB refer to the test circuit of fig. 1, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_s	Supply Current	V_s = 8V to 20V			8		mA
I_o	Output Current	Source	V_s = 8V to 20V		10		mA
		Sink			1		mA
G_v	Gain	f = 1KHz			60		dB
R_i	Input Resistance			50	100		KΩ
R_o	Output Resistance				50		Ω
THD	Total Harmonic Distortion Without Noise	V_o = 300mV	f = 1KHz		0.05		%
			f = 10KHz		0.05		%
V_o	Peak to Peak Output Voltage	f = 40Hz to 15KHz			12		V
e_n	Total Input Noise (°)	R_s = 50Ω R_s = 600Ω R_s = 5kΩ			0.25 0.4 1.3	0.7	μV μV μV
S/N	Signal to Noise Ratio (°)	V_{in} = 0.3mV V_{in} = 1mV	R_s = 600Ω R_s = 0		57 73		dB
	(°°)	Vin = 0.3mV Vin = 1mV	Rs = 600Ω Rs = 0		55 71		dB
CS	Channel Separation	f = 1KHz			60		dB
SVR	Supply Voltage Rejection (°°°)	f = 1KHz	Rs = 600Ω		110		dB

AMPLIFIER N° 1

G_v	Gain (pin 6 to pin 5)			27.5	28.5	29	dB
d	Distortion	V_o = 300mV	f = 1KHz f = 10KHz		0.05 0.05		%
e_n	Total Input Noise (°)	R_s = 600Ω			0.4		μV
Z_o	Output Impedance (pin 5)	f = 1KHz			100		Ω
I_o	Output Current (pin 5)				1		mA
V5	DC Output Voltage (pin 5)	Test Circuit Fig. 2			2.8		V
		Test Circuit Fig. 1		1.0	1.5		

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AMPLIFIER N° 2						
G_v	Open Loop Voltage Gain			100		dB
I_B	Input Bias Current			0.2		µA
V_{os}	Input Offset Voltage			2		mV
I_{os}	Input Offset Current			50		nA
e_n	Total Input Noise(°)	R_s = 600Ω		2		µV
R_i	Input Impedance	f = 1KHz (open loop)	150	500		KΩ

(°) Weighting filter : curve A.
(°°) Weighting filter : Dolby CCIR/ARM.
(°°°) Referred to the input.

Figure 3 : Total Input Noise vs. Source Resistance (curve A).

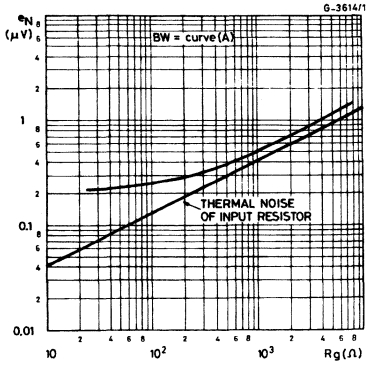


Figure 4 : Total Input Noise vs. Source Resistance (BW = 22 Hz to 22 KHz).

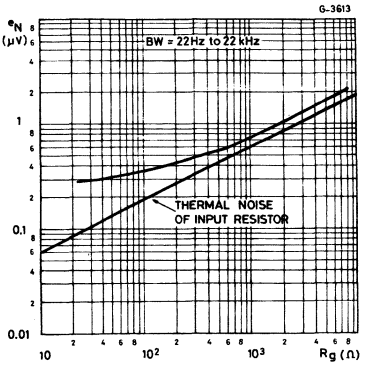


Figure 5 : Total Harmonic Distorsion vs. Output Voltage.

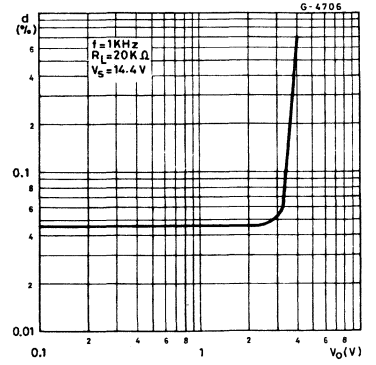


Figure 6 : Output Voltage vs. Frequency.

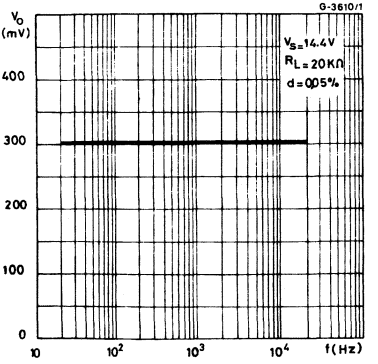


Figure 7 : Distortion vs. Input Level (test circuit of Figure 1).

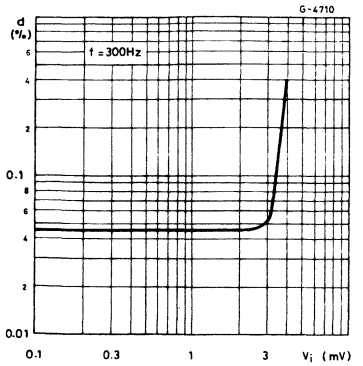
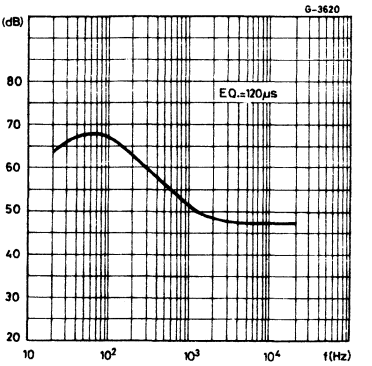
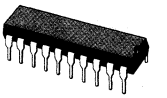


Figure 8 : Frequency Response of the Circuit of Figure 10.



LOW NOISE PREAMPLIFIER COMPRESSOR

- SINGLE SUPPLY OPERATION (10 to 30V)
- HIGH SUPPLY VOLTAGE REJECTION
- COMPRESSOR FACILITY
- VERY LOW NOISE AND DISTORTION
- HIGH COMMON MODE REJECTION
- SHORT CIRCUIT PROTECTION



DIP-20
(Plastic 0.4)

ORDER CODE : TDA7232

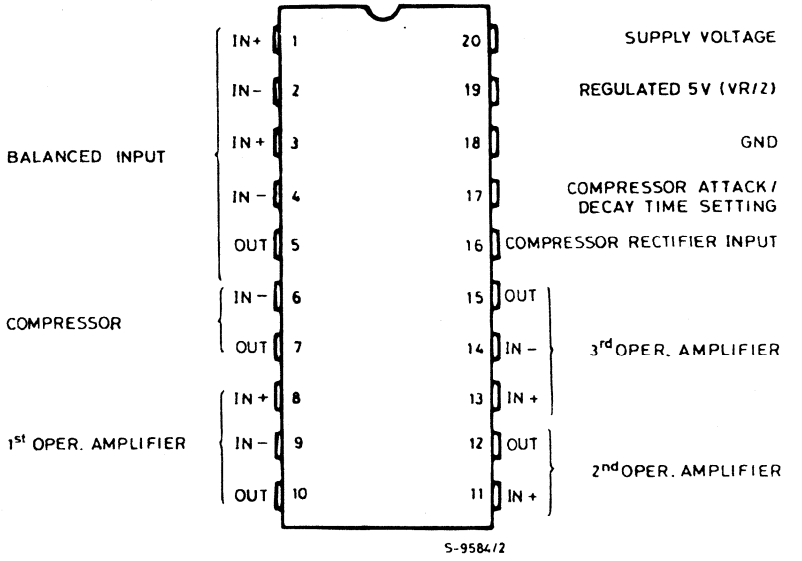
DESCRIPTION

The TDA 7232 is a preamplifier mainly intended for car-radio applications, requiring very low noise and distortion performance.

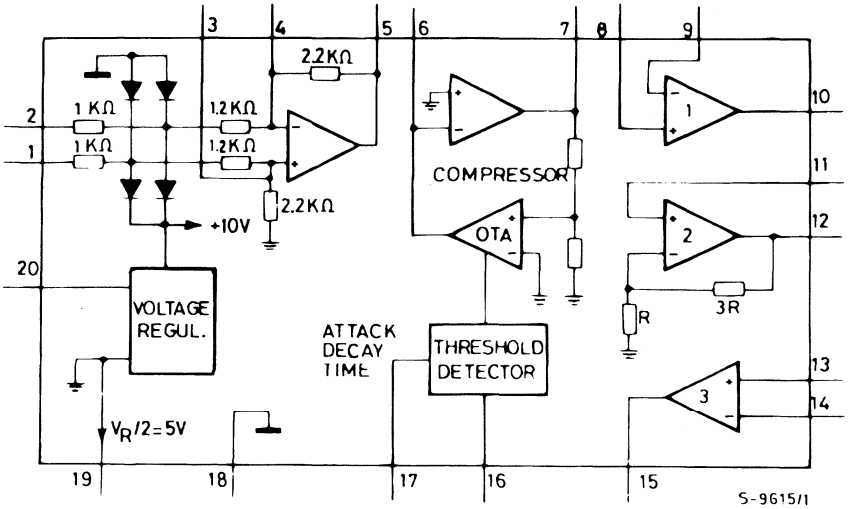
It consists of a unity gain differential input amplifier with a very high common mode rejection, a compressor wich avoids the output clipping and three multipurpose operational amplifiers.

A high stability voltage regulator is also included. The TDA 7232 is assembled in a 20 lead dual in line plastic package.

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Operating Supply Voltage	30	V
V_s	Peak Supply Voltage (for 50 ms)	40	V
V_i	Input Voltage	$\pm V_s$	
T_{op}	Operating Temperature	– 25 to 85	°C
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1	W

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, V_s = 14.4 V, G_v = 30 dB, refer to test circuit amplifier fig. 1)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage			10		30	V
I_s	Supply Current				10	16	mA
G_v	Closed Loop Gain	Pin 1–2 to Pin 15		29	30	31	dB
d	Total Harmonic Distortion	f = 1 KHz out of Compression V_o = 2 V_{RMS}			0.03	0.12	%
		in compression V_i = 0.7 V_{RMS}			0.15	0.5	%
V_o	Output Volt. Swing			7.5	8.4		V
e_N	Total Output Noise		B = 22 Hz to 22 KHz		160		μV
		R_g = 50 Ω	Curve A		120		μV
SVR	Supply Volt. Rejection (*)	R_g = 50 Ω V_R = 1 V_{RMS}	f = 100 Hz	90	110		dB

INPUT DIFFERENTIAL AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OS}	Input Offset Voltage			1	7	mV
G_v	Voltage Gain	f = 20 Hz to 20 KHz	0.98	1	1.02	V/V
e_N	Total Input Noise Voltage	R_g = 50 Ω ; B = 22 Hz to 22 KHz		1.5		μV
		R_g = 50 Ω ; Curve A		1.1		μV
d	Distortion	R_L = 2 KΩ V_o = 1 V_{RMS} f = 1 KHz		0.01		%
V_o	Output Swing	R_L = 2 KΩ	7.5	8.4		V_{pp}
SR	Slew Rate			1		V/μS
CMR	Common Mode Reject.	f = 20 Hz to 20 KHz	36	50		dB

COMPRESSOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_b	Input Bias Current			60	300	nA
V_{os}	Input Offset Voltage	$R_g \leq$ 10 KΩ out of Compression		1	3.5	mV
V_{os}	Output Offset Voltage	in Compression $V_{pin.17}$ = 0.7 V			350	mV
e_N	Total Input Noise Voltage	R_g = 50 Ω ; B = 22 Hz to 22 KHz		1.8		μV
		R_g = 50 Ω ; Curve A		1.3		μV
d	Distortion	R_L = 2 KΩ V_o = 1 V_{RMS} f = 1 KHz G_v = 20 dB		0.01		%
SVR	Supply Voltage Rejection	V_R = 1 V, f = 100 Hz, R_g = 50 Ω	86			dB

(*) Referred to the input.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	DC Output Voltage Swing	R_L = 2 KΩ	7.5	8.4		V
SR	Slew Rate			0.7		V/μS

1st AND 3rd OPERATION AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_b	Input Bias Current			60	300	nA
I_{os}	Input Offset Current			20	50	nA
V_{os}	Input Offset Voltage	$R_g \leq$ 10 KΩ		1	3.5	mV
CMR	Common Mode Rejection		86			dB
SVR	Supply Voltage Rejection	V_R = 1 V, f = 100 Hz, R_g = 50 Ω	86			dB
e_N	Total Input Noise Voltage	R_g = 50 Ω ; B = 22 Hz to 22 KHz		1.4		μV
		R_g = 50 Ω ; Curve A		1.1		μV
V_o	Output Voltage Swing	R_L = 2 KΩ	7.5	8.4		V_{pp}
d	Total Harmonic Distortion	R_L = 2 KΩ V_o = 1 V_{RMS} f = 1 KHz G_v = 20 dB		0.01		%
G_v	Open Loop Gain	R_L = 2 KΩ	86	100		dB
SR	Slew Rate	R_L = 2 KΩ		1		V/μS

2nd OPERATIONAL AMPLIFIER (G_v = 12 dB internally set)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{os}	Output Offset Voltage			4	15	mV
SVR	Supply Voltage Rejection	V_R = 1 V f = 100 Hz	86			dB
e_N	Total Input Noise Voltage	R_g = 50 Ω ; B = 22 Hz to 22 KHz		2.2		μV
		R_g = 50 Ω ; Curve A		1.4		μV
V_o	DC Output Voltage Swing	R_L = 2 KΩ	7.5	8.4		V
d	Total Harmonic Distortion	R_L = 2 KΩ, f = 1 KHz V_o = 1 V_{RMS}		0.01		%
G_v	Voltage Gain	f = 20 Hz to 20 KHz	11.5	12	12.5	dB
SR	Slew Rate	R_L = 2 KΩ		1		V/μs

VOLTAGE REGULATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	Pin 19 $I_{sink, source}$ from 0 to 12 mA	4.6	5	5.4	V
I_o	Output Max. Current	I_{source}		12		mA
		I_{sink}		12		mA

Figure 1 : Test Circuit.

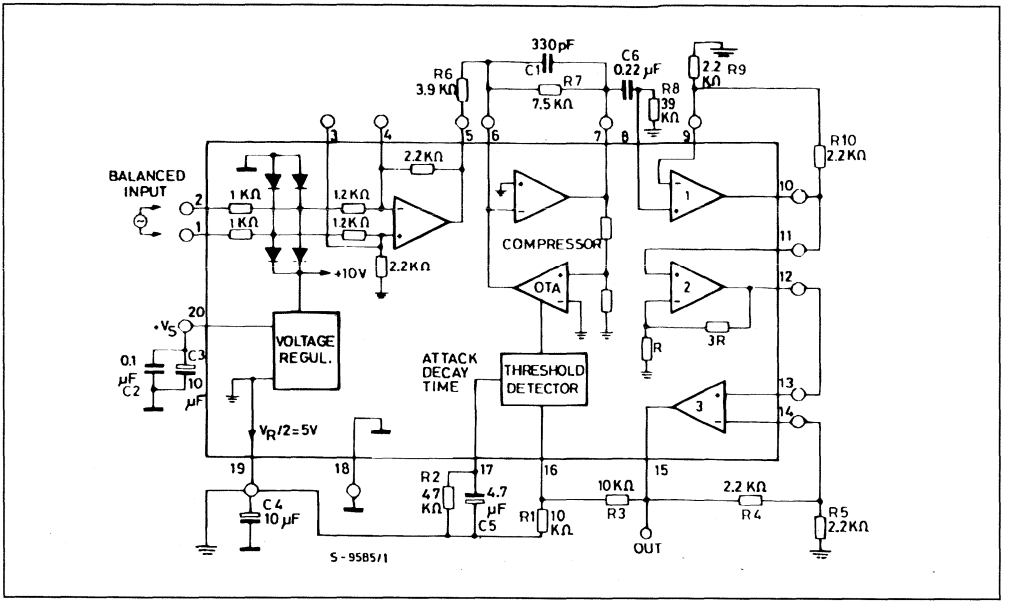


Figure 2 : P.C. Board and Components Layout of the Test Circuit of Fig. 1 (1 : 1 scale).

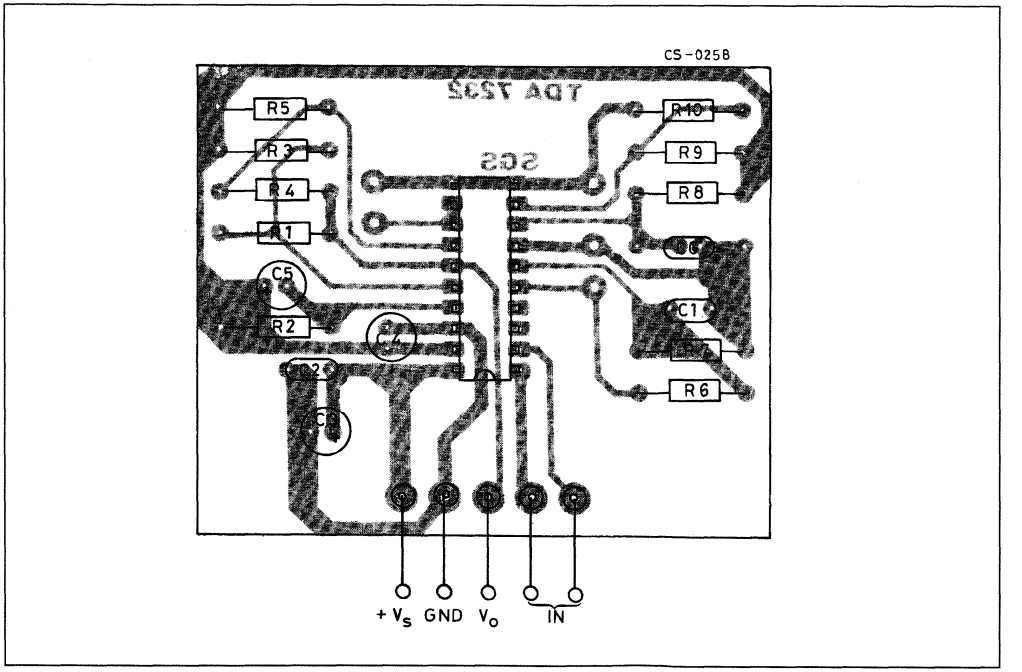


Figure 3 : Supply Current vs. Supply Voltage (complete test circuit).

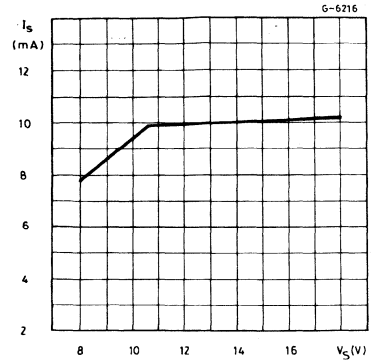


Figure 4 : Compression Characteristics.

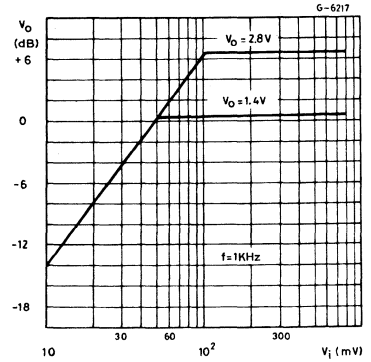


Figure 5 : Distortion vs. Frequency (complete test circuit).

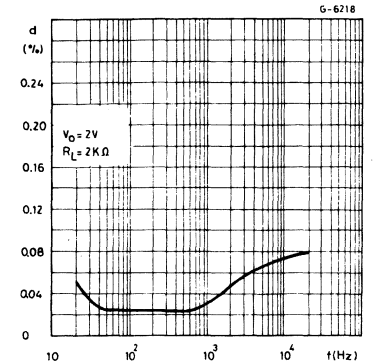


Figure 6 : Distortion vs. Input Signal Level (complete test circuit).

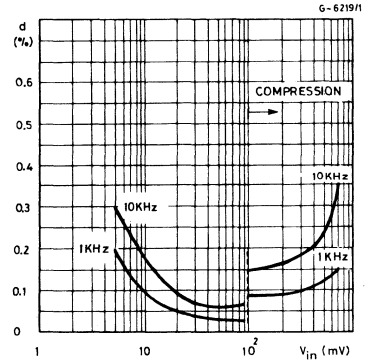


Figure 7 : Supply Voltage Rejection vs. Frequency (complete test circuit).

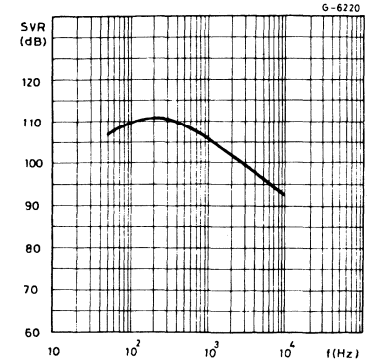


Figure 8 : Distortion vs. Output Voltage (input differ. amplifier).

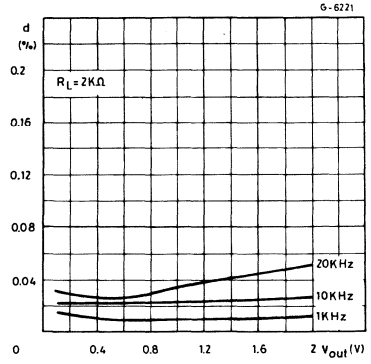


Figure 9 : Distortion vs. Frequency (input differ. amplifier).

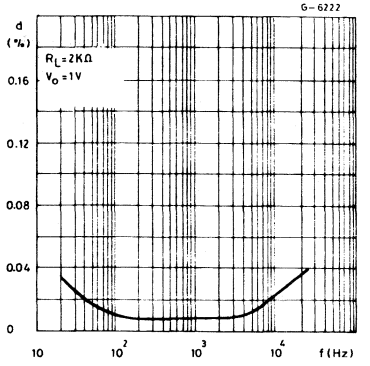


Figure 10 : Distortion vs. Output Voltage (compressor).

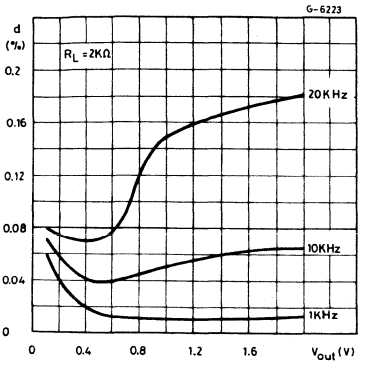


Figure 11 : Distortion vs. Frequency (compressor).

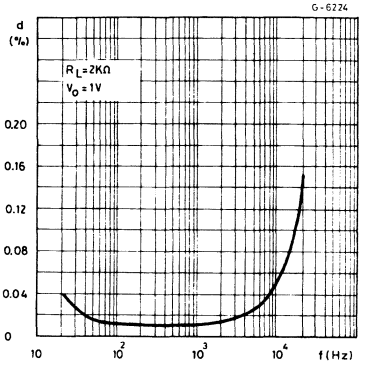


Figure 12 : Distortion vs. Output Voltage (op. amp. 1 & 3).

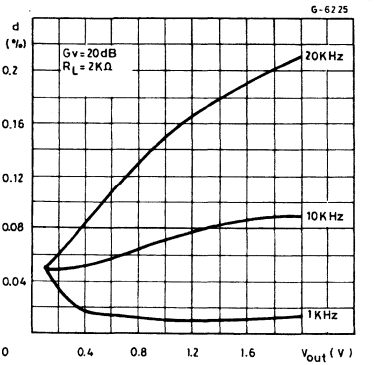


Figure 13 : Distortion vs. Frequency (op. amp. 1 & 3).

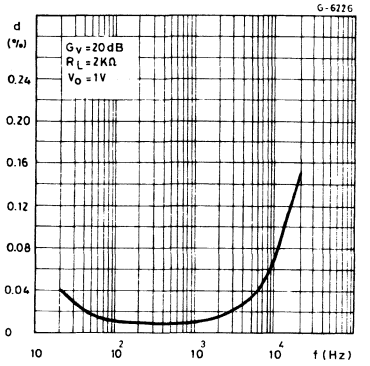


Figure 14 : Open Loop Frequency and Phase Response (op. amp. 1 & 3).

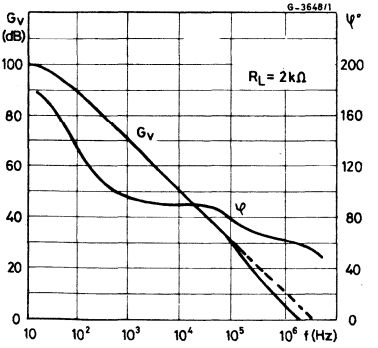


Figure 15 : Distortion vs. Output Voltage (op. amp. 2).

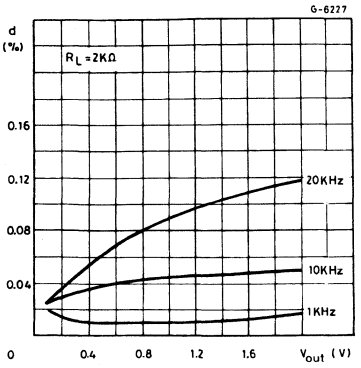
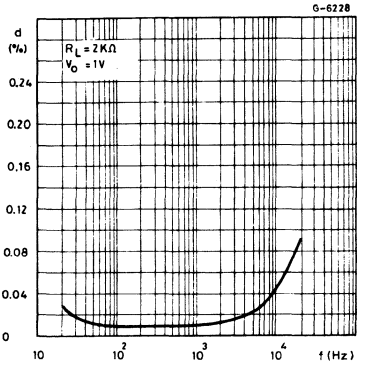


Figure 16 : Distortion vs. Frequency (op. amp. 2).



APPLICATION INFORMATION

The devices TDA7232 and TDA7260 realize with four external POWER MOS an exclusive audio system for car radio, thanks to their unique feature as:

- 25 W output power (d = 0.3 %) without heatsink, thanks to the extra-high efficiency (85 % typ. at rated output power) of the power stage, which operates in class "D" (pulse width modulation).
- In-car frequency response compensation, thanks to the availability of several operational amplifiers for the necessary equalization.
- High-quality sound at all listening levels, thanks to an appropriate compressor circuit that avoids clipping in the system.
- Low distortion, low noise, fully protected operation of the whole system.

Figure 17 : Suggested Application Using the TDA7260 Audio PWM Amplifier.

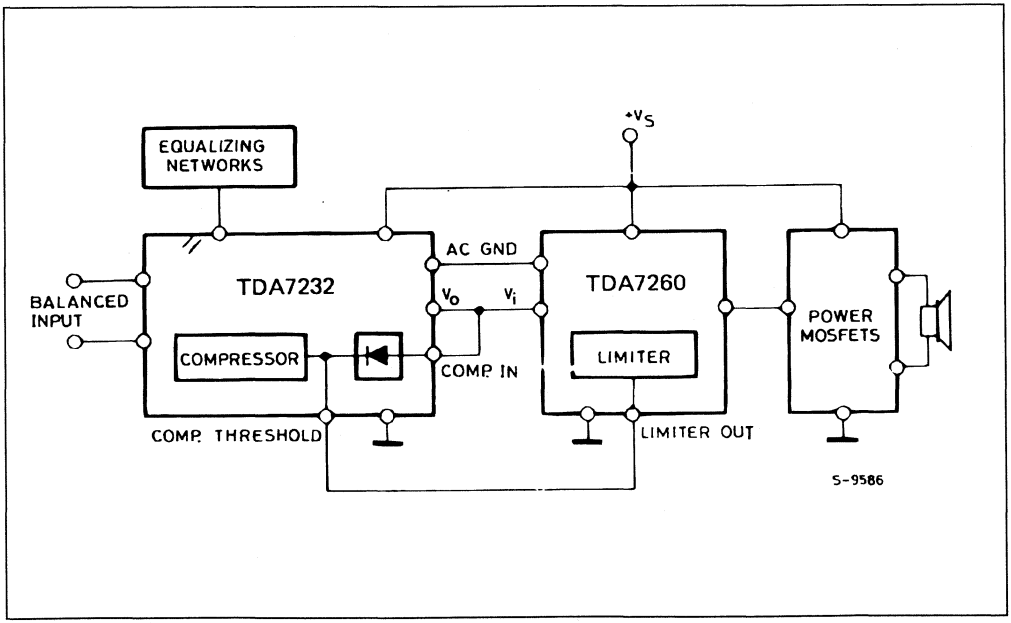


Figure 18 : 25 W Application Circuit Using the TDA7260 Audio PWM.

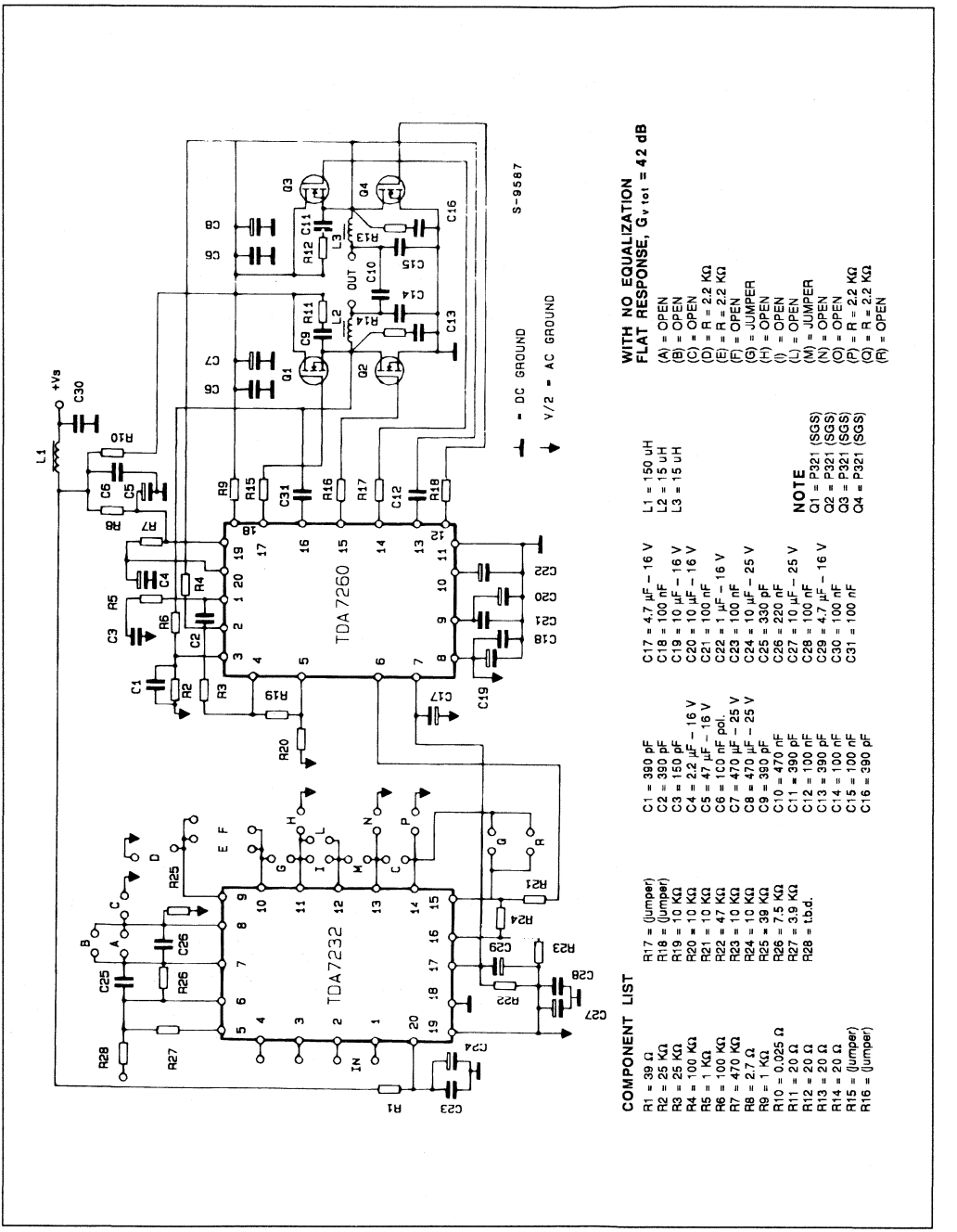


Figure 19 : P.C. Board and Components Layout for the Circuit of Fig. 18 (1 : 1 scale).

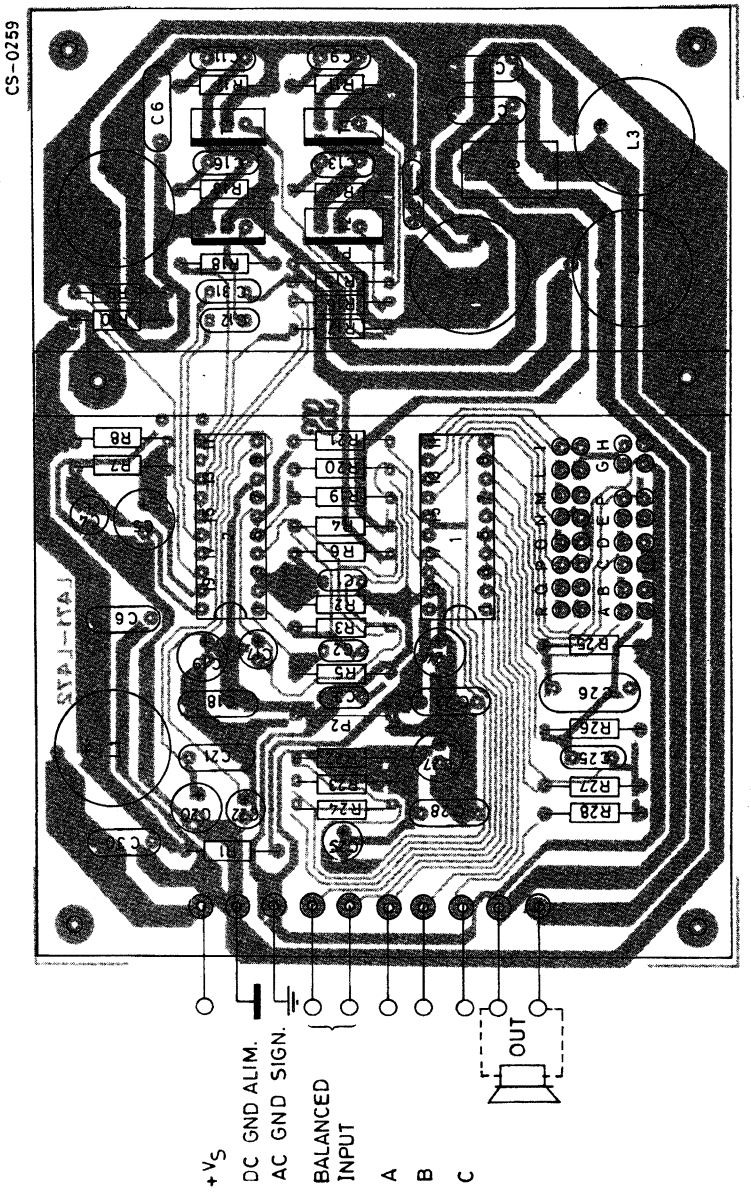


Figure 20 : Five Bands Equalizer with Compression Indicator.

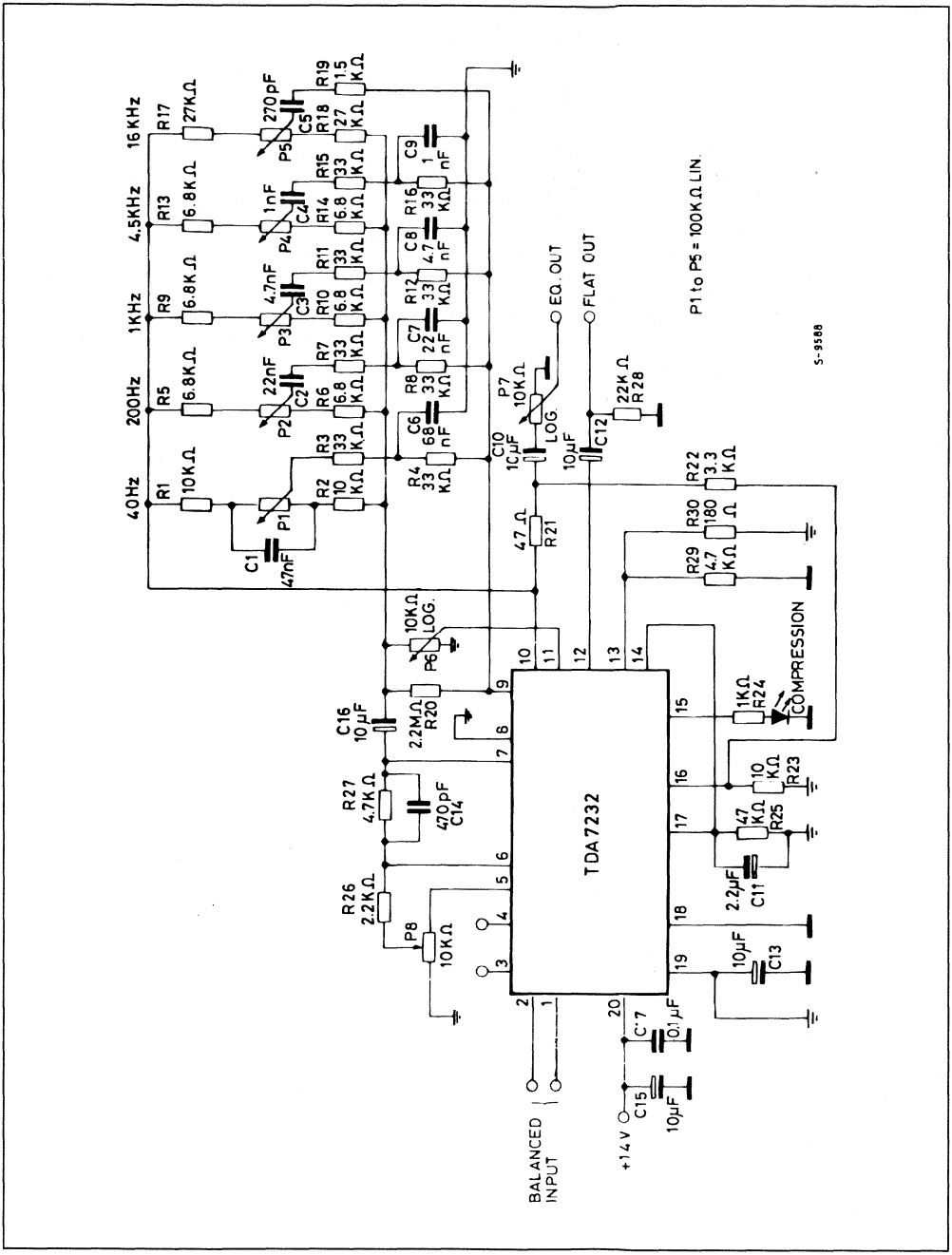


Figure 21 : P.C. and Components Layout for the Circuit of Fig. 20 (1 : 1 scale).

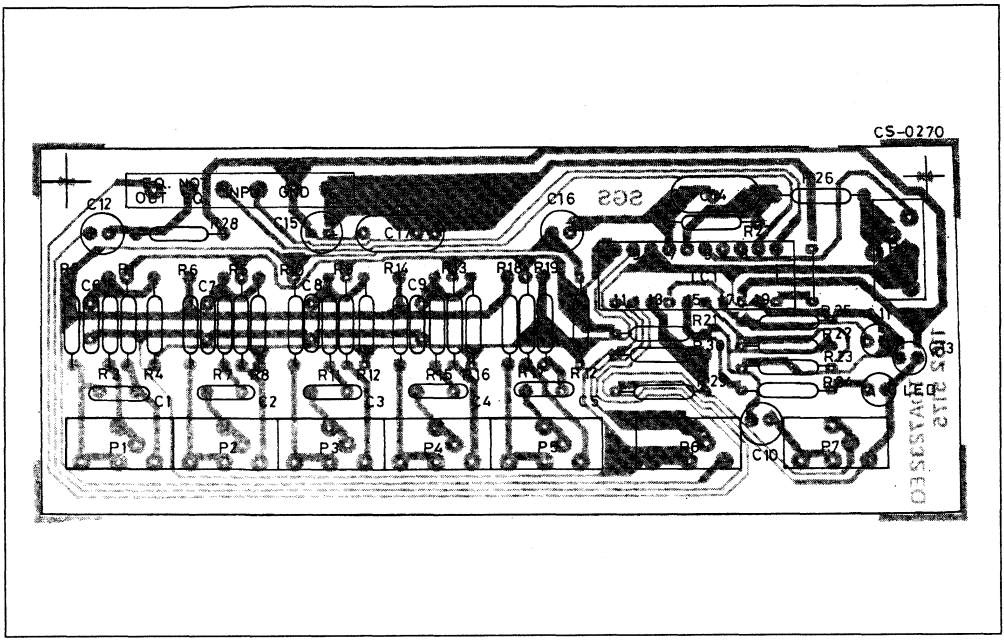
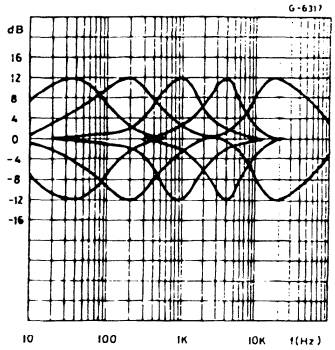
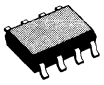


Figure 22 : Frequency Response of the five Bands Equalizer Circuit.

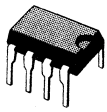


STEREO LOW VOLTAGE CASSETTE PREAMPLIFIER

- LOW ON/OFF POP NOISE
- LOW OPERATING VOLTAGE
- VERY LOW DISTORTION



SO – 8J



MINIDIP
(Plastic)

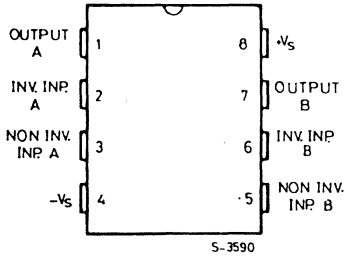
ORDER CODES : TDA7282 (Minidip)
TDA7282D (SO – 8)

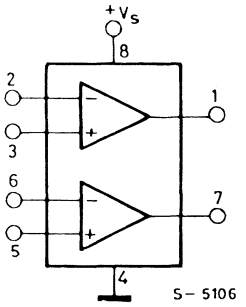
DESCRIPTION

The TDA7282 is a monolithic integrated circuit intended for stereo cassette players.

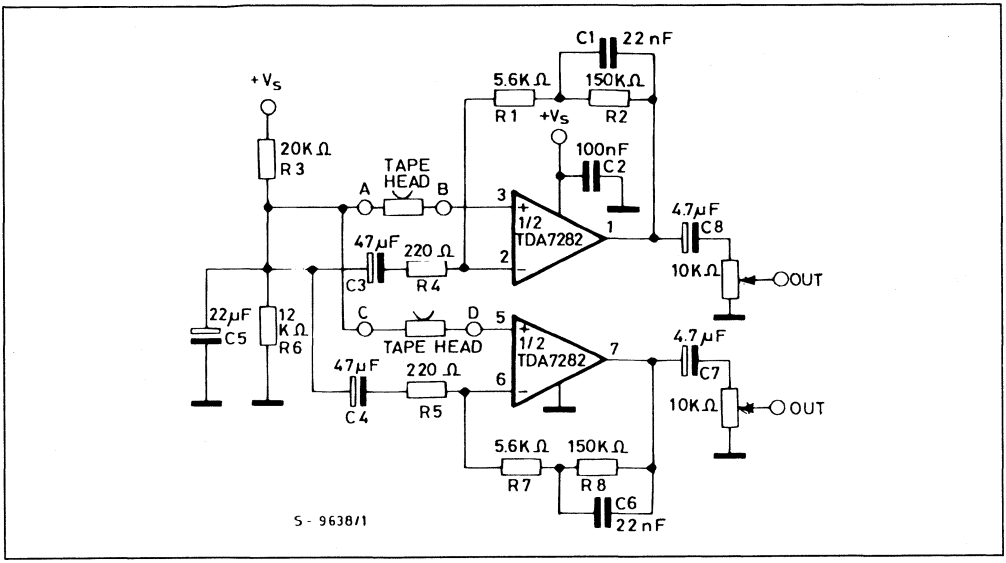
The TDA7282 is assembled in 8 leads plastic minidip.

CONNECTION AND BLOCK DIAGRAM

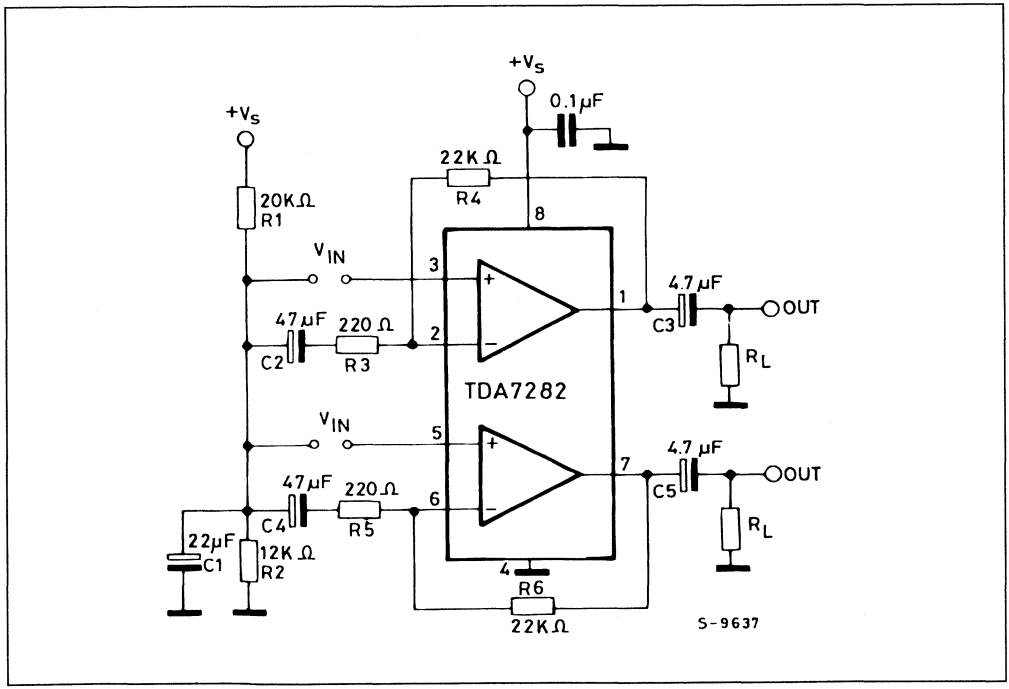




STEREO PREAMPLIFIER FOR CASSETTE PLAYERS



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	10	V
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	400	mW

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	200	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 3 V, T_{amb} = 25 °C, f = 1 kHz, G_v = 40 dB, R_L = 10 kΩ, R_s = 600 Ω unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		1.8		9	V
I_d	Supply Current			1.5	3	mA
I_b	Input Bias Current			280	500	nA
I_{os}	Input Offset Current			20		nA
V_{os}	Input Offset Voltage			0.5		mV
$V_{o\ DC}$	Quiescent Voltage			1.1		V
V_o	Output Voltage	THD = 1 %	550	650		mV
THD	Total Harmonic Distortion f = 100 Hz f = 1 kHz f = 10 kHz	 V_o = 300 mV		 0.08 0.07 0.1	 0.5	 % % %
G_v	Open Loop Volage Gain	f = 1 kHz	68	80		dB
G_v	Closed Loop Gain			40		dB
	Channel Balance			0.5		dB
e_N	Total Input Noise Voltage	B_W = 22 kHz to 22 kHz		1.5		μV
C_S	Channel Separation	f = 1 kHz Vo = 30 mV		65		dB
SVR	Supply Volage Rejection	f = 100 Hz	36	45		dB
R_{IN}	Input Resistance			100		kΩ
R_o	Output Resistance			15		Ω

APPLICATION INFORMATION

Figure 1 : Stereo Preamplifier for Cassette Players.

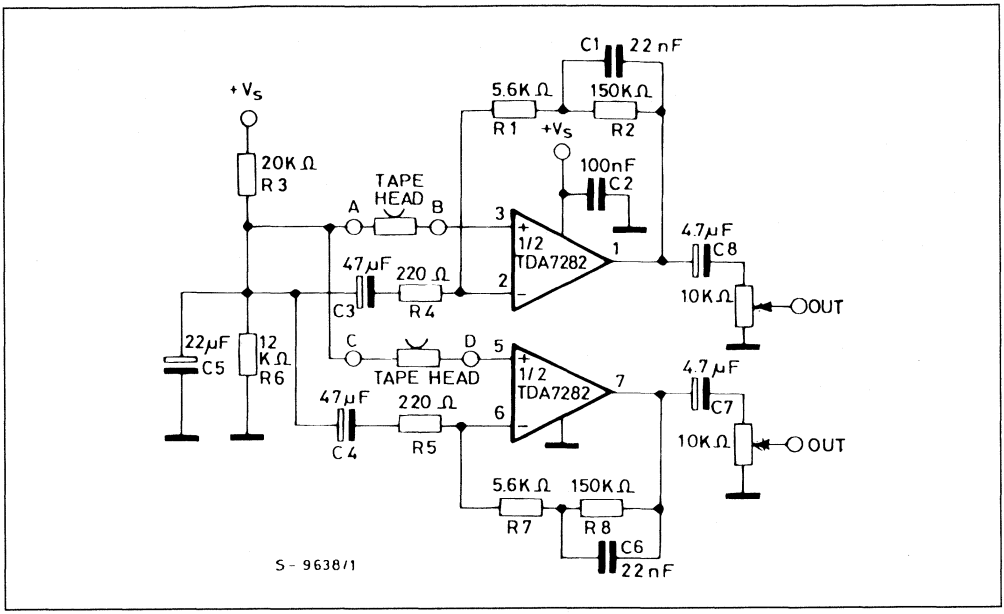


Figure 2 : P. C. and Components layout of the Circuit of Fig. 1 (1 : 1 scale).

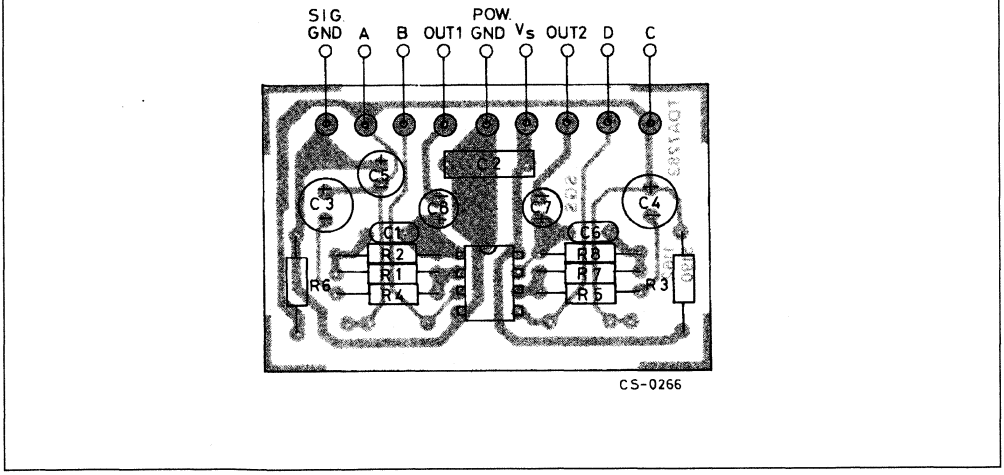


Figure 3 : Quiescent Current vs Supply voltage.

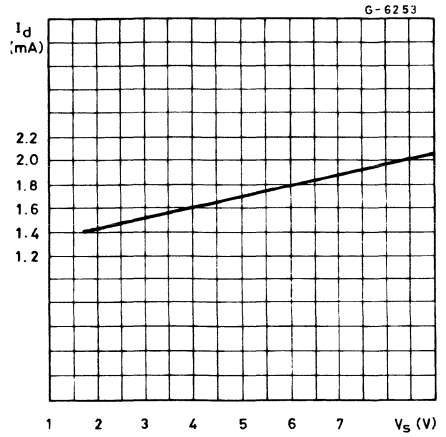


Figure 4 : DC Output Voltage vs. Supply Voltage.

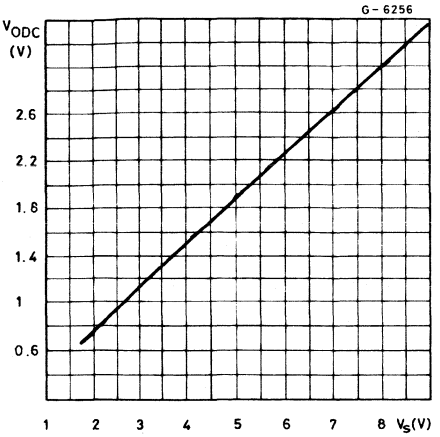


Figure 5 : Input bias Current vs Supply voltage.

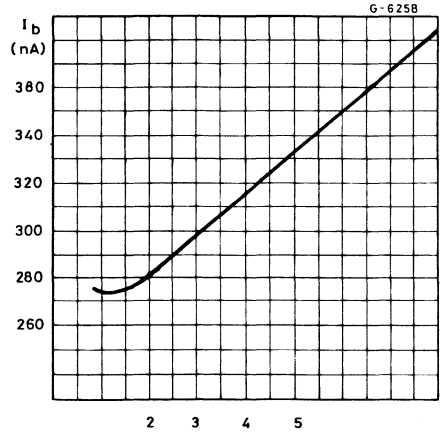


Figure 6 : Distortion Versus. Output Level.

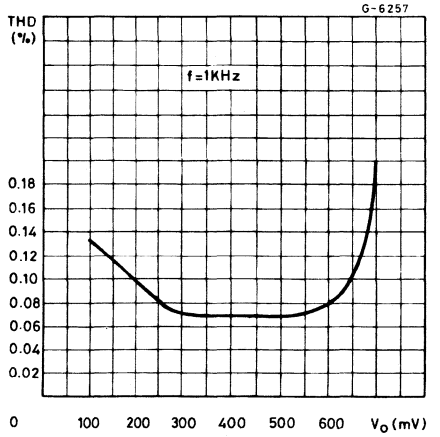


Figure 7 : Distortion vs Frequency.

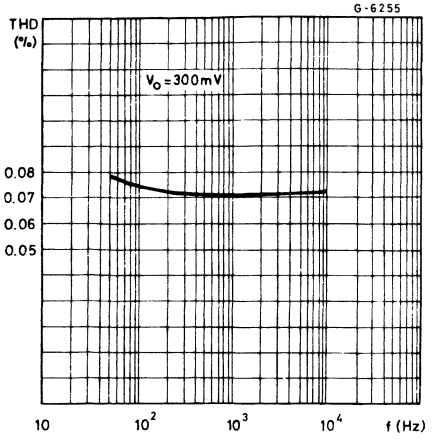


Figure 8 : NAB Response of Circuit of Fig. 1.

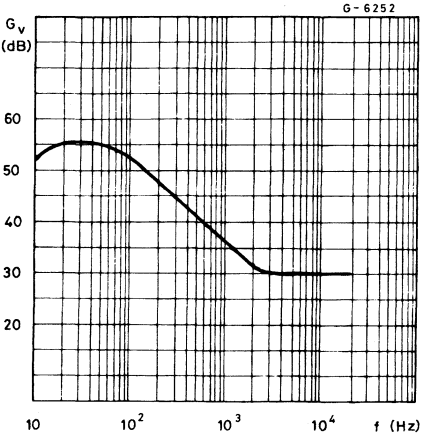


Figure 9 : Supply Voltage rejection vs. Frequency.

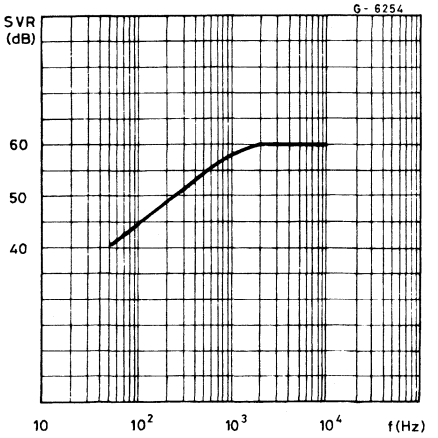
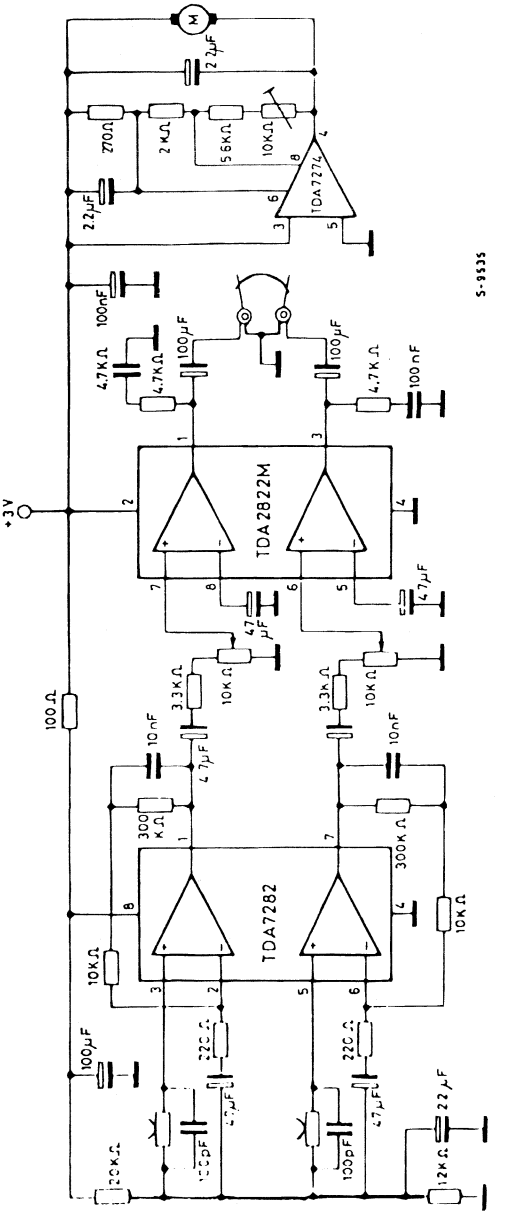


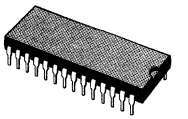
Figure 10 : Stereo Cassette Player with Motor Speed Control.

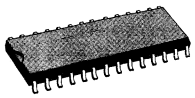


DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

PRELIMINARY DATA

- SINGLE SUPPLY OPERATION
- FOUR STEREO INPUT SOURCE SELECTION
- MONO INPUT
- TREBLE, BASS, VOLUME AND BALANCE CONTROL
- FOUR INDEPENDENT SPEAKER CONTROL (front/rear)
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- VERY LOW NOISE AND VERY LOW DISTORTION
- POP FREE SWITCHING





DIP-28
(plastic)

SO-28

ORDER CODES : TDA7300 (DIP-28)
TDA7300D (SO-28)

DESCRIPTION

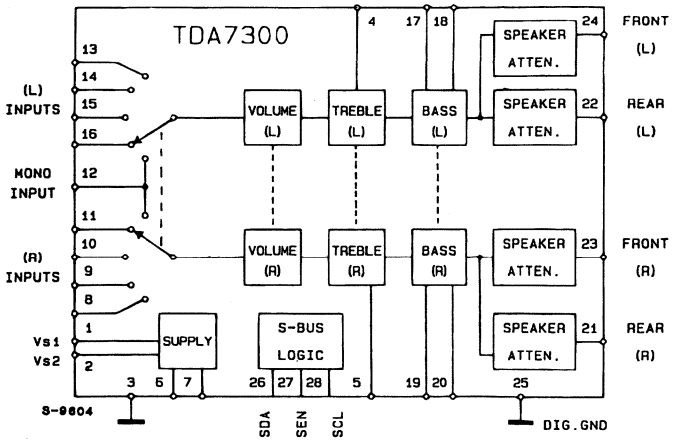
The TDA 7300 is a volume, tone (bass and treble) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi systems.

Control is accomplished by serial bus microprocessor interface.

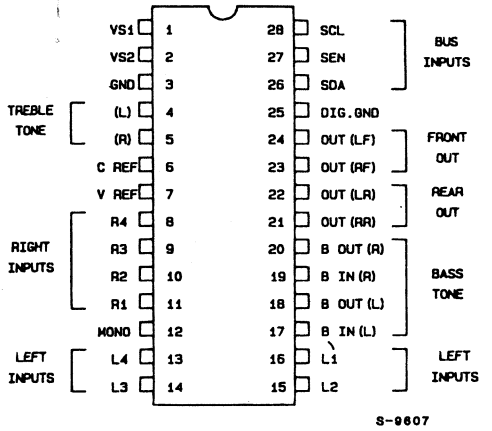
The AC signal setting is obtained by resistor networks and analog switches combined with operational amplifiers.

The results are : low noise, low distortion and high dynamic range.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	18	V
T_{amb}	Operating Ambient Temperature	– 40 to 85	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

THERMAL DATA

			DIP-28	SO-28	
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	65	85	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C ; V_{s1} = 12V or V_{s2} = 8.5V ; R_L = 10KΩ ; and R_g = 600Ω ; f =1KHz unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY (1)						
V_{s1}	Supply Voltage V_{s1}		10	12	16	V
V_{s2}	Supply Votlage V_{s2}		6	8.5	10	V
I_{s2}	Supply Current		20	30	40	mA
V_{ref}	Reference Voltage (pin 7)		3.5	4.3	5	V
SVR	Ripple Rej. at V_{s1}	f = 300Hz to 10KHz	80	100		dB
SVR	Ripple Rej. at V_{s2}	f = 300Hz to 10KHz	50	60		dB

Note : 1. The circuit can be supplied either at V_{S1} or at V_{S2} without the use of the internal voltage regulator. The circuit also operates at a supply voltage V_{S1} lower than 10 V. In this case the ripple rejection of V_{S2} is valid, because the voltage regulator saturates to about 0.8 V.

ELECTRICAL CHARACTERISTICS (continued)

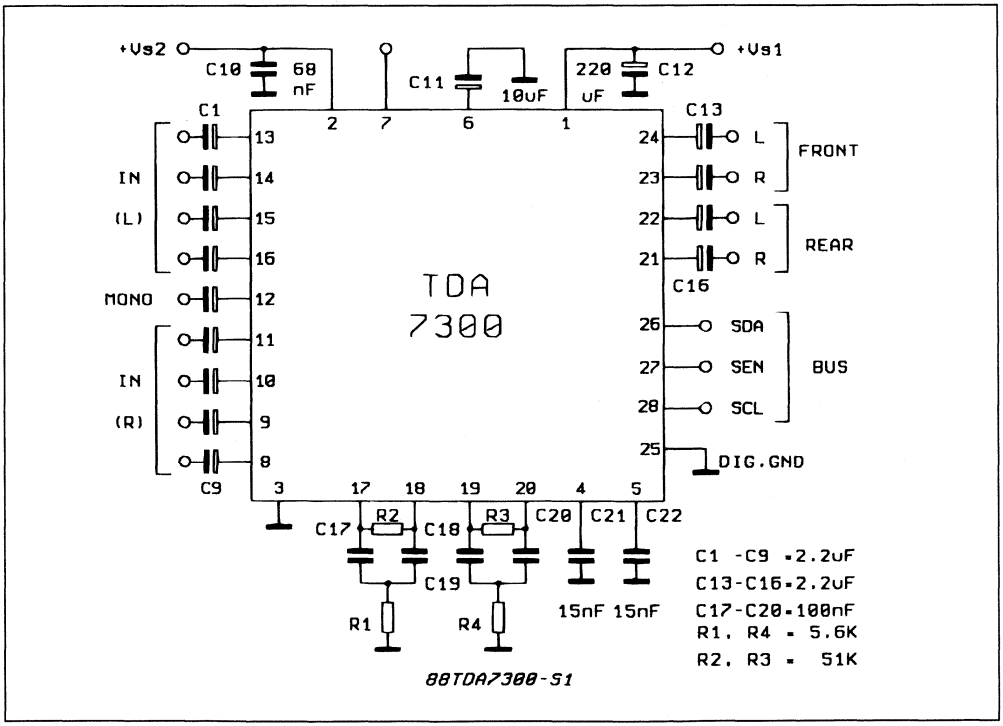
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INPUT SELECTORS						
R_i	Input Resistance		30	45		KΩ
$V_{IN\ MAX}$	Input Signal	G_v = 0 dB ; d = 0.3 %	1.5	2.2		VRMS
C_s	Channel Separation	f = 1 KHz	90	100		dB
		f = 10 KHz	70	80		dB
V_i (DC)	DC Voltage Level		3.5	4.3	5	V
VOLUME CONTROLS						
	Control Range			78		dB
G_{max}	Max Gain			10		dB
	Max Attenuation		64	68		dB
	Step Resolution	G_v = − 50 to 10 dB		2	3	dB
	Attenuator Set Error				2	dB
	Tracking Error				2	dB
SPEAKER ATTENUATORS						
	Control Range		35	38	41	dB
	Step Resolution			2	3	dB
	Attenuator Set Error				2	dB
	Tracking Error				2	dB
BASS AND TREBLE CONTROL (2)						
	Control Range			± 15		dB
	Step Resolution			2.5	3.5	dB
AUDIO OUTPUT						
Vo	Output Voltage	d = 0.3%	1.5	2.2		VRMS
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				1	nF
R_o	Output Resistance			70	150	Ω
V_o (DC)	DC Voltage Level		3	3.8	4.5	V

Note : 2. Bass and Treble response see attached diagram. The center frequency and quality of the resonance behaviour can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
e_{NO}	Output Noise	G_v = 0 dB BW = 22 Hz to 22 KHz		6		µV
		G_v = 0 dB Curve A		4		µV
S/N	Signal to Noise Ratio	All Gain = 0 dB V_o = 1 VRMS BW = 22 Hz to 22 KHz		105		dB
d	Distortion	f = 1 KHz ; V_o = 1 V ; G_v = 0		0.01	0.1	%
	Frequency Response (– 1dB)	G_v = 0 dB High Low	20		 30	KHz Hz
S_c	Channel Separation Left/Right	f = 1 KHz f = 10 KHz	90 70	100 80		dB dB
BUS INPUTS						
V_{iL}	Input LOW Voltage				0.8	V
V_{IH}	Input High Voltage		2.4			V
V_o	Output Voltage SDA Acknowledge	I = 1.6mA			0.4	V

Figure 1 : Test Circuit.



APPLICATION INFORMATION

Figure 2 : P. C. Board and Component Layout of the Circuit in Fig. 11 (1 : 1 scale).

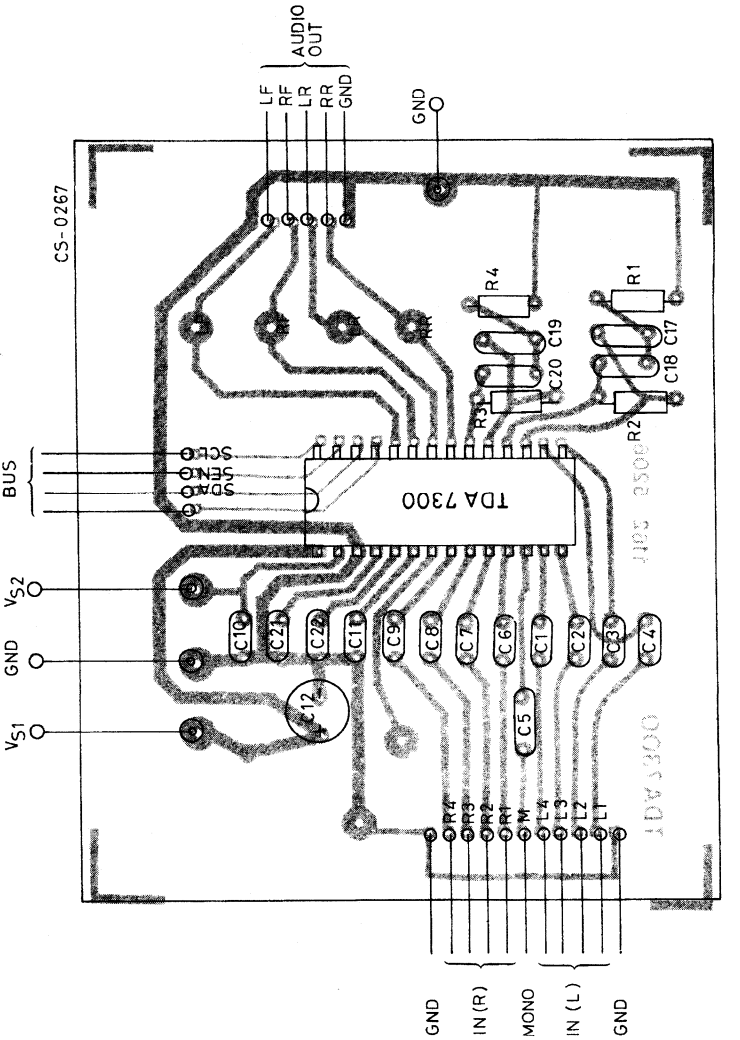


Figure 3 : Total Output Noise vs. Volume Setting.

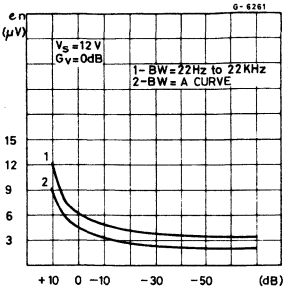


Figure 4 : Signal to Noise Ratio vs. Volume Setting.

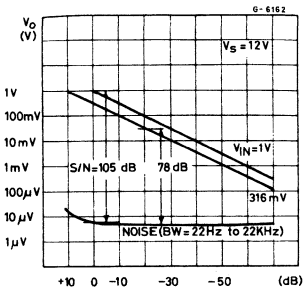


Figure 5 : Distortion + Noise vs. Frequency.

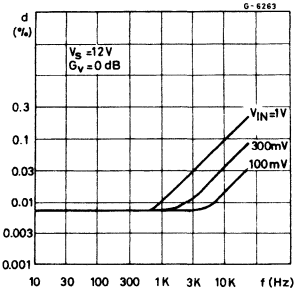


Figure 6 : Distortion vs. Output Voltage.

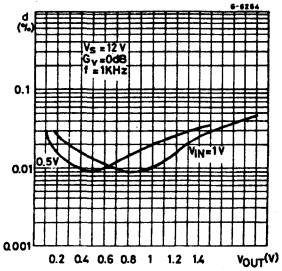


Figure 7 : Distortion vs. Load Resistance.

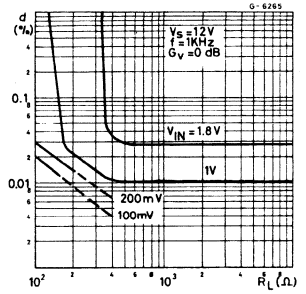


Figure 8 : Channel Separation (L1 – R1) vs. Frequency.

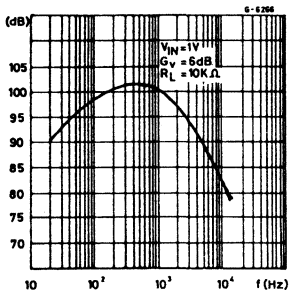


Figure 9 : Channel Separation (L1 – L2) vs. Frequency.

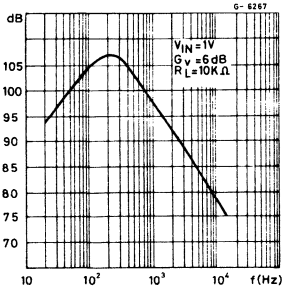


Figure 10 : Supply Voltage Rejection (V_{S1}) vs Frequency.

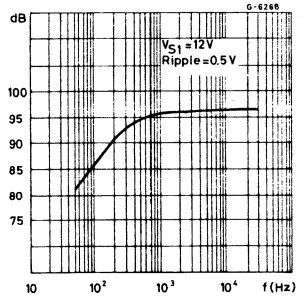


Figure 11 : Supply Voltage Rejection (V_{S2}) vs. Frequency.

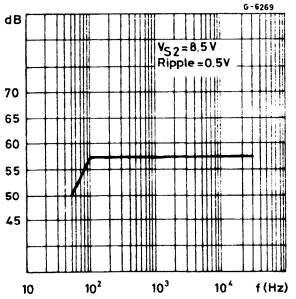


Figure 12 : Supply Voltage Rejection Versus V_{S1}.

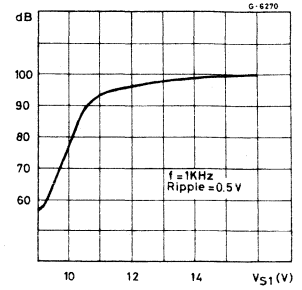


Figure 13 : Supply Voltage Rejection Versus V_{S2}.

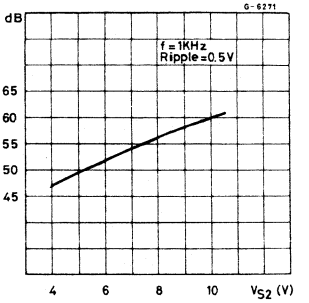


Figure 14 : Clipping Level (V_{ms}) vs. Supply Voltage.

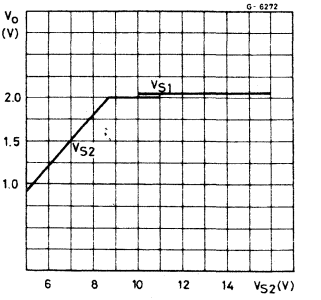


Figure 15 : Quiescent Current vs. Supply Voltage.

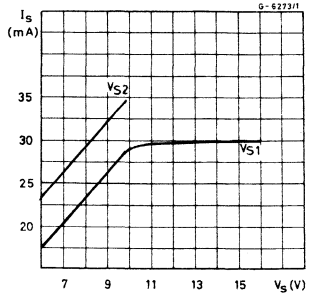


Figure 16 : Quiescent Current vs. Temperature.

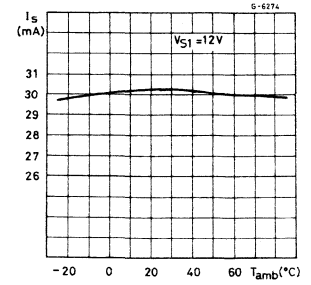


Figure 17 : Typical Tone Response.

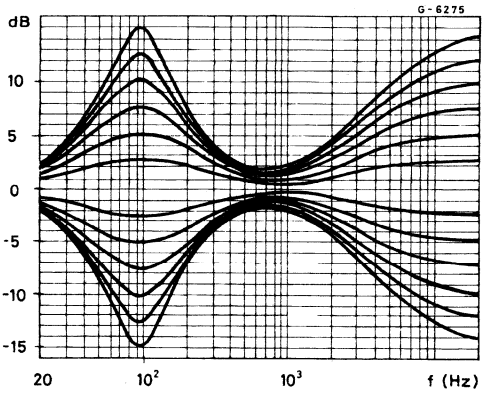
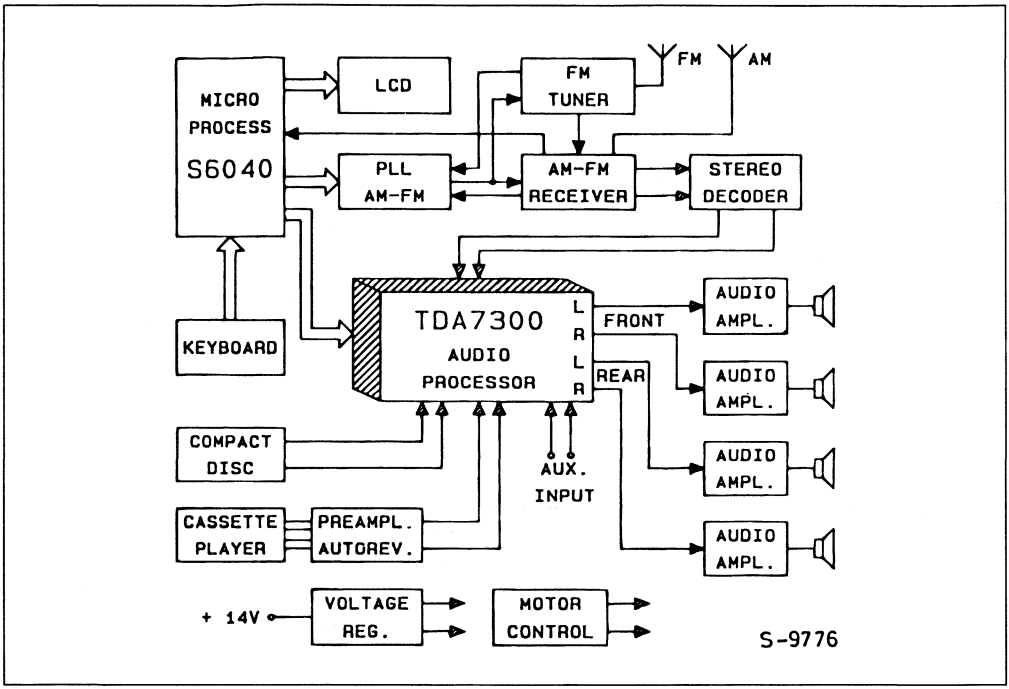


Figure 18 : Complete Car-radio System Using Digital Controlled Audio Processor.

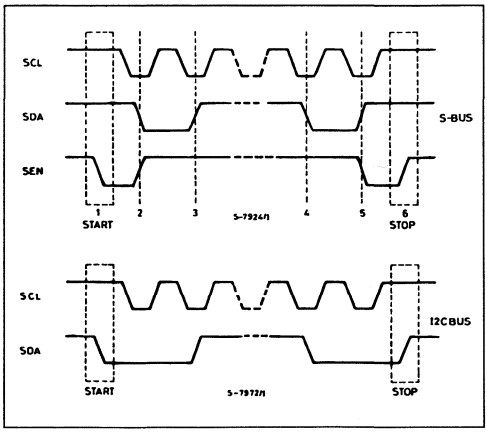


SERIAL BUS INTERFACE

S-BUS Interface and I²C BUS Compatibility. Data transmission from microprocessor to the TDA7300 and viceversa takes place thru the 3-wire S-BUS interface, consisting of the three lines SDA, SCL, SEN. If SDA and SEN inputs are shortcircuited together, then the TDA7300 appears as a standard I2CBUS slave.

In this case the S6040 µP can be programmed to generate the two different transmission systems : the S-BUS using the three lines of the serial bus, and the I2CBUS using the SCL and SDA lines only.

Figure 19 : Timing Diagram of S-BUS and I2CBUS.

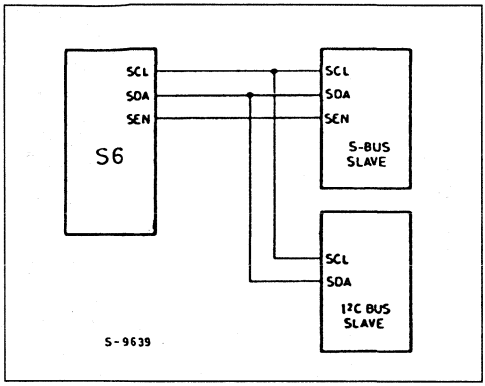


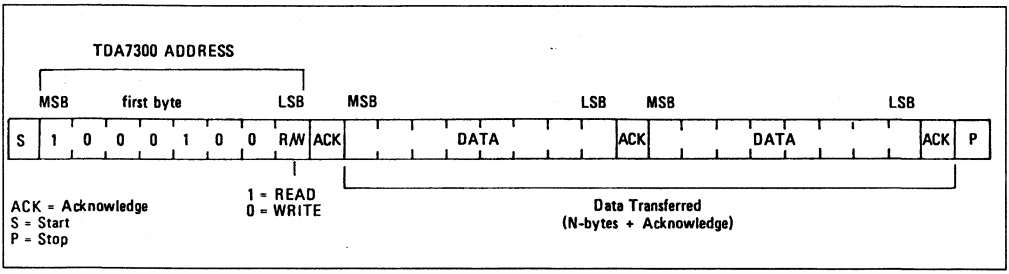
Interface Protocol

The interface protocol comprises :

- A start condition (S)
- A chip address byte, containing the TDA7300 address and the direction of the transmission on the BUS (this information is given in the 8th bit of the byte : "0" means "write", that is from the master to the slave, while "1" means "read"). The TDA7300 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)

Figure 20 : System with Mixed S-Bus Peripherals.





SOFTWARE SPECIFICATION

Chip address (TDA7300 address)

1 0 0 0 1 0 0 0
MSB LSB

DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	X	X	S2	S1	S0	Audio Switch
0	1	1	0	C3	C2	C1	C0	Bass Control
0	1	1	1	C3	C2	C1	C0	Treble Control

X = don't care. Bx = 10 dB steps.
Ax = 2 dB steps. Cx = 2.5 dB steps.

Status after Power-on-reset

Volume	– 68 dB
Speaker	– 38 dB
Audio Switch	Mono
Bass	+ 2.5 dB
Treble	+ 2.5 dB

Note : Using S6 is it necessary an external EPROM (M2716 F6X) previously programmed. Further information is available in S6 µP datasheet.

DATA BYTES (detailed description)

Volume

MSB					LSB			
0	0	B2	B1	B0	A2	A1	A0	Volume 2dB Steps
					0	0	0	0
					0	0	1	– 2
					0	1	0	– 4
					0	1	1	– 6
					1	0	0	– 8
					1	0	1	Not Allowed
					1	1	0	Not Allowed
					1	1	1	Not Allowed
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB Steps
		0	0	0				+ 10
		0	0	1				0
		0	1	0				– 10
		0	1	1				– 20
		1	0	0				– 30
		1	0	1				– 40
		1	1	0				– 50
		1	1	1				– 60

For example if you want setting the volume at -32 dB the 8 bit string is : 0 0 1 0 0 0 0 1.

Speaker Attenuators

MSB					LSB			
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	– 2
					0	1	0	– 4
					0	1	1	– 6
					1	0	0	– 8
					1	0	1	Not Allowed
					1	1	0	Not Allowed
					1	1	1	Not Allowed
			0	0				0
			0	1				– 10
			1	0				– 20
			1	1				– 30

For example attenuation of 24 dB on speaker RF is giving by : 1 0 1 1 0 0 1 0.

Audio Switch - Select the input channel to activate

MSB			LSB					
0	1	0	X	X	S2	S1	S0	Audio Switch
			X	X	0	0	0	Stereo 1
			X	X	0	0	1	Stereo 2
			X	X	0	1	0	Stereo 3
			X	X	0	1	1	Stereo 4
			X	X	1	0	0	Mono
			X	X	1	0	1	Not Allowed
			X	X	1	1	0	Not Allowed
			X	X	1	1	1	Not Allowed

X = don't care.
For example to set the stereo 2 channel the 8 bit string may be : 0 1 0 0 0 0 0 1.

Bass and Treble - Control range of ± 15dB (boost and cut) steps of 2.5dB

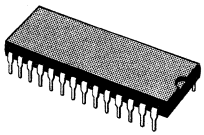
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treable
				0	0	0	0	− 15
				0	0	0	1	− 15
				0	0	1	0	− 12.5
				0	0	1	1	− 10
				0	1	0	0	− 7.5
				0	1	0	1	− 5
				0	1	1	0	− 2.5
				0	1	1	1	− 0
				1	1	1	1	+ 0
				1	1	1	0	+ 2.5
				1	1	0	1	+ 5
				1	1	0	0	+ 7.5
				1	0	1	1	+ 10
				1	0	1	0	+ 12.5
				1	0	0	1	+ 15
				1	0	0	0	+ 15

C3 = sign.
For example Bass at -12.5 dB is obtained by the following 8 bit string : 0 1 1 0 0 0 1 0.

DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

PRELIMINARY DATA

- INPUT AND OUTPUT PINS FOR EXTERNAL EQUALIZER
- THREE STEREO INPUT SOURCE SELECTION PLUS MONO INPUT
- TREBLE, BASS, VOLUME AND BALANCE CONTROL
- FOUR INDEPENDENT SPEAKER CONTROL (front/rear)
- SINCE SUPPLY OPERATION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- VERY LOW NOISE AND VERY LOW DISTORTION
- POP FREE SWITCHING



DIP28
(Plastic)

ORDER CODE : TDA7302

DESCRIPTION

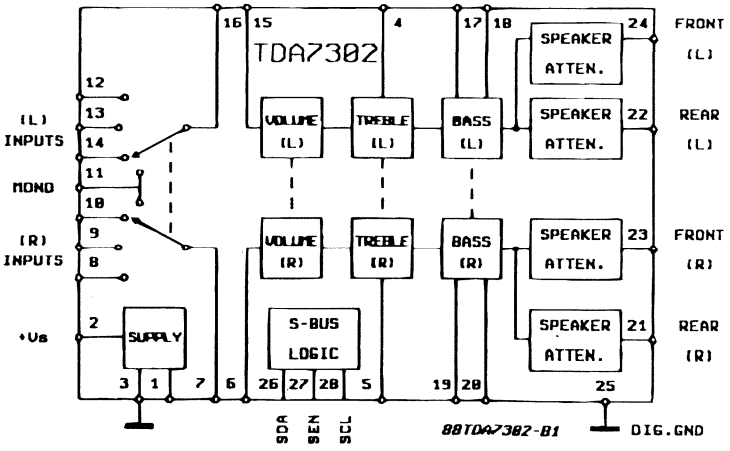
The TDA7302 is a volume, tone (bass and treble) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi systems.

Control is accomplished by serial bus microprocessor interface.

The AC signal setting is obtained by resistor networks and analog switches combined with operational amplifiers.

The results are : low noise, low distortion and high dynamic range.

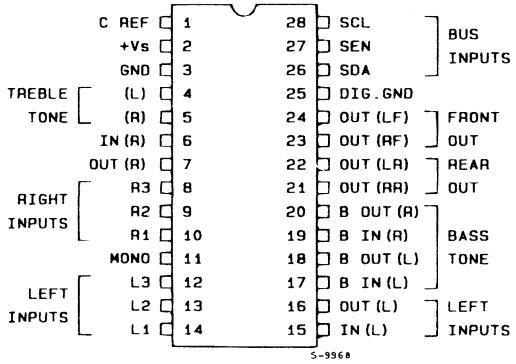
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	14	V
P_{tot}	Total Power Dissipation (T_{amb} = 25°C)	2	W
T_{amb}	Operating Ambient Temperature	– 40 to 85	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

$R_{(th\ j\text{-}pins)}$	Thermal Resistance Junction-pins	Max.	65	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C ; V_S = 10V ; R_L = 10kΩ ; and R_g = 600Ω ; f =1kHz unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	10	14	V
I_s	Supply Current		20	30	40	mA
SVR	Ripple Rejection	f = 300Hz to 10kHz	50	60		dB
INPUT SELECTORS						
R_i	Input Resistance		30	45		kΩ
$V_{IN\ MAX}$	Input Signal	G_v = 0dB ; d = 0.3%	1.5	2.2		V_{RMS}
C_s	Channel Separation	f = 1kHz	90	96		dB
		f = 10kHz	70			
R_L	Output Load Resistance		5			kΩ
V_i (DC)	Input DC Voltage		3.5	4.3	5	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VOLUME CONTROLS						
R_{in}	Input Resistance		7	10		kΩ
	Control Range			78		dB
G_{max}	Max Gain			10		dB
	Max Attenuation		64	68		dB
	Step Resolution			2	3	dB
	Attenuator Set Error	G_v = – 50 to 10dB			2	dB
	Tracking Error				2	dB
SPEAKER ATTENUATORS						
	Control Range		35	38	41	dB
	Step Resolution			2	3	dB
	Attenuator Set Error				2	dB
	Tracking Error				2	dB
BASS AND TREBLE CONTROL (1)						
	Control Range			± 15		dB
	Step Resolution			2.5	3.5	dB
AUDIO OUTPUT						
V_o	Output Voltage	d = 0.3%	1.5	2.2		V_{RMS}
R_L	Output Load Resistance		2			kΩ
C_L	Output Load Capacitance				1	nF
R_o	Output Resistance			70	150	Ω
V_o (DC)	DC Voltage Level		3	3.8	4.5	V
GENERAL						
e_{No}	Output Noise	BW = 22Hz to 22kHz, G_v = 0 dB		6		μV
		BW = 22Hz to 22kHz, Out Atten. ≥ 20dB		3.5		μV
		G_v = 0dB, Curve A		4		μV
S/N	Signal to Noise Ratio	All Gain = 0dB, V_o = 1V_{RMS}, BW = 22Hz to 22kHz		105		dB
d	Distortion	f = 1kHz, V_o = 1V, G_v = 0		0.01	0.1	%
	Frequency Response (– 1dB)	G_v = 0dB, High	20			kHz
		G_v = 0dB, Low			20	Hz
S_c	Channel Separation Left/Right	f = 1kHz		100		dB
		f = 10kHz		82		dB

Note : (1) Bass and Treble response see attached diagram. The center frequency and quality of the resonance behaviour can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BUS INPUTS						
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage		2.4			V
V_o	Output Voltage SDA Acknowledge	I = 1.6mA			0.4	V
	Digital Input Current		– 5		+ 5	µA

Figure 1 : Test Circuit.

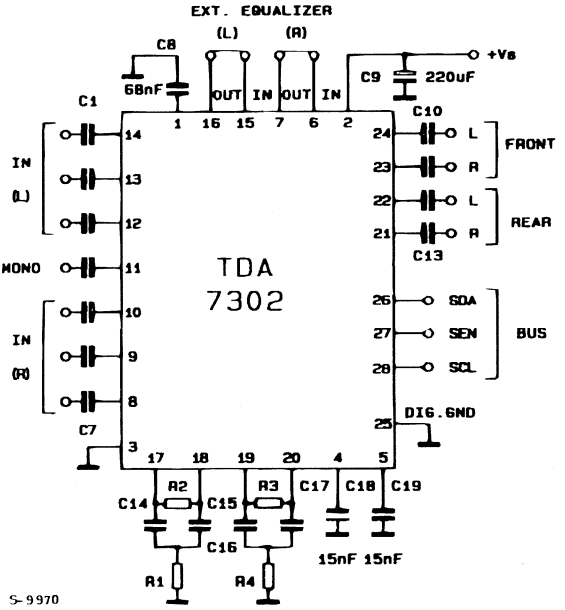


Figure 2 : Total Output Noise vs. Volume Setting.

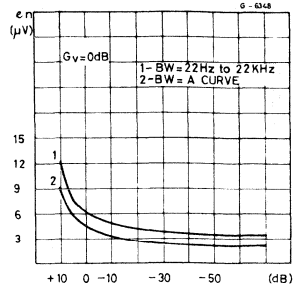


Figure 3 : Signal to Noise Ratio vs. Volume Setting.

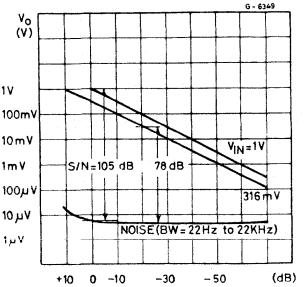


Figure 4 : Distortion + Noise vs. Frequency.

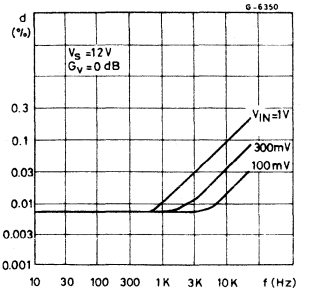


Figure 5 : Distortion vs. Output Voltage.

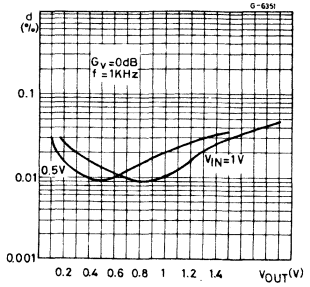


Figure 6 : Distortion vs. Load Resistance.

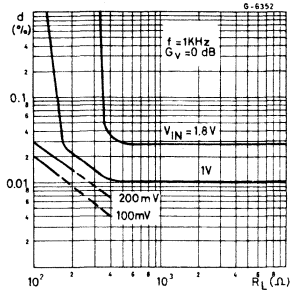


Figure 7 : Channel Separation (L1 – R1) vs. Frequency.

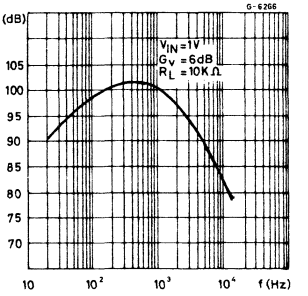


Figure 8 : Channel Separation (L1 – L2) vs. Frequency.

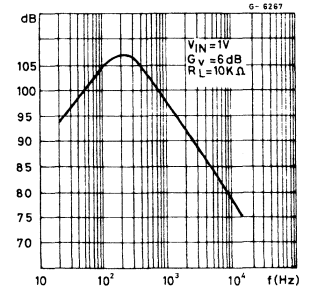


Figure 9 : Supply Voltage Rejection vs. Frequency.

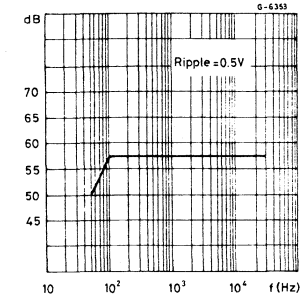
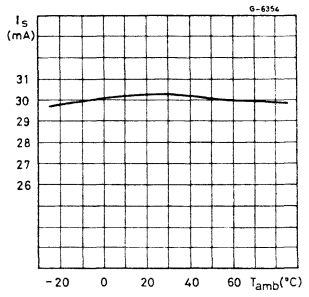


Figure 10 : Quiescent Current vs. Temperature.



APPLICATION INFORMATION

VOLUME CONTROL CONCEPT

Traditional electronic volume control circuits use a multiplier technique with all the disadvantages of high noise and distortion.

The used concept, as shown in fig. 11 with digital switched resistor dividers, provides extremely low noise and distortion. The multiplexing of the resistive dividers is realized with a multiple-input operational amplifier.

BASS AND TREBLE CONTROL

The principle operation of the bass control is shown in fig. 12. The external filter together with the internal buffer allows a flexible filter design according to the different requirements in car radios. The function of the treble is similar to the bass.

A typical filter curve is shown in fig 13.

OUTPUTS

A special class-A output amplifier with a modulated sink current provides low distortion and ground compatibility with low current consumption.

Figure 11 : Volume Control.

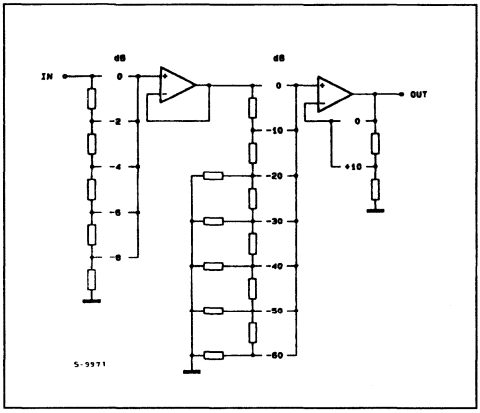


Figure 12 : Bass Control.

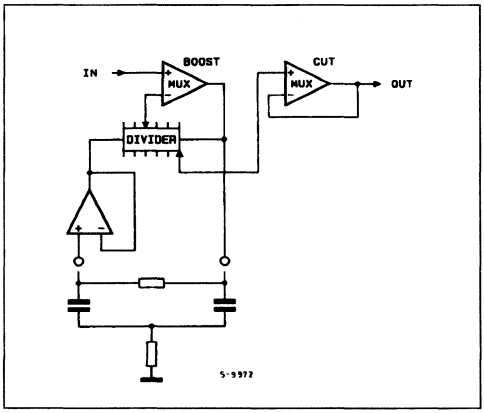


Figure 13 : Typical Tone Response.

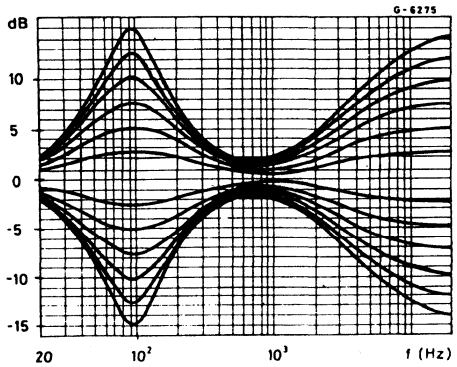
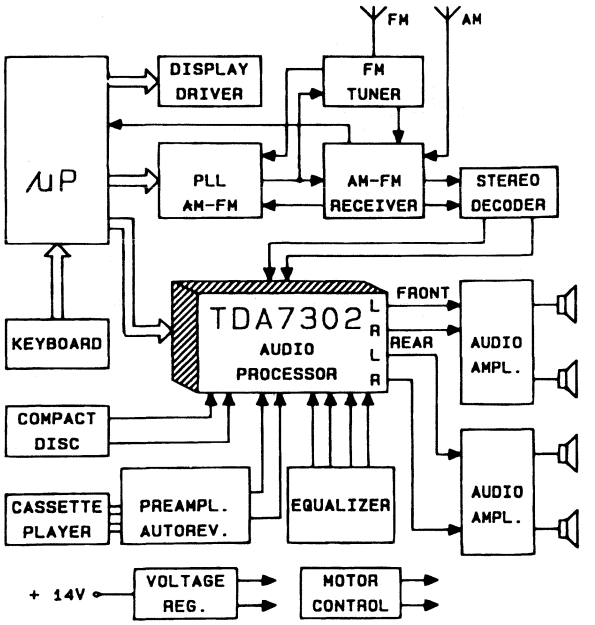


Figure 14 : Complete Car-radio System Using Digital Controlled Audio Processor.

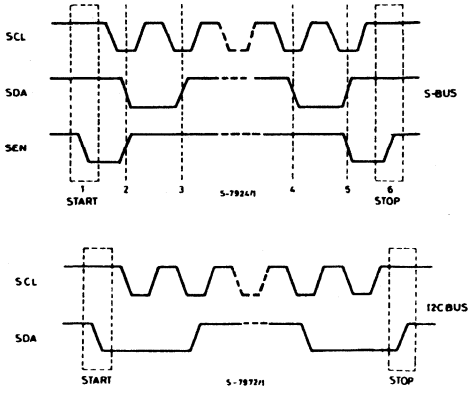


SERIAL BUS INTERFACE

S-BUS Interface and I^2C BUS Compatibility.
Data transmission from microprocessor to the TDA7302 and viceversa takes place thru the 3-wire S-BUS interface, consisting of the three lines SDA, SCL, SEN. If SDA ane SEN inputs are short-circuited together, then the TDA7302 appears as a standard I2 CBUS slave.

In this case the S6040 P can be programmed to generate the two different transmission systems : the S-BUS using the three lines of the serial bus, and the I2CBUS using the SCL and SDA lines only.

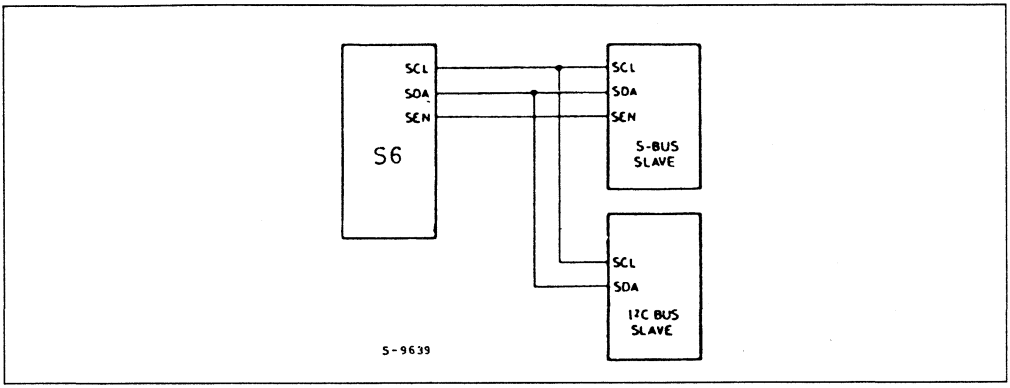
Figure 15 : Timing Diagram of S-BUS and I^2 CBUS.

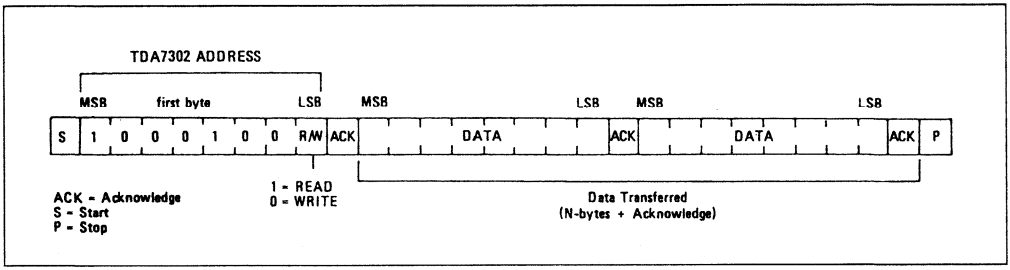


Interface protocol.
The interface protocol comprises:

- A start conditions (S)
- A chip address byte, containing the TDA7302 address and the direction of the transmission on the BUS (this information is given in the 8th bit of the byte : "0" means "write", that is from the maste r to the slave, while "1" means "read"). The TDA7302 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)

Figure 16 : System with Mixed S-Bus Peripherals.





SOFTWARE SPECIFICATION

Chip Address (TDA7302 address)

1 0 0 0 1 0 0 0

MSB LSB

DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	X	X	S2	S1	S0	Audio Switch
0	1	1	0	C3	C2	C1	C0	Bus Control
0	1	1	1	C3	C2	C1	C0	Treble Control

X = don't care
Ax = 2 dB steps
Bx = 10 dB steps
Cx = 2.5 dB steps

STATUS AFTER POWER-ON-RESET

Volume	– 68 dB
Speaker	– 38 dB
Audio Switch	Mono
Bass	+ 2.5 dB
Treble	+ 2.5 dB

Note : Using S6 is it necessary an external EPROM (M2716 F6X) previously programmed. Further information is available in S6 µP datasheet.

DATA BYTES (detailed description)

Volume

MSB					LSB			
0	0	B2	B1	B0	A2	A1	A0	Volume 2 dB Steps
					0	0	0	0
					0	0	1	− 2
					0	1	0	− 4
					0	1	1	− 6
					1	0	0	− 8
					1	0	1	Not Allowed
					1	1	0	Not Allowed
					1	1	1	Not Allowed
0	0	B2	B1	B0	A2	A1	A0	Volume 10 dB Steps
		0	0	0				+ 10
		0	0	1				0
		0	1	0				− 10
		0	1	1				− 20
		1	0	0				− 30
		1	0	1				− 40
		1	1	0				− 50
		1	1	1				− 60

For example if you want setting the volume at − 32 dB the 8 bit string is : 0 0 1 0 0 0 0 1.

Speaker Attenuators

MSB		LSB						
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	− 2
					0	1	0	− 4
					0	1	1	− 6
					1	0	0	− 8
					1	0	1	Not Allowed
					1	1	0	Not Allowed
					1	1	1	Not Allowed
			0	0				0
			0	1				− 10
			1	0				− 20
			1	1				− 30

For example attenuation of 24 dB on speaker RF is giving by : 1 0 1 1 0 0 1 0.

Audio Switch - Select the Input Channel to Activate

MSB			LSB					
0	1	0	X	X	S2	S1	S0	Audio Switch
			X	X	0	0	0	Stereo 1
			X	X	0	0	1	Stereo 2
			X	X	0	1	0	Stereo 3
			X	X	0	1	1	Mute Input
			X	X	1	0	0	Mono
			X	X	1	0	1	Not Allowed
			X	X	1	1	0	Not Allowed
			X	X	1	1	1	Not Allowed

X = don't care.
For example to set the stereo 2 channel the 8 bit string may be : 0 1 0 0 0 0 0 1.

Bass and Treble - Control Range of ± 15 dB (boost and cut) Steps of 2.5 dB

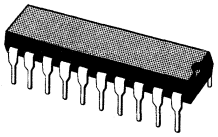
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	− 15
				0	0	0	1	− 15
				0	0	1	0	− 12.5
				0	0	1	1	− 10
				0	1	0	0	− 7.5
				0	1	0	1	− 5
				0	1	1	0	− 2.5
				0	1	1	1	− 0
				1	1	1	1	+ 0
				1	1	1	0	+ 2.5
				1	1	0	1	+ 5
				1	1	0	0	+ 7.5
				1	0	1	1	+ 10
				1	0	1	0	+ 12.5
				1	0	0	1	+ 15
				1	0	0	0	+ 15

C3 = Sign.
For example, Bass at – 12.5 dB is obtained by the following 8 bit string : 0 1 1 0 0 0 1 0.

TDA2220A

AM/FM RADIO

- VERY WIDE RANGE OF SUPPLY VOLTAGE 3 TO 16 V
- HIGH RECOVERED AUDIO SIGNAL
- DESIGNED FOR USE WITH EXTERNAL RATIO DETECTOR OR INTERNAL QUADRATURE DETECTOR
- VERY GOOD AM SIGNAL HANDLING (1V; m = 0.8)
- VERY SIMPLE DC SWITCHING OF AM-FM SECTIONS
- SUITABLE FOR CAPACITANCE, VARICAP AND INDUCTIVE TUNING
- VERY LOW TWEET
- COMMON (AM-FM) FIELD STRENGTH METER OUTPUT PIN



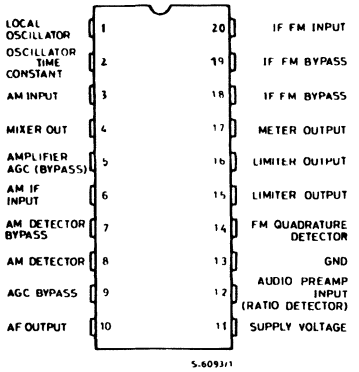
DIP - 20
(0.25)

ORDER CODE : TDA2220A

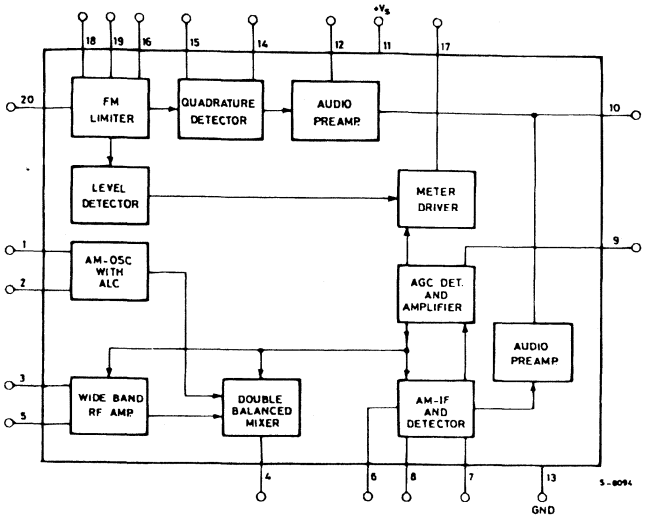
DESCRIPTION

The TDA 2220A is a high performance AM/FM radio IC designed for use in a wide range of car radio, portable radio and home radio applications, operating on a supply voltage from 3 to 16 V. A special feature of this device is that it may be used with an internal quadrature detector or an external ratio detector. The TDA 2220A is supplied in a 20 pin plastic DIP package.

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	16	V
P_{tot}	Total Power Dissipation at $T_{amb} \leq 70$ °C	800	mW
T_{op}	Operating Temperature	– 20 to 70	°C
T_{stg}–T_j	Storage and Junction Temperature	– 55 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuits, T_{amb} = 25 °C, V_s = 9 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		3	9	16	V
I_d	Current Drain	AM Section		16	21	mA
		FM Section		14	21	

AM SECTION (f_o = 1 MHz ; f_m = 1 KHz)

V_i	Input Sensitivity	S/N = 26 dB m = 0.3		12	25	µV
$\frac{S+N}{N}$	Signal to Noise Ratio	V_i = 10 mV m = 0.3	45	50		dB
V_i	AGC Range	ΔV_{out} = 10 dB m = 0.8	100			dB
V_o	Recovered Audio Signal (pin 10)	V_i = 1 mV m = 0.3	75	120	170	mV
d	Distortion			0.4		%
d	Distortion	V_i = 1 mV m = 0.8		2	3	%
V_H	Max Input Signal Handling Capability	m = 0.8 d < 10 %	1			V
R_i	Input Resistance between Pins 3 and 5	m = 0		7.5		KΩ
C_i	Input Capacitance between Pins 3 and 5	m = 0		18		pF
R_o	Output Resistance (pin 10)		4.5	7	9.5	KΩ
	Tweet 2 IF	m = 0.3 V_i = 1 mV		38		dB
	Tweet 3 IF			55		dB
V_m	Meter Output	V_i = 1 mV m = 0.3	2.5	3.5		V
		V_i = 5 µV			200	mV

FM SECTION (f_o = 10.7 MHz ; f_m = 1 KHz) (RATIO DETECTOR)

V_i	Input Limiting Voltage	– 3 dB Limiting Point		25	36	µV
AMR	Amplitude Modulation Rejection	Δf = ± 22.5 KHz m = 0.3 V_i = 3 mV	50	60		dB
$\frac{S+N}{N}$	Signal to Noise Ratio	Δf = ± 22.5 KHz V_i = 10 mV	55	70		dB
d	Distortion	Δf = ± 75 KHz V_i = 1 mV		0.4	0.7	%
d	Distortion	Δf = ± 22.5 KHz V_i = 1 mV		0.2		%
V_o	Recovered Audio Signal (pin 10)	Δf = ± 22.5 KHz V_i = 1 mV	90	130	170	mV
R_i	Input Resistance between Pin 20 and Ground	Δf = 0		6.5		KΩ
C_i	Input Capacitance between Pin 20 and Ground	Δf = 0		14		pF
R_o	Output Resistance (pin 10)		4.5	7	9.5	KΩ
V_m	Meter Output	Δf = ± 22.5 KHz V_i = 3 mV	3.1	4.1		V
		V_i = 500 µV	1.5	2.3	3.0	V
		V_i = 10 µV			0.2	V

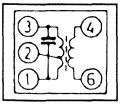
(*) Meter resistance = 1.3 KΩ.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
FM SECTION (f_o = 10.7 MHz ; f_m = 1 KHz) (QUADRATURE DETECTOR)						
V_i	Input Limiting Voltage	– 3 dB Limiting Point		25	36	µV
AMR	Amplitude Modulation Rejection	$\Delta f = \pm$ 22. 5 KHz m = 0.3 V_i = 10 mV		40		dB
$\frac{S+N}{N}$	Signal to Noise Ratio	$\Delta f = \pm$ 22.5 KHz V_i = 10 mV	55	65		dB
d	Distortion	$\Delta f = \pm$ 75 KHz V_i = 1 mV		0.7	1.5	%
d	Distortion	$\Delta f = \pm$ 22.5 KHz V_i = 1 mV		0.25		%
d	Distortion (double tuned)			0.1		%
V_o	Recovered Audio Signal (pin 10)	$\Delta f = \pm$ 22.5 KHz V_i = 1 mV	60	90	130	mV
R_i	Input Resistance between Pin 20 and Ground	Δf = 0		6.5		KΩ
C_i	Input Capacitance between Pin 20 and Ground	Δf = 0		14		pF
R_o	Output Resistance (pin 10)		4.5	7	9.5	KΩ
V_m	Meter Output	$\Delta f = \pm$ 22.5 KHz V_i = 3 mV	3.1	4.1		V
		V_i = 500 µV	1.5	2.3	3.0	V
		V_i = 10 µV			0.2	V

APPLICATION INFORMATION

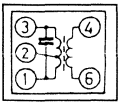
L1 - 455 kHz IF COIL



C_o(pF)	f (MHz)	Q_o	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	70	57	116	24

TOKO AM3 - 10 x 10 mm.
RCL - 4 A7525N

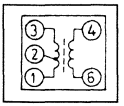
L2 - AM DETECTOR COIL



C_o(pF)	f (KHz)	Q_o	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	70	173	94	9

TOKO AM2 - 10 x 10 mm.
RCL - 4 A7524EK

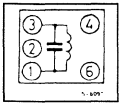
L3 -AM OSCILLATOR COIL



f (KHz)	L (µH)	Q_o	TURNS		
	1-3	1-3	1-2	2-3	4-6
796	220	80	2	75	8

TOKO - 10 x 10 mm.
RWO - 6 A6574N

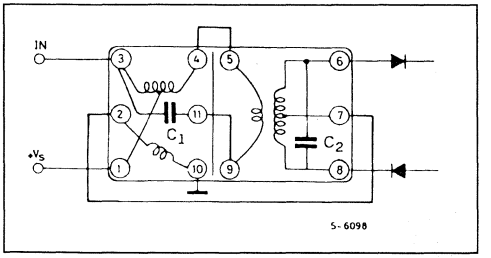
L4 - FM DETECTOR COIL



C_o(pF)	f (MHz)	Q_o	TURNS		
1-3		1-3	1-3	–	–
82	10.7	100	12	–	–

TOKO - 10 x 10 mm.
KACS - K 586 HM

L5 - RATIO DETECTOR

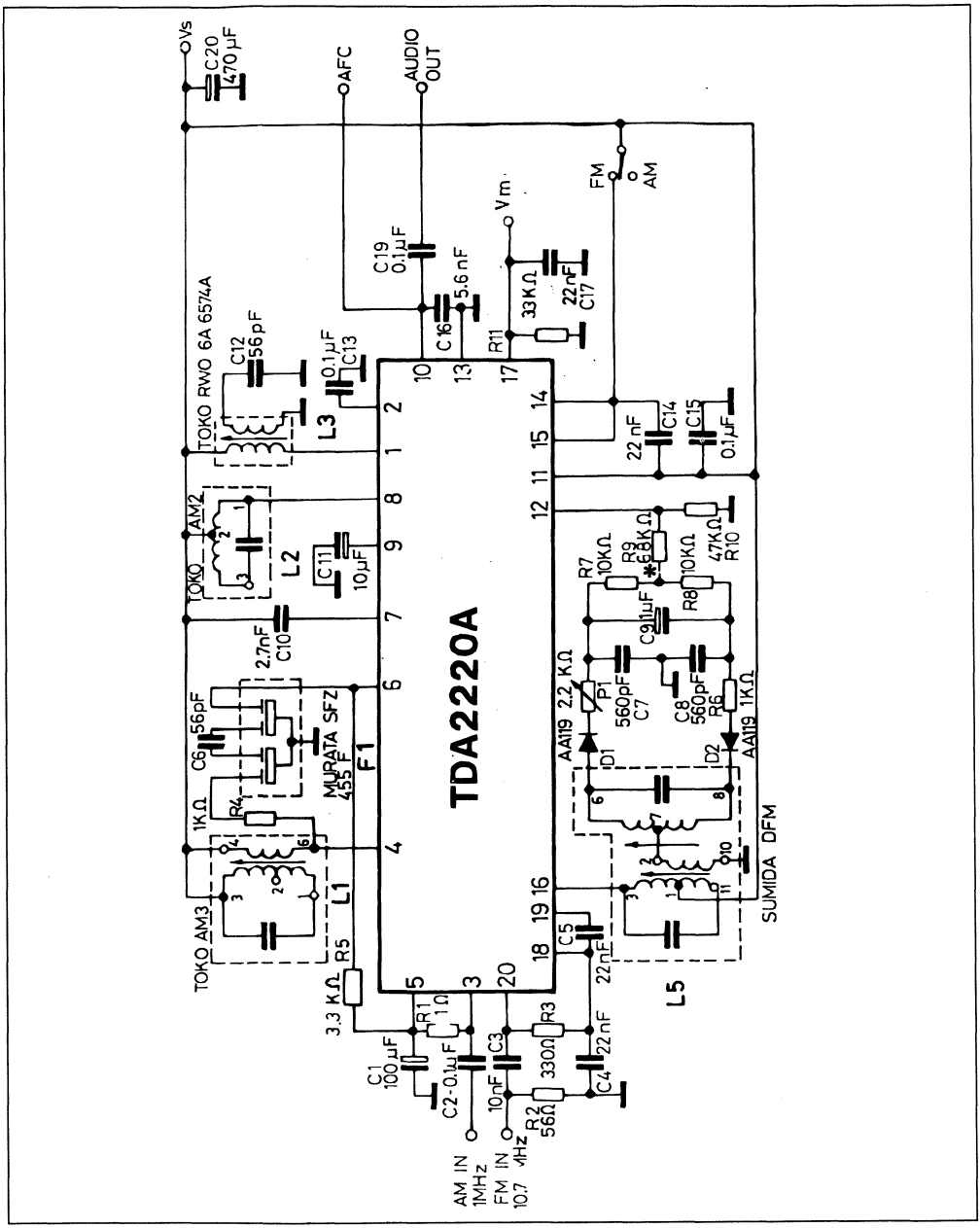


C_1(pF)	C_2(pF)	f (MHz)	Q_o
3-11	6-8		3-11/4-8
27	47	10.7	70

SUMIDA
DFM

TURNS					
1-3	1-4	2-10	5-9	6-7	7-8
11	6 1/2	5 1/2	1/2	7	7

Figure 1 : Test Circuit with FM Ratio Detector.



(*) The audio output amplitude can be modified changing the resistor value.

Figure 2 : Test Circuit with FM Quadrature Detector.

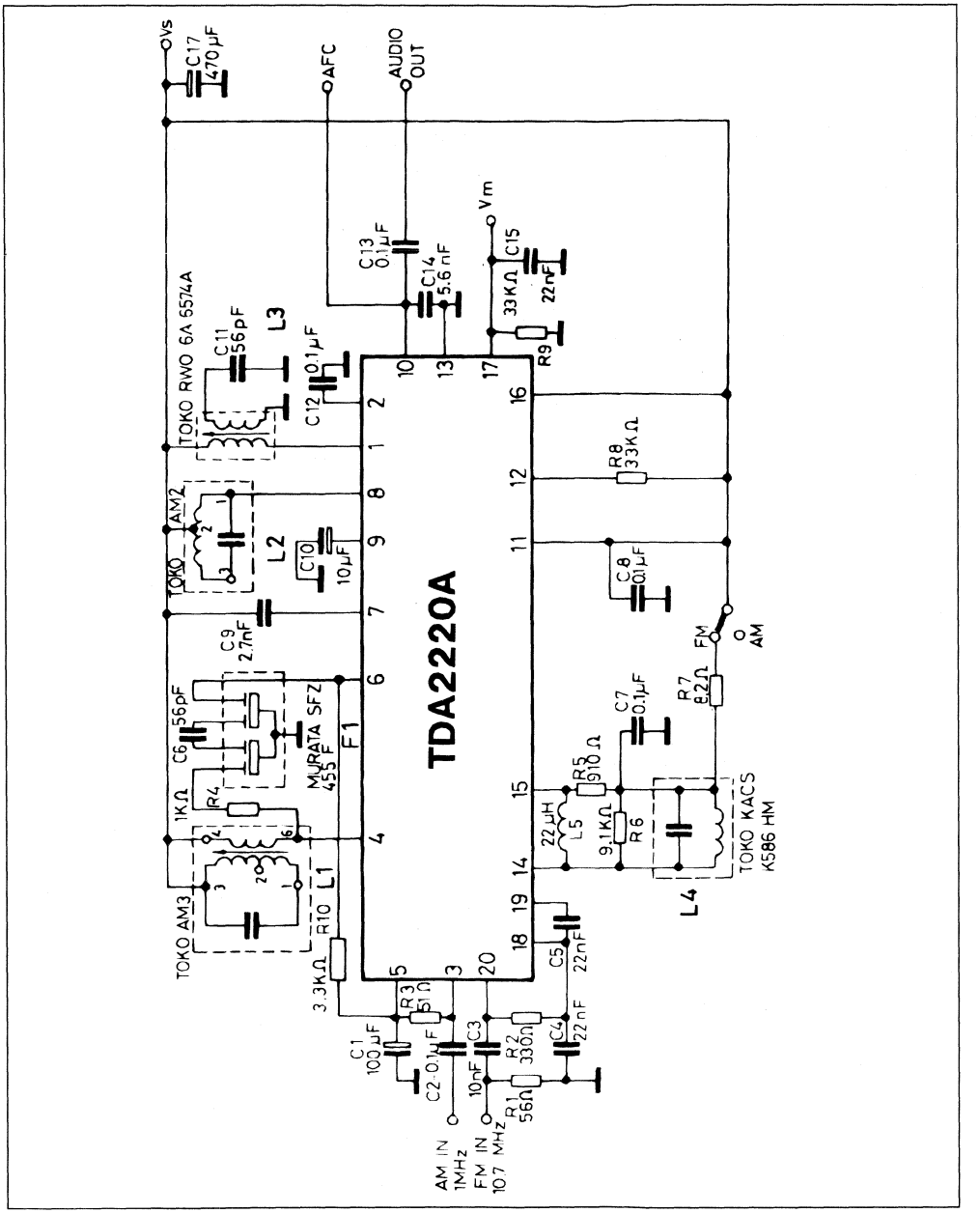
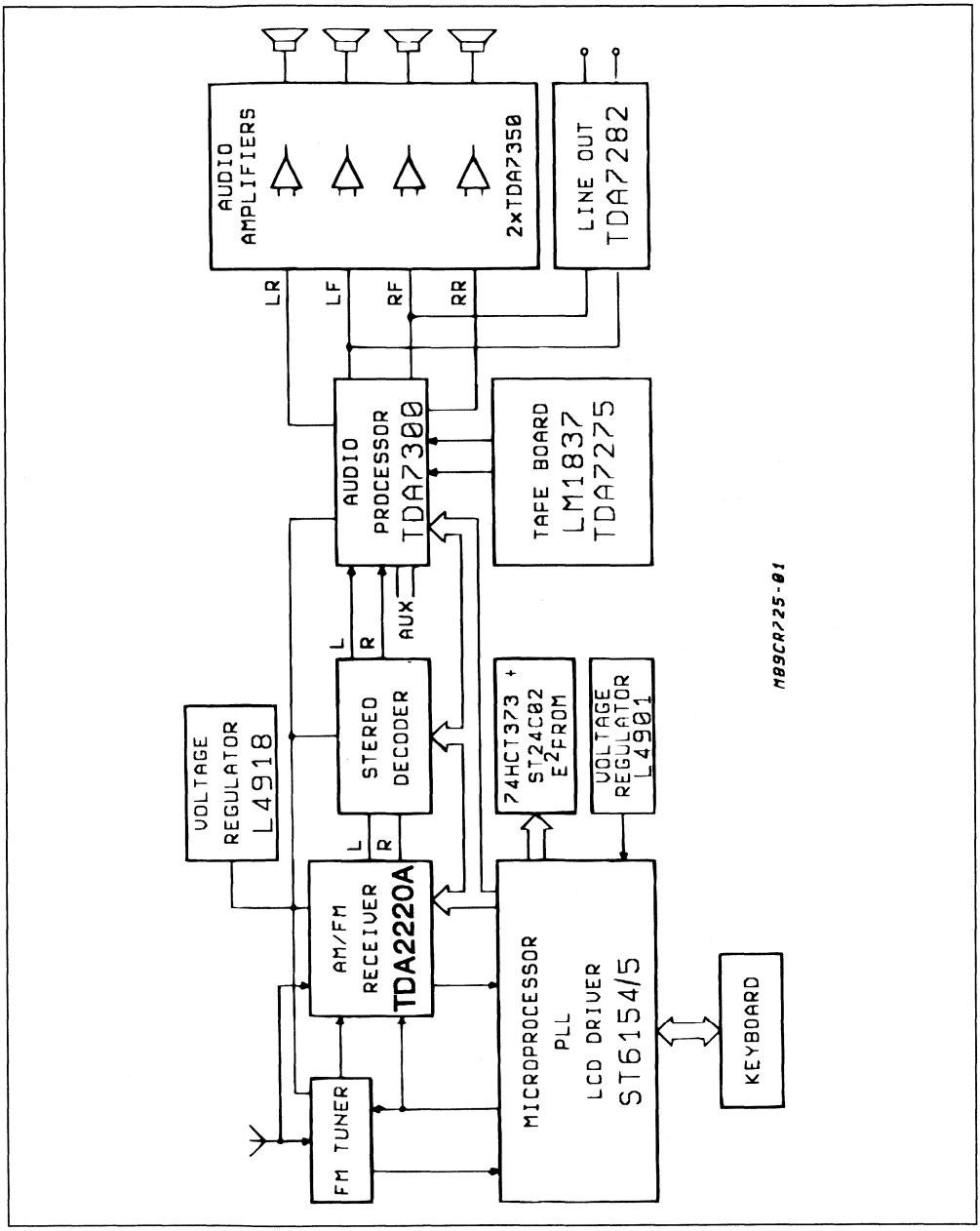
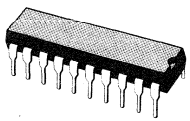


Figure 3 : Car Radio System..



HIGH PERFORMANCE MOTOR SPEED REGULATOR

- TACHIMETRIC SPEED REGULATION WITH NO NEED FOR AN EXTERNAL SPEED PICK-UP
- V/I SUPPLEMENTARY PREREGULATION
- DIGITAL CONTROL OF DIRECTION AND MOTOR STOP
- SEPARATE SPEED ADJUSTMENT
- 5.5 V TO 18 V OPERATING SUPPLY VOLTAGE
- 1 A PEAK OUTPUT CURRENT
- OUTPUT CLAMP DIODES INCLUDED
- SHORT CIRCUIT CURRENT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION (40 V)



POWERDIP
(16 + 2 + 2)

ORDER CODE : TDA7272

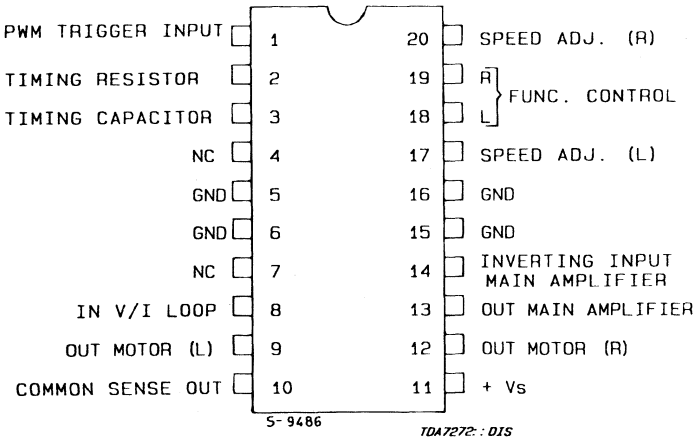
DESCRIPTION

TDA7272 is an high performance motor speed controller for small power DC motors as used in cassette players.

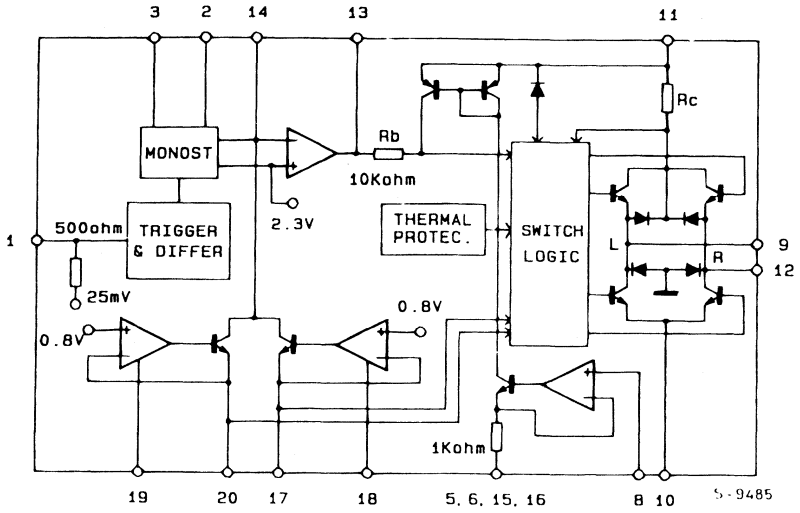
Using the motor as a digital tachogenerator itself the performance of true tacho controlled systems is reached.

A dual loop control circuit provides long term stability and fast settling behaviour.

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



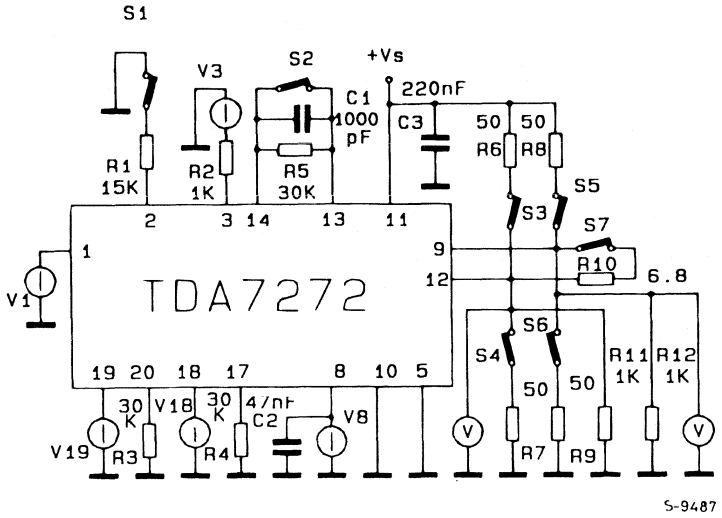
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	24	V
V_S	Dump Voltage (300 ms)	40	V
I_O	Output Current	internally limited	
P_{tot}	Power Dissipation at T_{pins} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_j	Operating Junction Temperature	– 40 to 150	°C
T_{stg}	Storage Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C ; V_S = 13.5 V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage		5.5		18	V
I_S	Supply Current	No Load		5	12	mA

OUTPUT STAGE

I_O	Output Current Pulse		1			A
I_O	Output Current Continuous		250			mA
$V_{10-9,12}$	Voltage Drop	I_O = 250 mA		1.2	1.5	V
$V_{11-9,12}$	Voltage Drop	I_O = 250 mA		1.7	2	V

MAIN AMPLIFIER

R_{14}	Input Resistance		100			kΩ
I_b	Bias Current			50		nA
V_{OFF}	Offset Voltage			1	5	mV
V_R	Reference Voltage	Internal at non Inverting Input		2.3		V

CURRENT SENSE AMPLIFIER V/I LOOP

R_8	Input Resistance		100			kΩ
G_L	Loop Gain			9		

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TRIGGER AND MONOSTABLE STAGE						
$V_{IN\,1}$	Input Allowed Voltage		– 0.7		3	V
$R_{IN\,1}$	Input Resistance			500		Ω
$V_{T\,Low}$	Trigger Level			0		V
$V_{T\,B}$	Bias Voltage (pin 1)		15	20	25	mV
$V_{T\,H}$	Trigger Histeresis			10		mV
$V_{2\,REF}$	Reference Voltage		750	800	850	mV
SPEED PROGRAMMING, DIRECTION CONTROL LOGIC AND CURRENT SOURCE PROGRAMMING						
$V_{18,19\,Low}$	Input Low Level				0.7	V
$V_{18,19\,High}$	Input High Level		2			V
$I_{18,19}$	Input Current	$0 < V_{18,19} < V_S$		2		μA
$V_{17,20\,REF}$	Reference Voltage		735	800	865	mV

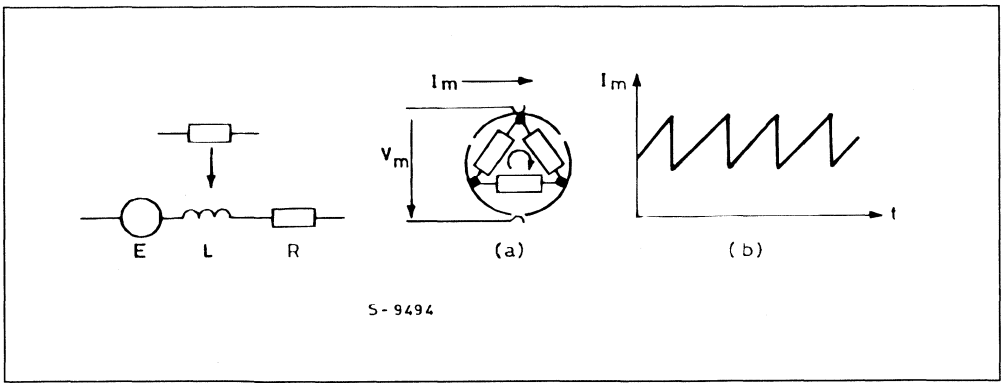
OPERATING PRINCIPLE

The TDA7272 novel applied solution is based on a tachometer control system without using such extra tachometer system. The information of the actual motor speed is extracted from the motor itself. A DC motor with an odd number of poles generates a motor current which contains a fixed number of discontinuities within each rotation. (6 for the 3 pole motor example on fig. 1)

Deriving this inherent speed information from the motor current, it can be used as a replacement of a low resolution AC tachometer system. Because the settling time of the control loop is limited on principle by the resolution in time of the tachometer, this control principle offers a poor reaction time for motors with a low number of poles. The realized circuit is extended by a second feed forward loop in order to improve such system by a fast auxiliary control path.

This additional path senses the mean output current and varies the output voltage according to the voltage drop across the inner motor resistance. Apart from a current averaging filter, there is no delay in such loop and a fast settling behaviour is reached in addition to the long term speed motor accuracy.

Figure 1 : Equivalent of a 3 Pole DC Motor (a) and Typical motor Current Waveform (b).



BLOCK DESCRIPTION

The principle structure of the element is shown in fig. 2. As to be seen, the motor speed information is derived from the motor current sense drop across the resistors R_S ; capacitor CD together with the input impedance of 500 Ω at pin 1 realizes a high pass filter.

This pin is internally biased at 20 mV, each negative zero transition switches the input comparator. A 10 mV hysteresis improves the noise immunity.

The trigger circuit is followed by an internal delay time differentiator.

Thus, the system becomes widely independent of the applied waveform at pin 1, the differentiator triggers a monostable circuit which provides a constant current duration. Both, output current magnitude and duration T, are adjustable by external elements CT and RT.

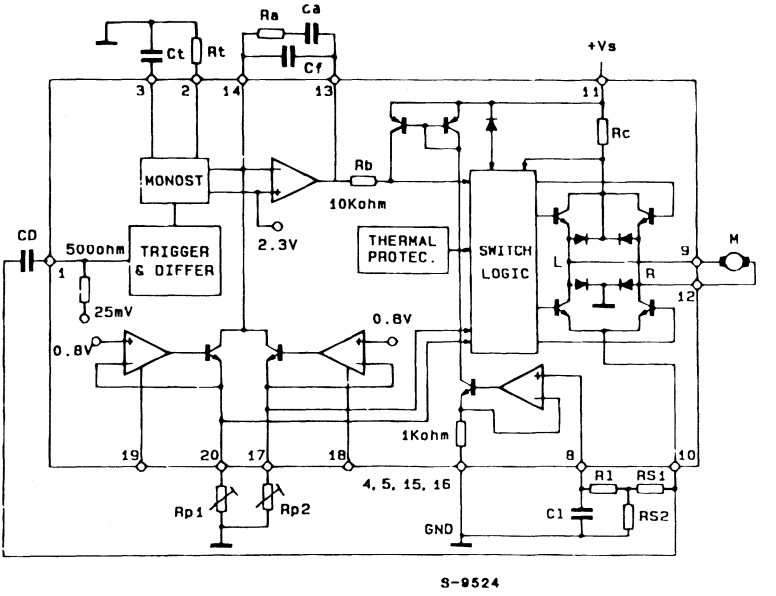
The monostable is retriggerable ; this function prevents the system from fault stabilization at higher harmonics of the nominal frequency.

The speed programming current is generated by two separate external adjustable current sources. A corresponding digital input signal enables each current source for left or right rotation direction. Resistor RP1 and RP2 define the speed, the logical inputs are at pin 18 and 19.

At the inverting input (pin 14) of the main amplifier the reference current is compared with the pulsed monostable output current.

For the correct motor speed, the reference current matches the mean value of the pulsed monostable current. In this condition the charge of the feedback capacitor becomes constant.

Figure 2 : Block Diagram.



The speed n of a k pole motor results :

$$n = \frac{10,435}{C_T K R_p}$$

and becomes independent of the resistor RT which only determines the current level and the duty cycle which should be 1 : 1 at the nominal speed for minimum torque ripple.

The second fast loop consists of a voltage to current converter which is driven at pin 8 by the low pass filter R_L, C_L. The output current at this stage is injected by a PNP current mirror into the inner resistor R_B. So the driving voltage of the output stage consists of the integrator output voltage plus the fast loop voltage contribution across R_B.

The power output stage realizes different modes depending on the logic status at pin 18 and 19.

- normal operation for left and right mode : each upper TR of the bridge is used as voltage follower whereas the lower acts as a switch.
- stop mode where the upper half is open and the lower is conductive.
- high impedance status where all power elements are switched-off.

The high impedance status is also generated when the supply voltage overcomes the 5 V to 20 V operating range or when the chip temperature exceeds 150 °C.

A short circuit protection limits the output current at 1.5 A. Integrated diodes clamp spikes from the inductive load both at V_{CC} and ground.

The reference voltages are derived from a common bandgap reference. All blocks are widely supplied by an internal 3.5 V regulator which provides a maxi-

PIN FUNCTION AND APPLICATION INFORMATION

PIN 1

Trigger input. Receives a proper voltage which contains the information of the motor speed. The waveform can be derived directly by the motor current (fig. 3). The external resistor generates a proper voltage drop. Together with the input resistance at pin 1 [$R_{IN}(1) = 500\ \Omega$] the external capacitor C_D realize a high pass filter which differentiates the commutation spikes of the motor current. The trigger level is 0V.

The biasing of the pin 1 is 20 mV with a hysteresis of 10 mV. So the sensing resistance must be chosen high enough in order to obtain a negative spike of the least 30 mV on pin 1, also with minimum variation of motor current :

$$R_S \geq \frac{30\ mV}{\Delta I_{MOT}\ min.}$$

Such value can be too much high for the preregulation stage V-I and it could be necessary to split them into 2 series resistors $R_S = R_{S1} + R_{S2}$ (see fig. 4) as explained on pin 8 section.

Figure 3.

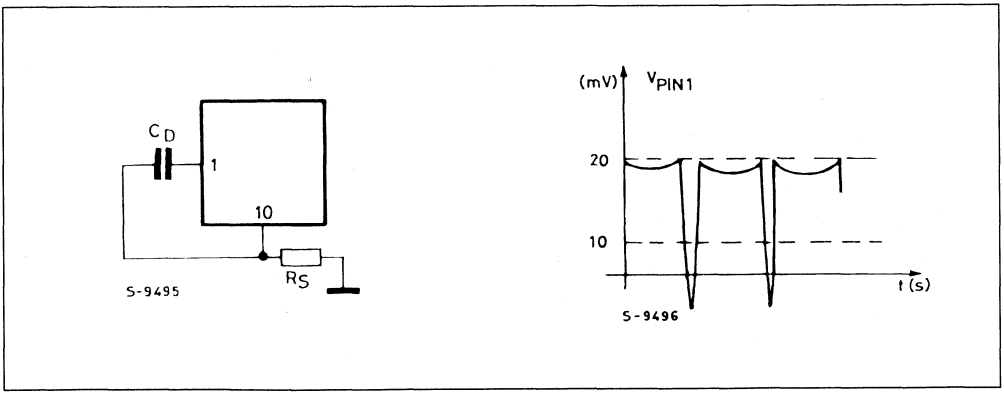


Figure 4.

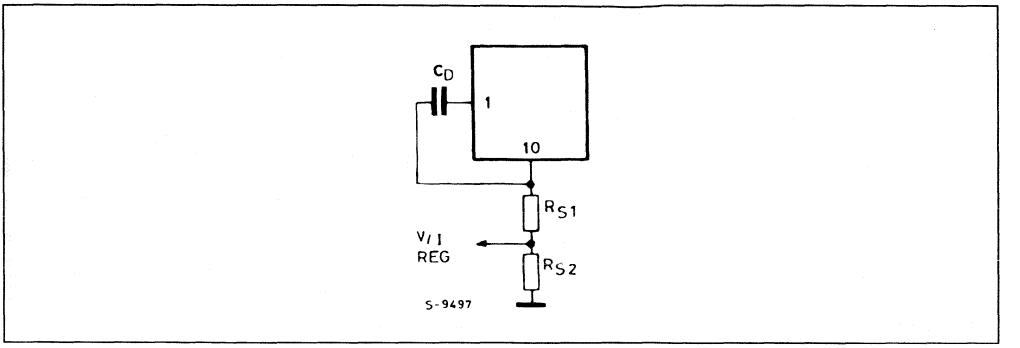
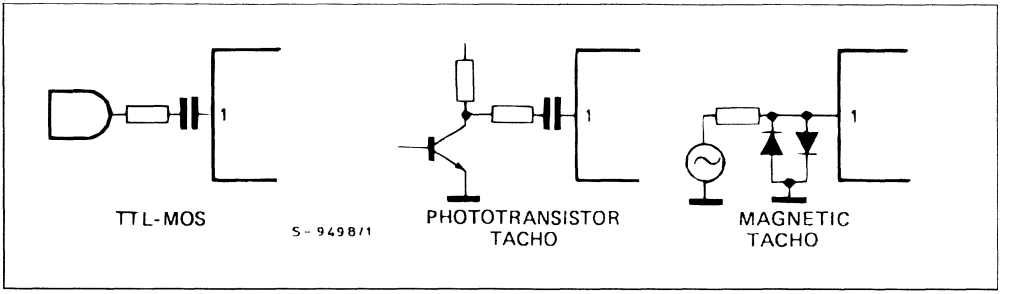


Figure 5.



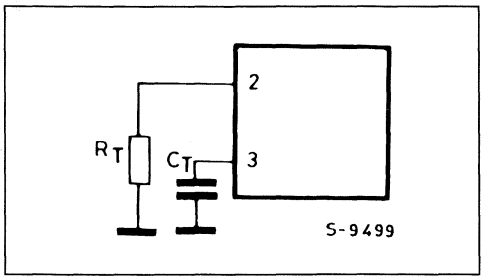
The information can be taken also from an external tachogenerator. Fig. 5 shows various sources connections :

the input signal mustn't be lower than 0.7 V.

PIN 2

Timing resistor. An internal reference voltage (V2 = 0.8 V) gives possibility to fix by an external resistor (R_T), from this pin and ground, the output current amplitude of the monostable circuit, which will be reflected into the timing capacitor (pin 3) ; the typical value would be about 50 μ A.

Figure 6.



PIN 3

Timing capacitor. A constant current, determined by the pin 2 resistor, flowing into a capacitor between pin 3 and ground provides the output pulse width of the monostable circuit, the max voltage at pin 3 is fixed by an internal threshold : after reaching this value the capacitor is rapidly discharged and the pulse width is fixed to the value :

$$T_{on} = 2.88\ R_T\ C_T \text{ (fig. 6)}$$

PIN 4

Not connected.

PIN 5

Ground. Connected with pins 6, 15, 16.

PIN 6

Ground. Connected with pins 5, 15, 16.

PIN 7

Not connected.

PIN 8

Input V/I loop. Receives from pin 10, through a low pass filter, the voltage with the information of the

current flowing into the motor and produces a negative resistance output :

$$R_{out} = -9\,R_S \text{ (fig. 7)}$$

For compensating the motor resistance and avoiding instability :

$$RS \leq \frac{R_{MOTOR}}{9}$$

The optimization of the resistor R_S for the tachometric control must not give a voltage too high for the V/I stage : one solution can be to divide in two parts, as shown in fig. 8, with :

$$R_{S2} = \frac{R_M}{10} \quad \text{and} \quad R_{S1} + R_{S2} \geq$$

$$\geq \frac{30\text{ mV}}{\Delta Imot\ min} \text{ (see pin 1 sect.)}$$

The low pass filter R_L, C_L must be calculated in order to reduce the ripple of the motor commutation at least 20 dB. Another example of possible pins 10-8 connections is showed on fig. 9. A choke can be used in order to reduce the radiation.

PIN 9

Output motor left. The four power transistors are realized as darlington structures. The arrangement is controlled by the logic status at pins 18 and 19.

As before explained (see block description), in the normal left or right mode one of the lower darlington becomes saturated whereas the other remains open. The upper half of the bridge operates in the linear mode.

In stop condition both upper bridge darlingtons are off and both lower are on. In the high output impedance state the bridge is switched completely off.

Connecting the motor between pins 9 and 12 both left or right rotation can be obtained. If only one rotation sense is used the motor can be connected at only one output, by using only the upper bridge half. Two motors can be connected each at the each output : in such case they will work alternatively (see application section).

The internal diodes, together with the collector substrate diodes, protect the output from inductive voltage spikes during the transition phase (fig. 10)

Figure 7.

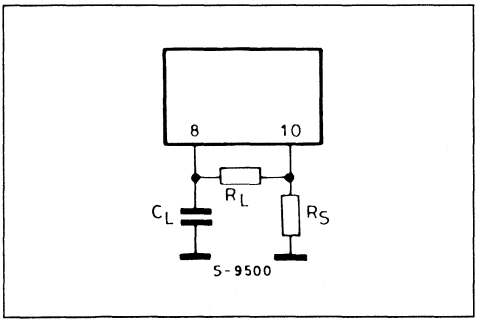


Figure 8.

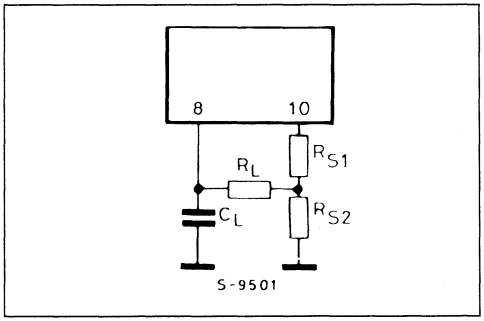


Figure 9.

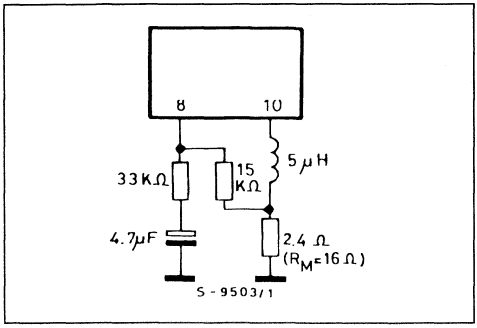
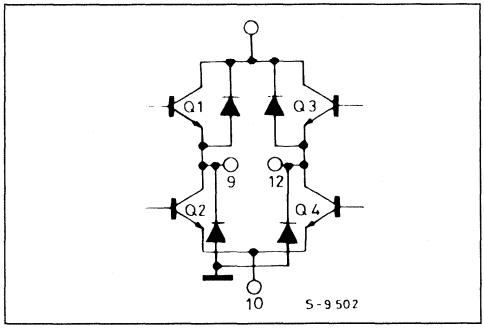


Figure 10.



PIN 10

Common sense output. From this pin the output current of the bridge configuration (motor current) is fed into R_S external resistor in order to generate a proper voltage drop.

The drop is supplied into pin 1 for tachometric control and into pin 8 for V/I control (see pin 1 and pin 8 sections).

PIN 11

Supply voltage.

PIN 12

Output motor right. (see pin 9 section)

PIN 13

Output main amplifier. The voltage on this pin results from the tachometric speed control and feeds the output stage.

The value of the capacitor C_F (fig. 11), connected from pins 13 and 14, must be chosen low enough in order to obtain a short reaction time of the tachometric loop, and high enough in order to reduce the output ripple.

A compromise is reached when the ripple voltage (peak-to-peak) V_{ROP} is equal to 0.1 V_{MOTOR} :

$$C_F = 2.3 \frac{C_T}{V_{RIP}} \left(1 - \frac{R_T}{R_p}\right)$$

$$\text{with } V_{RIP} = \frac{V_{FEM} + IMOT \cdot R_{MOT}}{10} \text{ and}$$

with duty cycle = 50 %. (see pin 2-3 section)

In order to compensate the behaviour of the whole system regulator-motor-load (considering axis friction, load torque, inertias moment of the motor of the load. etc.) a RC series network is also connected between pins 13 and 14 (fig. 12). The value of C_A and R_A must been chosen experimentally as follows:

- increase of 10 % the speed with respect to the nominal value by connecting in parallel to R_p a resistor with value about 10 time larger.
- vary the R_A and C_A values in order to obtain at pin 13 a voltage signal with short response time and without oscillations. Fig. 13 shows the step response at pin 13 versus R_A and C_A values.

Figure 11.

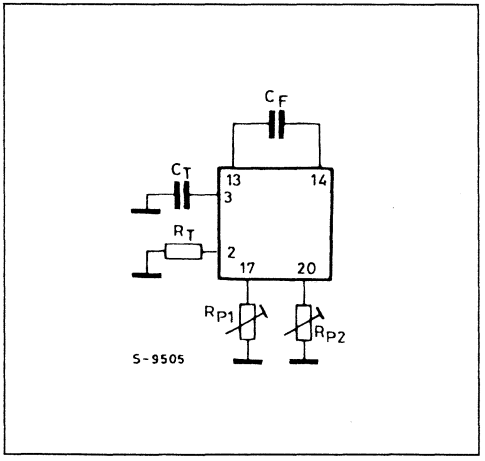
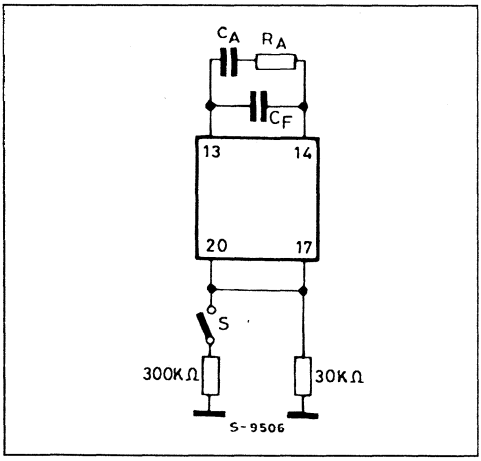


Figure 12.



PIN 14

Inverting input of main amplifier. In this pin the current reference programmed at pins 20, 17 is compared with the current from the monostable (stream of rectangular pulses).

In steady-state condition (constant motor speed) the values are equal and the capacitor C_F voltage is constant.

This means for the speed n (min 1) :

$$n = \frac{10.435}{C_T \, k \, R_p}$$

where "k" is the number of collector segments. (poles)

The non inverting input of the main amplifier is internally connected to a reference voltage (2.3 V).

PIN 15

Ground.

PIN 16

Ground.

PIN 17

Left speed adjustment. The voltage at this pin is fixed to a reference value of 0.8 V. A resistor from this pin and ground (fig. 14) fixes the reference current which will be compared with the medium output current of the monostable in order to fix the speed of the motor at the programmed value. The correct value of R_p would be :

$$R_p = \frac{10.435}{CT \cdot k \cdot n} = \quad \begin{matrix} n = \text{motor speed, (min 1)} \\ k = \text{poles number} \end{matrix}$$

The control of speed can be done in different way :

- speed separately programmed in two senses of rotation (fig. 14-15) ;
- only one speed for the two senses of rotation (fig. 16) ;
- speeds of the two senses a bit different (i.e. for compensating different pulley effects) (fig. 17) ;
- speed programmed with a DC voltage (fig. 18) i.e. with DA converter ;
- fast forward, by putting a resistor. In this case it is necessary that also at the higher speed for the duty cycle to be significately less than 1 (see value of R_T, C_T on pin 2, pin 3 sections).

Fig. 19 shows the function controlled with a µP.

PIN 18

Right function control. The voltages applied to this pin and to pin 19 determine the function, as showed in the table.

The typical value of the threshold (L-H) is 1.2 V.

PIN 19

Left function control. (see pin 18 sect).

PIN 20

Right speed adjustment. (see pin 17 sect).

Figure 13.

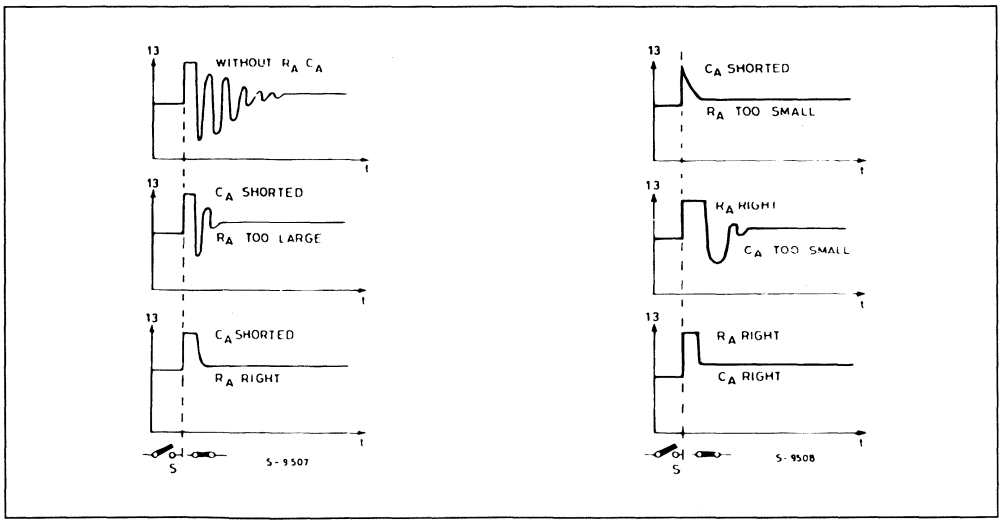


Figure 14.

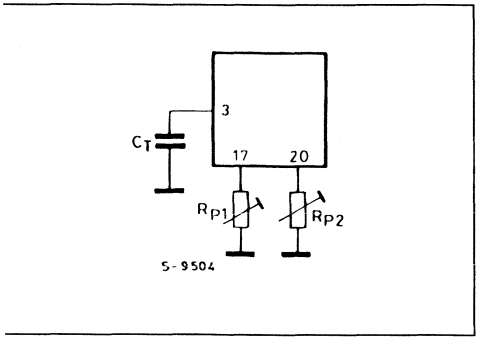


Figure 15.

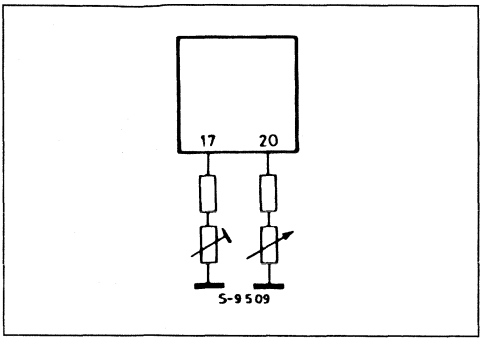


Figure 16.

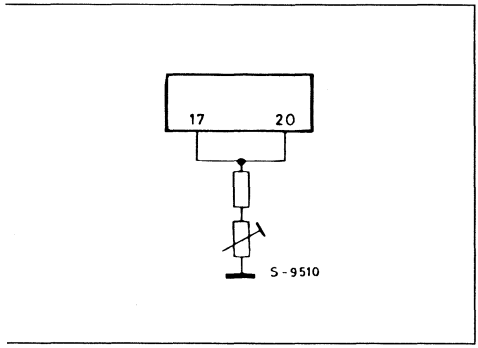


Figure 17.

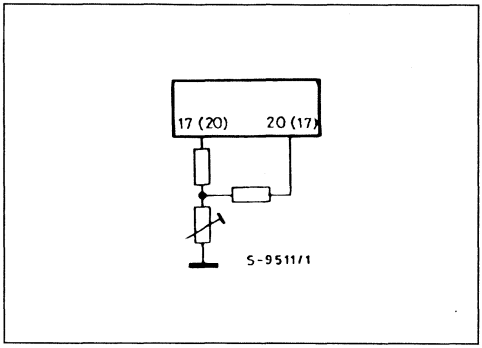


Figure 18.

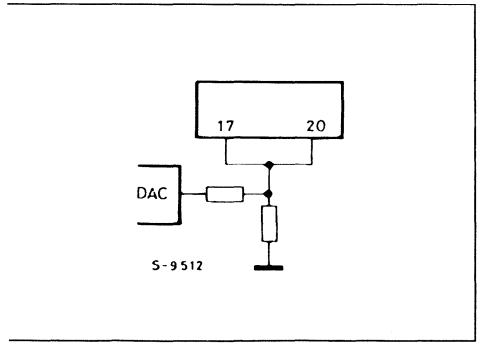
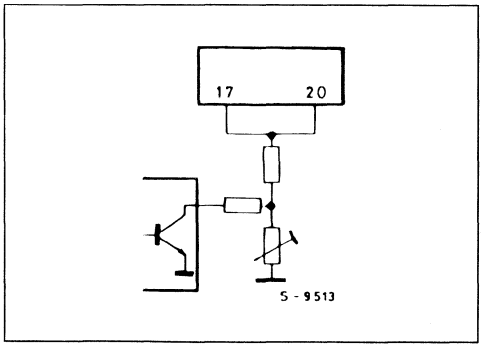


Figure 19.



Condition		Output Function	Output Voltage	
Pin 18	Pin 19		Pin 12	Pin 9
L	L	STOP	LOW	LOW
H	L	LEFT	LOW	REG
L	H	RIGHT	REG	LOW
H	H	OPEN	HIGH IMPEDANCE	

Figure 20 : Typical Application.

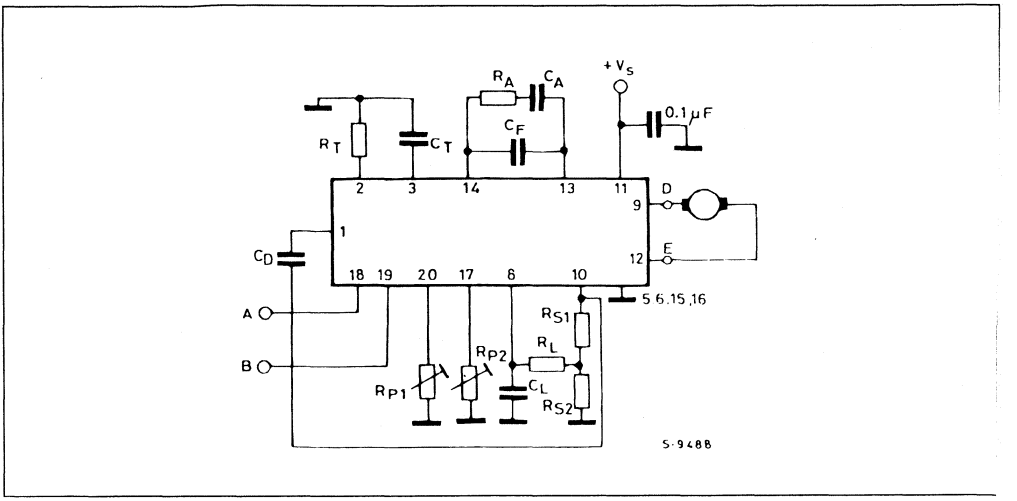


Figure 21 : Tacho Only Speed Regulation.

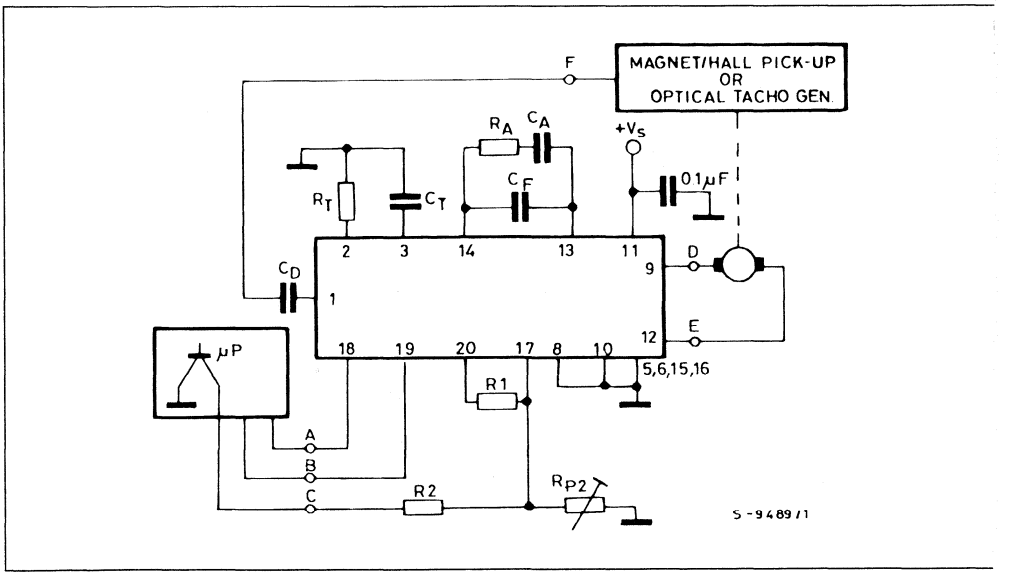


Figure 22 : One Direction Reg. of One Motor, or Alternatively of Two Motors.

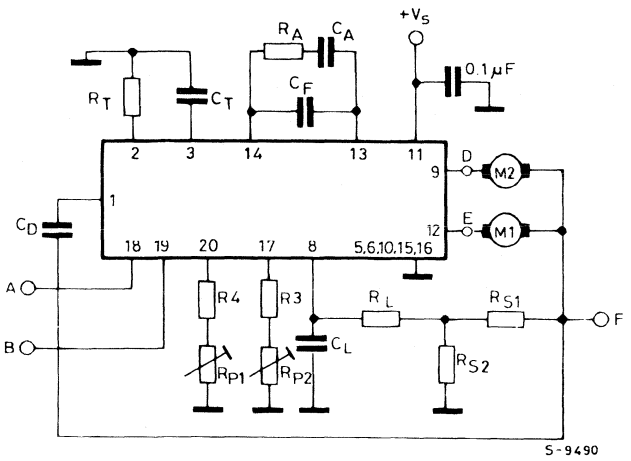
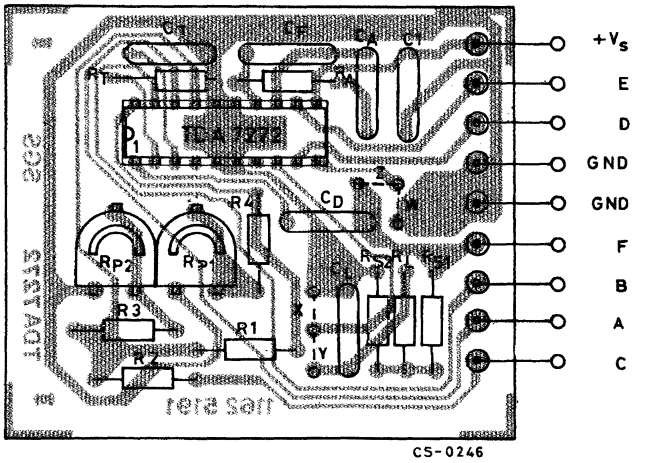


Figure 23 : P.C. Board and Components Layout of the Circuits of Figg. 20, 21, 22.



APPLICATION SUGGESTION (fig. 20, 21, 22) – (for a 2000 r.p.m. 3 pole DC motor with R_M = 16 Ω)

Comp.	Recommended Value	Purpose	If Larger	If Smaller	Allowed Range	
					Min.	Max.
R_{S1}	1Ω	Current sensing tacho loop.		Tacho loop do not regulate	0	
R_{S2}	1.5 Ω	Curr. sensing V/I loop.	Instability may occur.	Motor Regulator ; Undercompens.	0	$R_{MOT}/9$
R_L ; C_L	22 kΩ – 68 nF	Spike filtering.	Slow V/I Regulator Response.	High Output Ripple.		
C_D	68 nF	Pulse Transf.			33 nF	100 nF
R_T ; C_T	15 kΩ – 47 nF	Current source programming to obtain a 50 % duty cycle.			6 kΩ	30 kΩ
R_{P1} ; R_{P2}	47 kΩ trim.	Set of Speed.	Low Speed.	High Speed.	0	
C_F	Polyester 100 nF	Optimization of Integrator Ripple and Loop Response Time.	Low Ripple, Slower Tacho-regulator Response.	Higher Ripple, Faster Response.	10 nF	470 nF
R_A ; C_A	220 kΩ – 220 nF	Fast Response with no Overshoot.	Depending on electromechanical system.		10 kΩ 10 nF	10 MΩ 1 µF

Figure 24 : Speed Regulation Versus Supply Voltage (Circuit of Fig. 20).

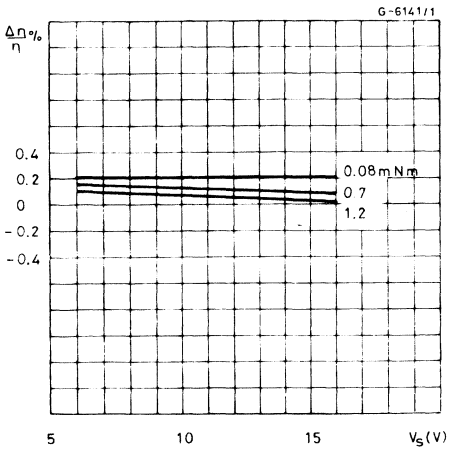


Figure 25 : High Current TDA7272 + 2 x L149 Application.

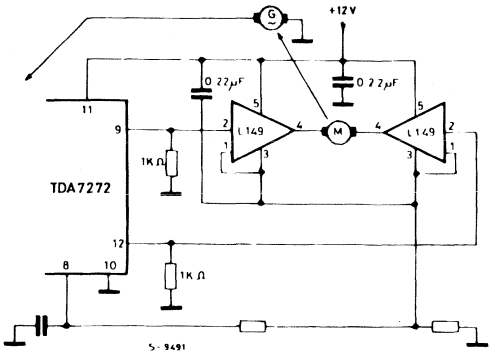
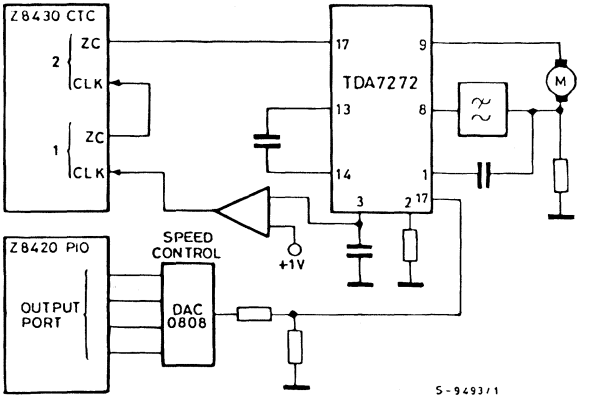


Figure 26 : In Connection with a Presettable Counter and I/O Peripheral the TDA7272 Controls the Speed through a D/A Converter.



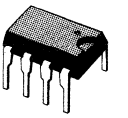
SGS-THOMSON MICROELECTRONICS

TDA7275A

MOTOR SPEED REGULATOR

ADVANCE DATA

- EXCELLENT VERSATILITY IN USE
- HIGH OUTPUT CURRENT (up to 1.5 A)
- LOW QUIESCENT CURRENT
- LOW REFERENCE VOLTAGE (1.32 V)
- EXCELLENT PARAMETERS STABILITY VERSUS AMBIENT TEMPERATURE
- START/STOP FUNCTION (TTL levels)
- DUMP PROTECTION



MINIDIP
(4 + 4)

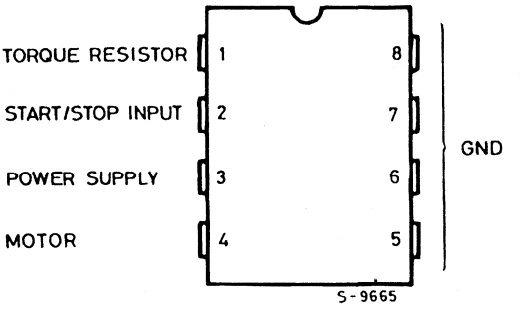
ORDER CODE : TDA7275A

DESCRIPTION

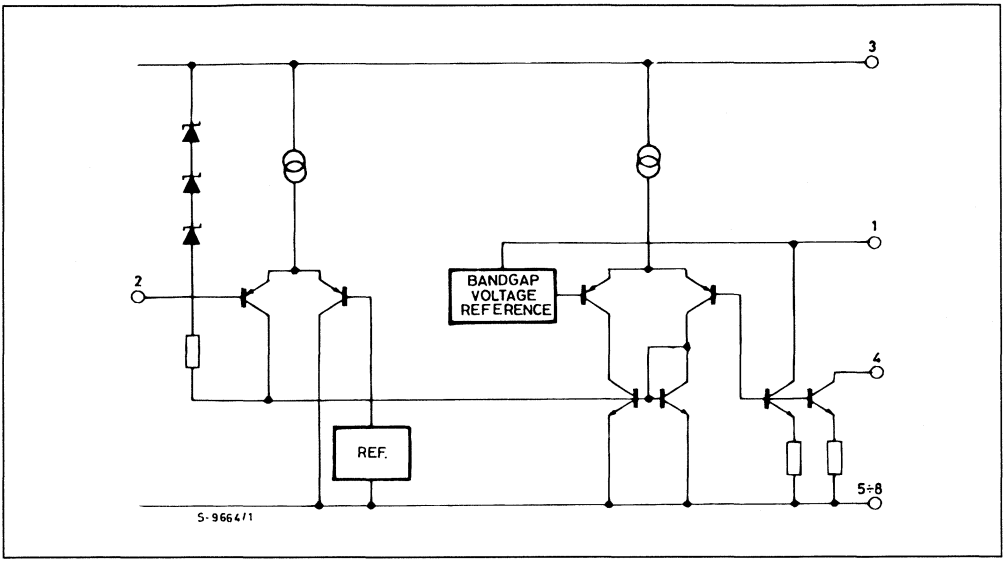
The TDA7275A is a linear integrated circuit in minidip plastic package. It is intended for use as speed regulator for DC motors of record players, tape and cassette recorders.

The dump protection make it particularly suitable for car radio applications.

PIN CONNECTIONS (top view)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	19	V
V_s	Peak Supply Voltage (for 50 ms)	45	V
I_M	Maximum Output Current	1.5	A
T_{op}	Operating Temperature Range	– 30 to 85	°C
P_{tot}	Total Power Dissipation T_{amb} = 70 °C T_{pins} = 70 °C	1 4	W W

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	20	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, V_s = 12 V unless otherwise specified, refer to test circuit)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage Range		8		18	V
V_{ref}	Reference Voltage	I_M = 0.1 A	1.05	1.22	1.35	V
$I_q + I_d$	Total Quiescent Current	I_M = 0.1 mA		2		mA
I_d	Quiescent Current	I_M = 0.1 mA		1		mA
I_{ms}	Starting Motor Current	$\frac{\Delta V_{ref}}{V_{ref}} = -50\ \%$	1			A
V_4	Saturation Voltage	I_M = 0.5 A		1.7	2	V
$K = I_M/I_T$	Reflection Coefficient	I_M = 0.1 A	18	20	22	
$\frac{\Delta K/\Delta V_s}{K}$		I_M = 0.1 A V_s = 8 V to 16 V		0.5		%/V
$\frac{\Delta K/\Delta I_M}{K}$		I_M = 25 to 200 mA		− 0.05		%/mA
$\frac{\Delta K/\Delta T}{K}$		I_M = 0.1 A T_{op} = − 30 to 85 °C		0.02		%/°C
$\frac{\Delta V_{ref}/\Delta V_s}{V_{ref}}$	Line Regulation	V_s = 8 V to 16 V I_M = 0.1 A		0.04		%/V
$\frac{\Delta V_{ref}/\Delta I_M}{V_{ref}}$	Load Regulation	I_M = 25 to 200 mA		− 0.01		%/mA
$\frac{\Delta V_{ref}/\Delta T}{V_{ref}}$	Temperature Coefficient	I_M = 0.1 A T_{op} = − 30 to 85 °C		0.02		%/°C
V_2	Motor "Stop" (acc. following data or grounded)			1		V
I_2	Motor "Stop"	V_2 = 1 V		− 0.05		mA
V_2	Motor "Run" (acc. following data or open)			1.5		V
I_2	Motor "Run"	V_2 = 1.5 V		− 0.1		mA

Figure 1 : Test Circuit.

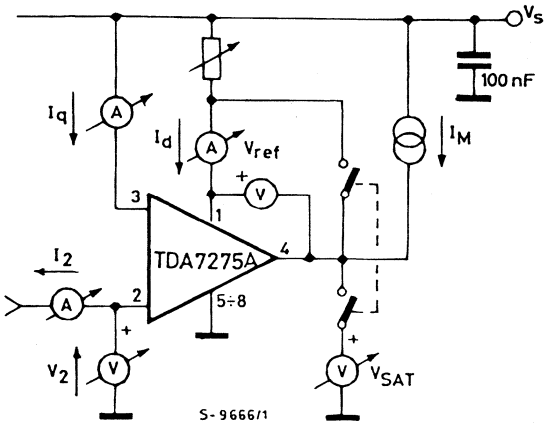
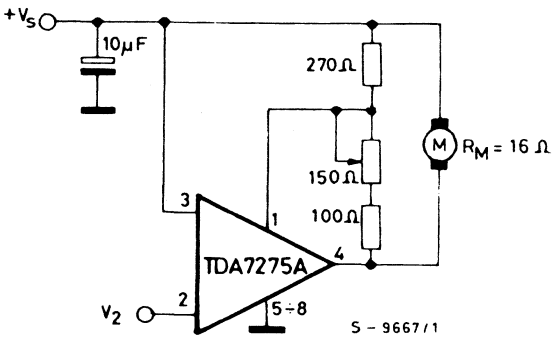


Figure 2 : Application Circuit.



– $R_{Ttyp.} = K_{typ.} R_{Mtyp.}$ if $R_T > K_{min} R_{Mmin}$ instability may accur.

– A diode across the motor could be necessary with certain kind of motor.

Figure 3 : Quiescent Current vs. Supply voltage.

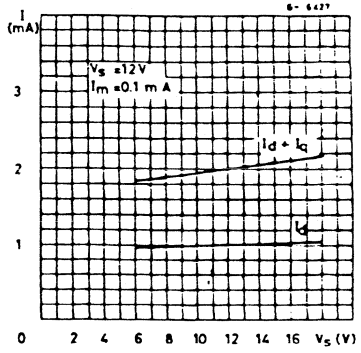


Figure 4 : Speed Variation vs. Supply Voltage.

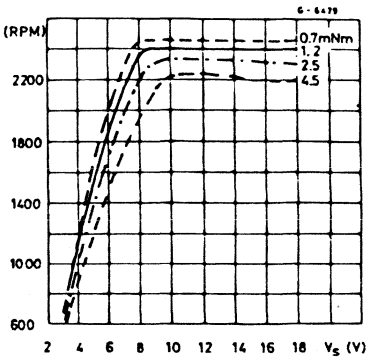
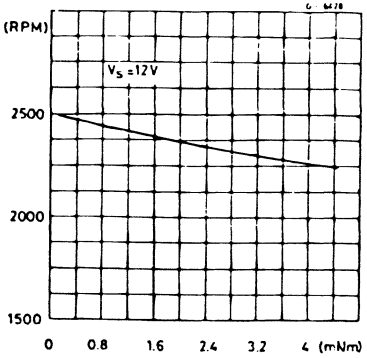


Figure 5 : Speed Variation vs. Torque (V_S = 12 V).



SGS-THOMSON MICROELECTRONICS

M5450
M5451

LED DISPLAY DRIVERS

- M5450 34 OUTPUTS/15mA SINK
- M5451 35 OUTPUTS/15mA SINK
- CURRENT GENERATOR OUTPUTS (NO EXTERNAL RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- ENABLE (ON M5450)
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

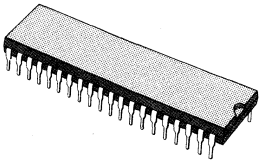
Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5450 and M5451 are monolithic MOS integrated circuits produced with an N-channel silicon gate technology. They are available in 40-pin dual in-line plastic packages.

A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD} or to a separate supply of 13.2V maximum.

The M5450 and M5451 are pin-to-pin replacements of the NS MM 5450 and MM 5451.



DIP-40 Plastic

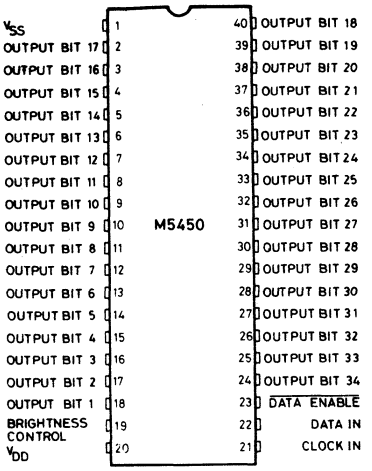
ORDERING NUMBERS: M5450 B7
M5451 B7

ABSOLUTE MAXIMUM RATINGS

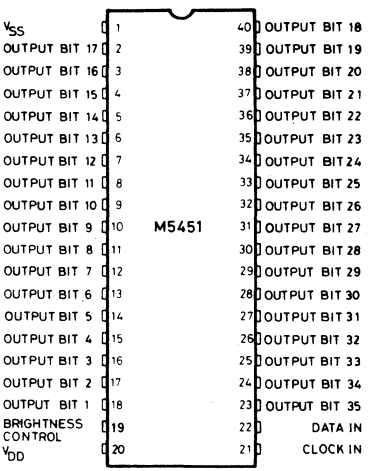
V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1W
		at 85°C	560 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAMS



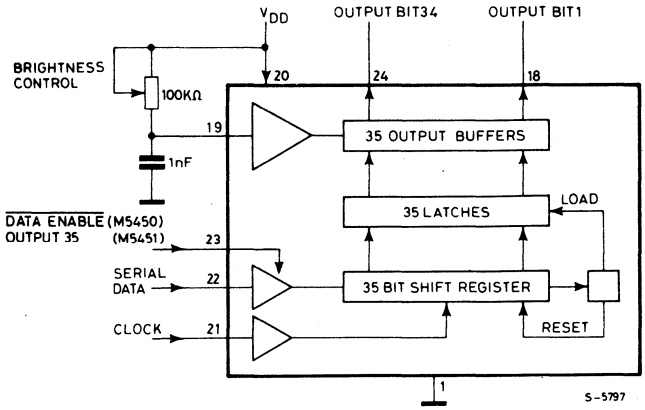
S-5795



S-5796

BLOCK DIAGRAM

Fig. 1



S-5797

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltage Logical "0" Level Logical "1" Level	± 10 µA input bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 19)	Input current = 750 µA	3		4.3	V
$V_{O(off)}$	Off State Out. Voltage				13.2	V
I_O	Out. Sink Current (note 3) Segment OFF Segment ON Brightness In. = 0 µA Brightness In. = 100 µA Brightness In. = 750 µA	 V_O = 3V V_O = 1V (note 4)	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes : 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.

2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.

3. Absolute maximum for each output should be limited to 40 mA.

4. The V_O voltage should be regulated by the user. See figures 5 and 6 for allowable V_O versus I_O operation.

FUNCTIONAL DESCRIPTION

Both the M5450 and the M5451 are specifically designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current LED displays.
A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.
A block diagram is shown in figure 1. For the M5450 a $\overline{\text{DATA ENABLE}}$ is used instead of the 35th output. The $\overline{\text{DATA ENABLE}}$ input is a metal option for the M5450.

FUNCTIONAL DESCRIPTION (continued)

The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.
Figure 3 shows the timing relationship between Data, Clock and $\overline{\text{DATA ENABLE}}$.
A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j = [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + (V_{DD} \cdot 7\ \text{mA})\ ]\ (124\ °C/W) + T_{amb}$$

where:

T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
124°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

The above equation was used to plot figure 4, 5 and 6.

Fig. 2 - Input Data Format

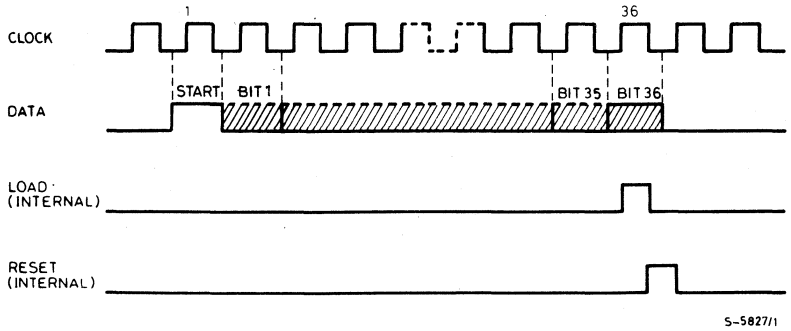


Fig. 3

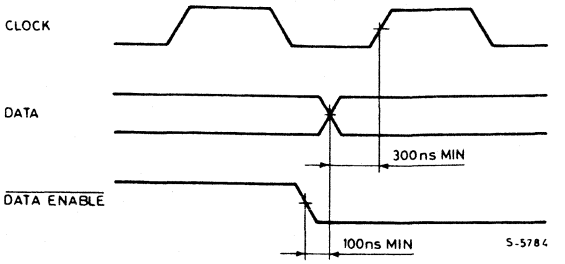


Fig. 4

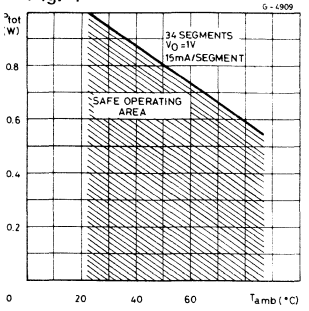


Fig. 5

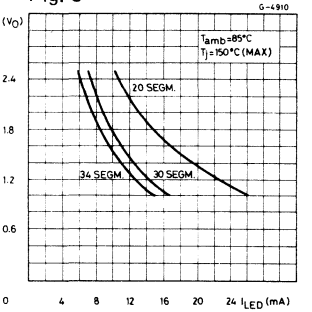
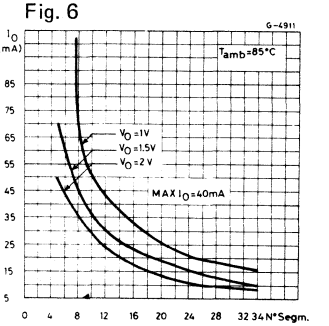
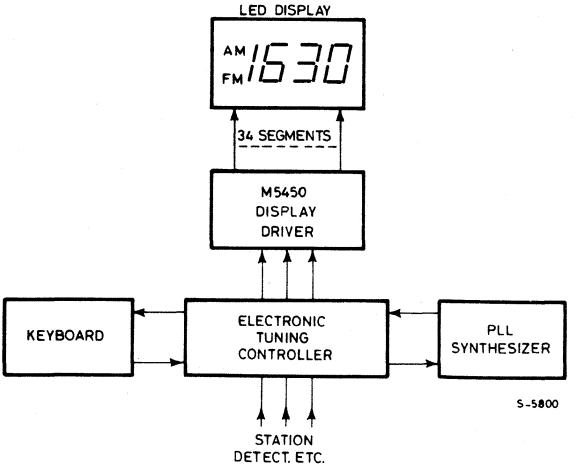


Fig. 6



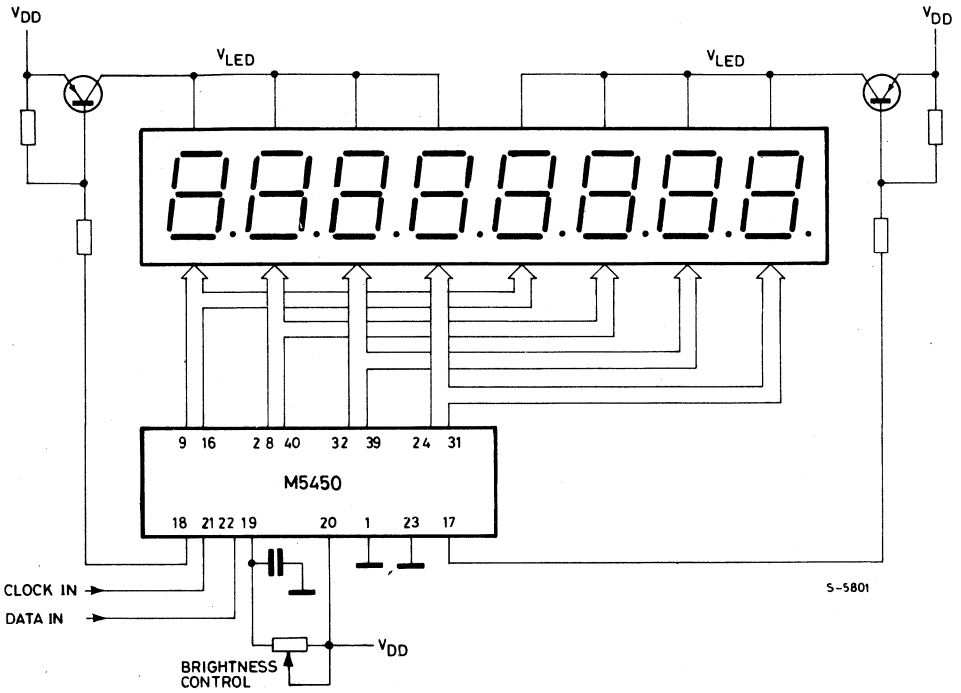
TYPICAL APPLICATIONS

Basic electronically tuned Radio or TV system



TYPICAL APPLICATIONS (continued)

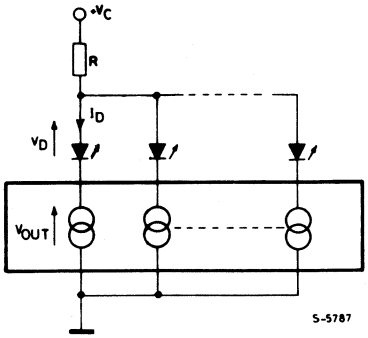
Duplexing 8 Digits with One M5450



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

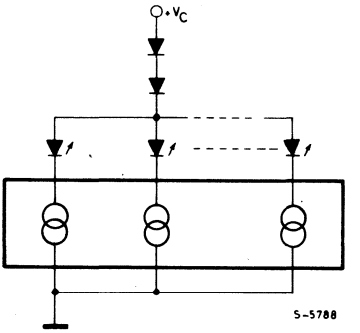


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

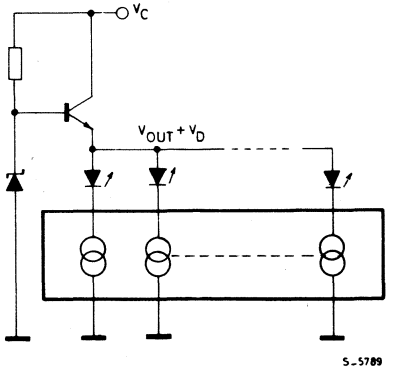
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

SGS-THOMSON MICROELECTRONICS

M5480

LED DISPLAY DRIVER

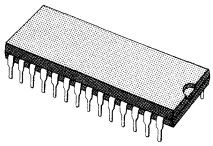
- 3½ DIGIT LED DRIVER (23 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- NO LOAD SIGNAL REQUIRED
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Applications examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATION
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5480 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5451 die packaged in a 28-pin plastic package making it ideal for a 3½ digit dispaly. A single pin controls the LED dispaly brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5480 is a pin-to-pin replacement of the NS MM 5480.



DIP-28 Plastic

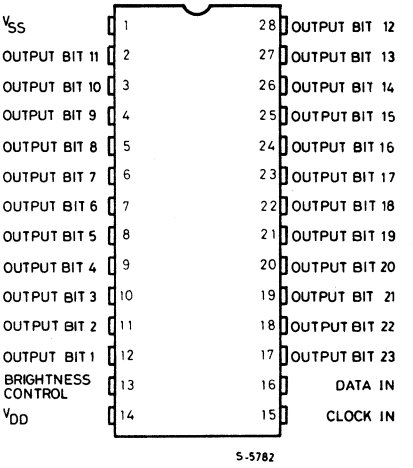
ORDERING NUMBER: M5480 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	940 mW
		at 85°C	490 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

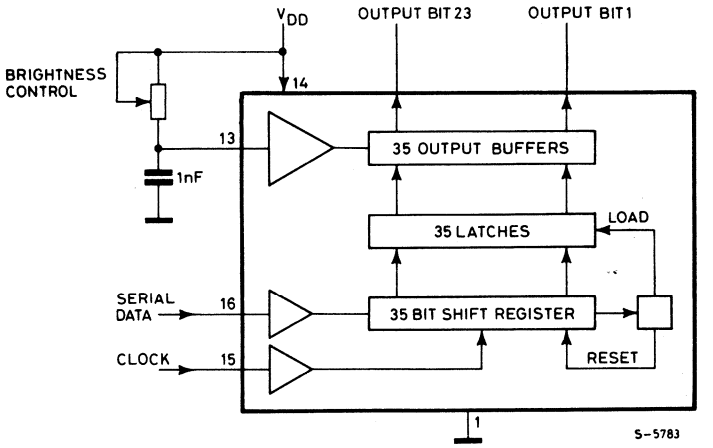
Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 µA Input Bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 13)	Input Current = 750 µA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage			13.2	18	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 µA Brightness In. = 100 µA Brightness In. = 750 µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5480 is specifically designed to operate $3\frac{1}{2}$ digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor.
There is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, and Clock. A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the 5480. Because it uses only 23 of the possible 35 outputs, 12 of the bits are "Don't Care".

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j = [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ mA\ ]\ (132\ °C/W) + T_{amb}$$

where:

T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
132°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Fig. 2 - Input Data Format

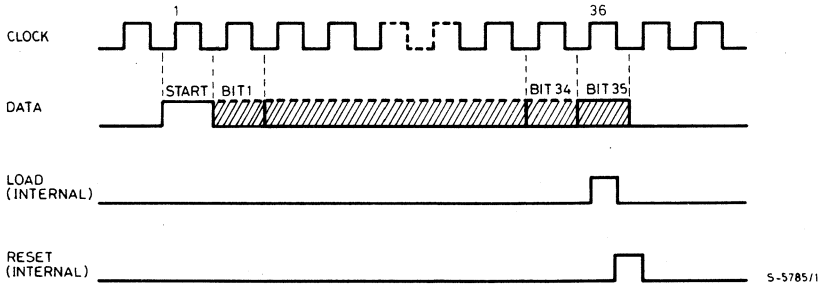


Fig. 3

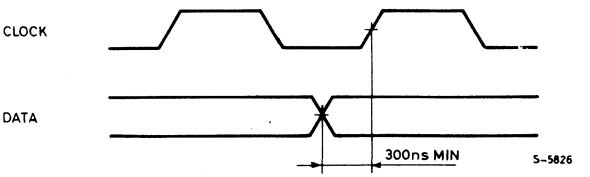
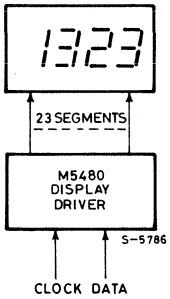


Fig. 4 - Serial Data Bus/Outputs Correspondence

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5480	X	23	22	21	20	19	X	X	18	X	17	16	15	14	13	12	X	X	X	X	11	10	9	8	X	X	X	7	6	5	4	3	2	1	X	START

TYPICAL APPLICATION

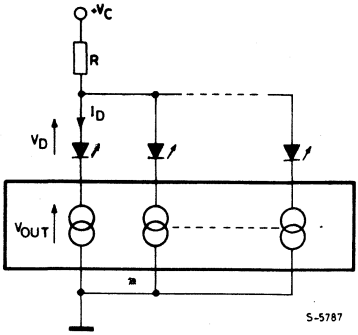
BASIC $3^1/_2$ Digit interface.



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

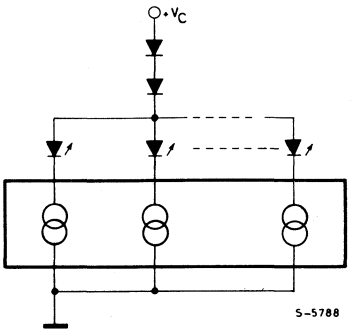


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{OUT\,MIN}}{N_{MAX} \cdot I_D}$$

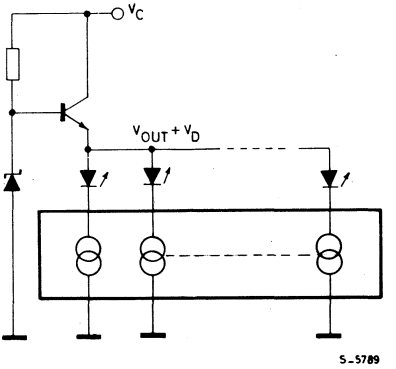
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)



In this configuration $V_{OUT}+V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

SGS-THOMSON MICROELECTRONICS

M5481

LED DISPLAY DRIVER

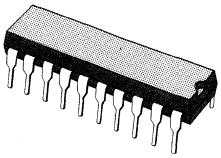
- 2 DIGIT LED DRIVER (14 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- DATA ENABLE
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5481 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5481 is a pin-to-pin replacement of the NS MM 5481.



DIP-20 Plastic (0.25)

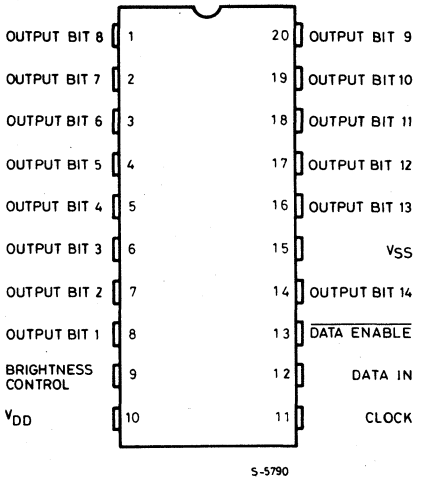
ORDERING NUMBER: M5481 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O\,(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1.5W
		at 85°C	800 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

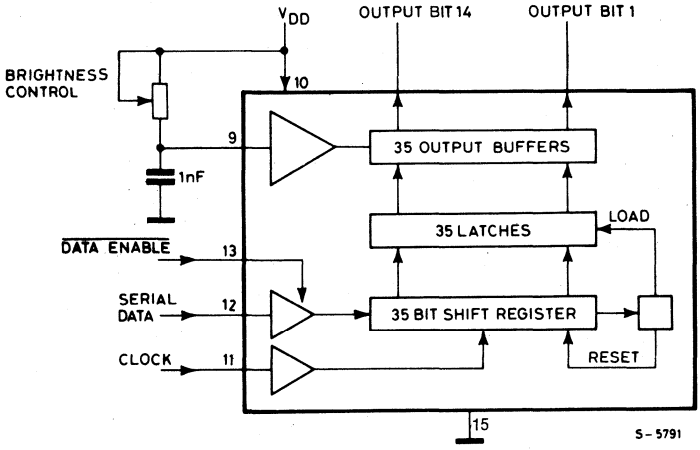
Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages					
	Logical "0" Level	± 10 μA Input Bias	-0.3		0.8	V
	Logical "1" Level	4.75 ⩽ V_{DD} ⩽ 5.25	2.2		V_{DD}	V
		V_{DD} > 5.25	V_{DD}-2		V_{DD}	V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3)					
	Segment OFF	V_O = 3V			10	μA
	Segment ON	V_O = 1V (note 4)				
		Brightness In. = 0 μA	0		10	μA
		Brightness In. = 100 μA	2	2.7	4	mA
		Brightness In. = 750 μA	12	15	25	mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculates as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5481 uses the M5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.
The 35 data bits are latched after the 36th bit is complete, thus providing non--multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.
These is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, Clock and $\overline{\text{DATA ENABLE}}$.
A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5481. Because it uses only 14 of the possible 35 outputs, 21 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j \equiv [\,(V_{OUT})\,(I_{LED})\,(\text{No. of segments}) + V_{DD} \cdot 7\ \text{mA}\,]\ (80\ °C/W) + T_{amb}$$

where:

T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
80°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Fig. 2 - Input Data Format

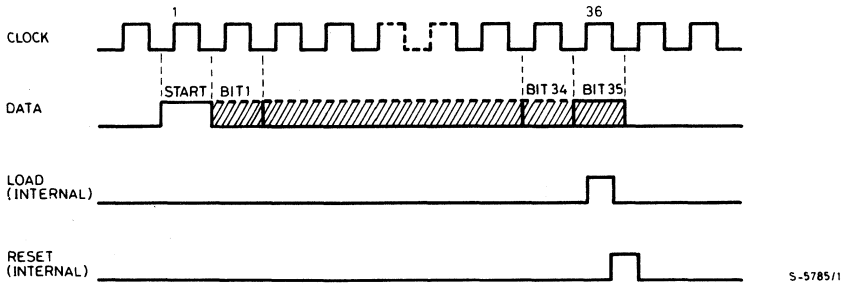


Fig. 3

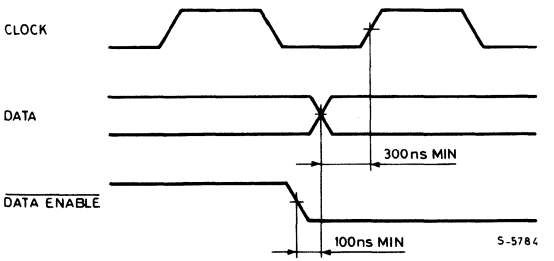
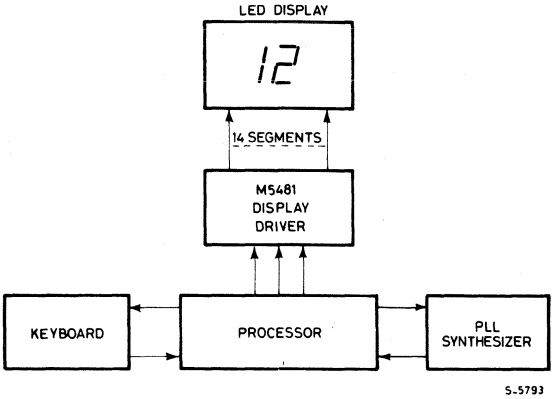


Fig. 4 - Serial Data Bus/Outputs Correspondence

5450	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5481	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

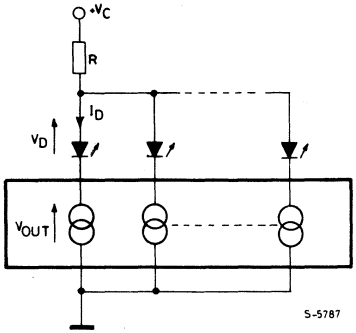
BASIC electronically tuned TV system



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

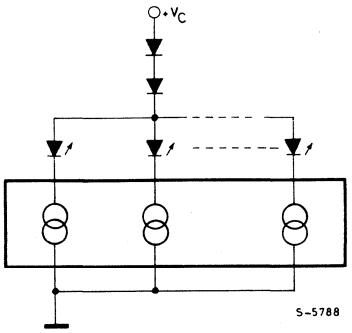


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

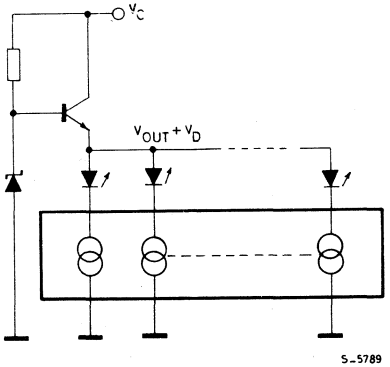
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)



In this configuration $V_{OUT}+V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

SGS-THOMSON MICROELECTRONICS

M5482

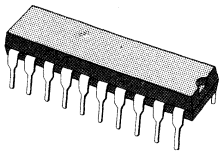
LED DISPLAY DRIVER

- 2 DIGIT LED DRIVER (15 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5482 is a monolithic MOS integrated circuit produced with an N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.



DIP-20 Plastic
(0.25)

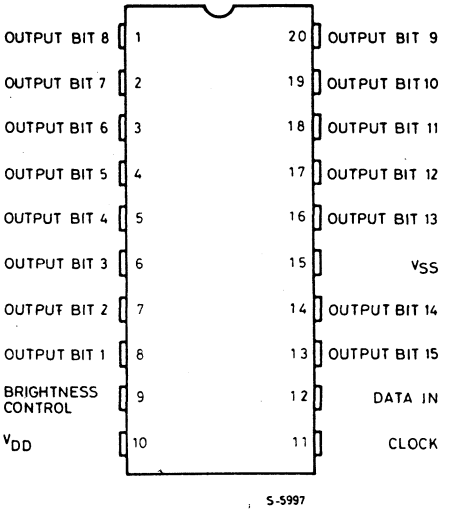
ORDERING NUMBER: M5482 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O\,(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1.5W
		at 85°C	800 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

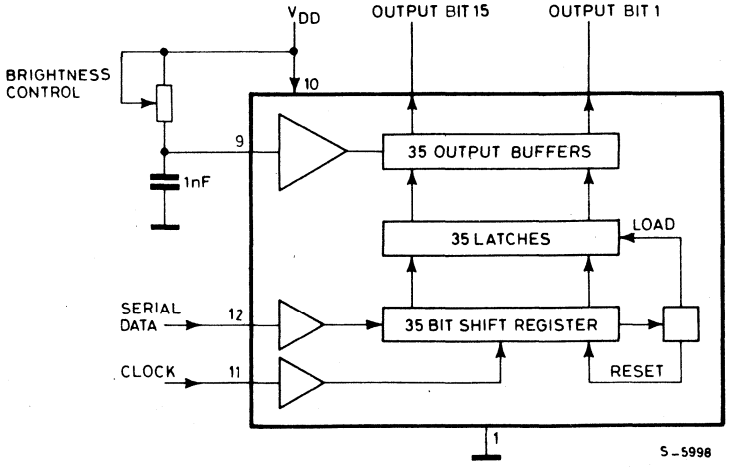
Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 µA Input Bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 µA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 µA Brightness In. = 100 µA Brightness In. = 750 µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes:
1. Output matching is calculated as the percent variation from I_{MAX} + I_{MIN}/2.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5482 uses the M5451 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.
There is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data and Clock.
A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5482. Because it uses only 15 of the possible 35 outputs, 20 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j \equiv [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ mA\ ]\ (80\ °C/W) + T_{amb}$$

where:

T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
80°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Fig. 2 - Input Data Format

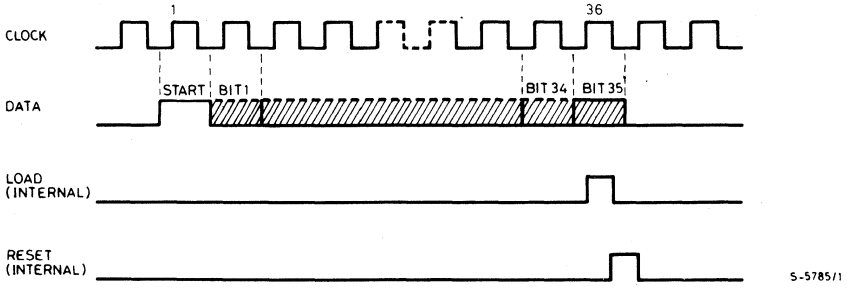


Fig. 3

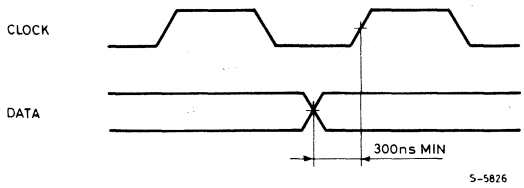
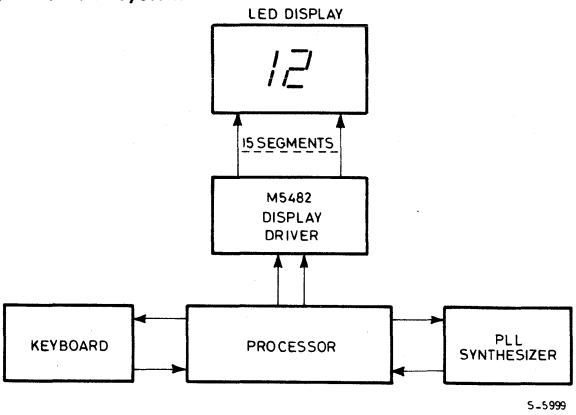


Fig. 4 - Serial Data Bus/Outputs Correspondence

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5482	15	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

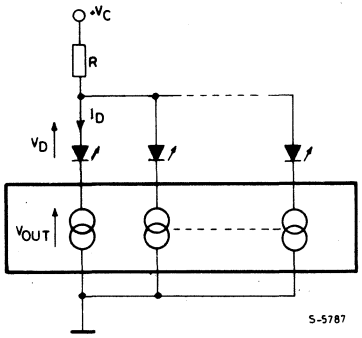
BASIC electronically tuned TV system



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

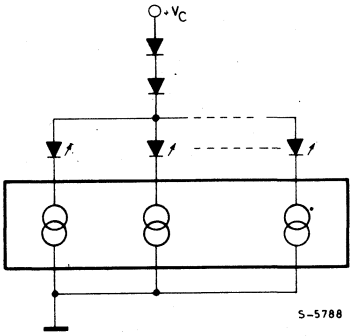


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

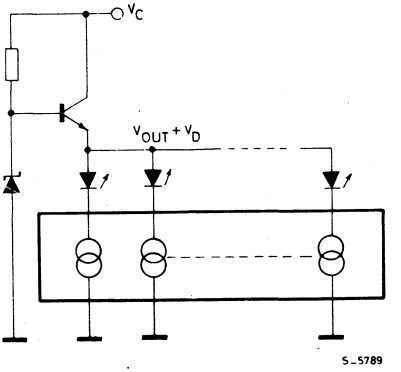
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)

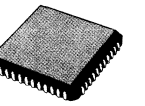


In this configuration $V_{OUT}+V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

SERIAL INPUT LCD DRIVER

- DRIVES UP TO 32 LCD SEGMENTS
- DATA TRANSFER : FIXED ENABLE MODE FOR DIP-40, ENABLE AND LATCH-MODE FOR 44PLCC
- INPUTS ARE CMOS, NMOS AND TTL COMPATIBLE
- CASCADABLE
- REQUIRES ONLY 3 CONTROL LINES
- ON CHIP OSCILLATOR
- CMOS TECHNOLOGY FOR WIDE SUPPLY VOLTAGE RANGE
- – 40 TO 85 °C TEMPERATURE RANGE

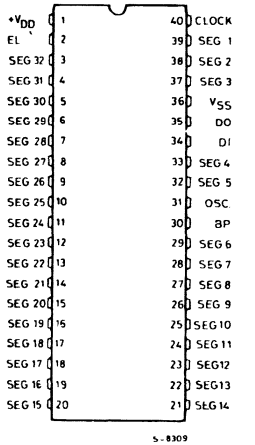
B
DIP-40
(Plastic)



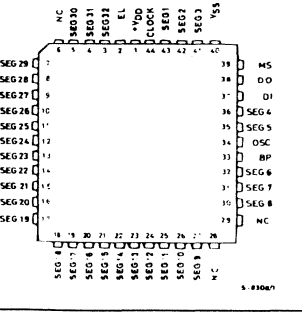
C
44 PLCC
(Plastic Chip Carrier)

ORDER CODE : M8438A DIE 1
M8438A B6
M8438A C6

PIN CONNECTIONS



S-8309



S-8308/1

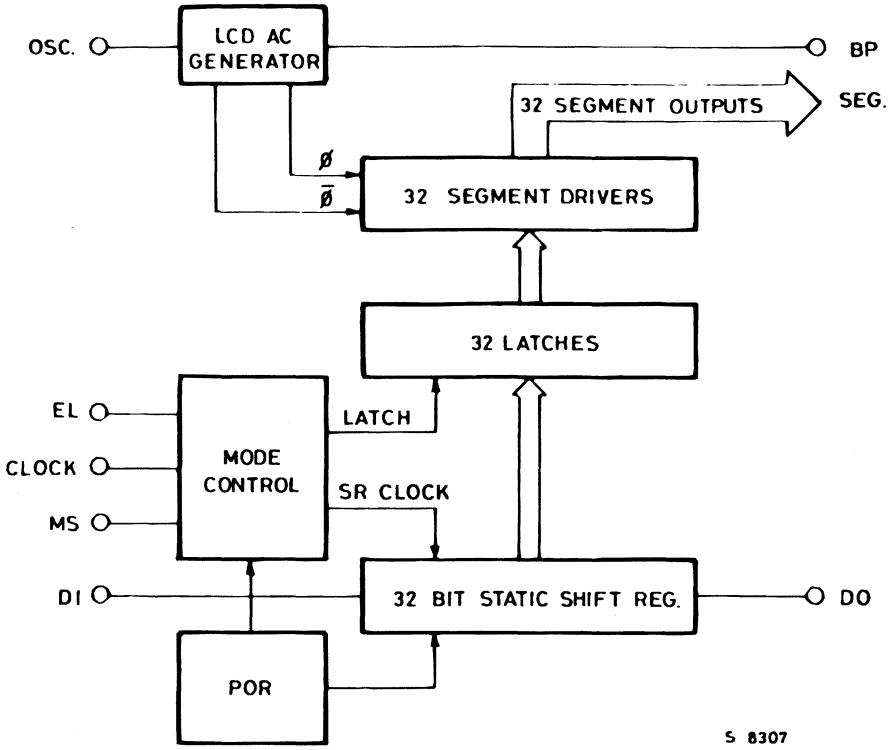
DESCRIPTION

The M8438A is a CMOS integrated circuit that drives an LCD display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.

The M8438A can drive any standard or custom parallel drive LCD whether it be field effect or dynamic scattering. Several drivers can be cascaded, if more than 32 segments are to be driven. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the OSC input which determines the frequency of an internal oscillator.

The M8438A is available in DIE form and assembled in 40 pin dual-in line plastic or 44 PLCC packages.

BLOCK DIAGRAM



OSC : Oscillator (capacitor or drive signal)
EL : Enable / Latch control input
MS : Mode select input (not available in 40 Pin DIL)
DI : Serial data input

DO : Serial data output
BP : Backplane output
SEG : Segment output signal

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$(V_{DD}-V_{SS})$	Supply Voltage	– 0.3 to + 12	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
P_D	Power Dissipation	250	mW
T_{stg}	Storage Temperature	– 55 to + 125	°C
T_A	Operating Temperature	– 40 to + 85	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
STATIC ELECTRICAL CHARACTERISTICS					
V_{DD}	Supply Voltage		3	10	V
I_{DD}	Supply Current	Oscillator f < 15 kHz		60	µA
I_Q	Quiescent Current	V_{DD} = 10 V		10	µA
V_{IH}	Input High Level		.5 V_{DD}	V_{DD}	V
V_{IL}	Input Low Level (CLOCK, DI, EL)		0	.2 V_{DD}	V
I_{IN}	Input Current (CLOCK, DI, EL)			± 5	µA
C_I	Input Capacitance			5	pF
V_{IH}	Input High Level	Driven Mode	.9 V_{DD}		V
V_{IL}	Input Low Level (OSC)	Driven Mode		.1 V_{DD}	V
I_{IN}	Input Current (OSC)	Driven Mode		± 10	µA
R_{ON}	Segment Output Impedance	I_{IL}= 10 µA		40	kΩ
R_{ON}	Backplane Output Impedance	I_L = 100 µA		3	kΩ
V_{OFF}	Output Offset Voltage	C_L = 250 pF between Each SEG Output and BP		± 50	mV
R_{ON}	Data Output Impedance	I_L = 100 µA		3	kΩ
DYNAMIC ELECTRICAL CHARACTERISTICS					
t_{TR}	Transition Time OSC	Driven Mode		500	ns
t_{SD}	Data Set-up Time	Fig. 1 and 2	150		ns
t_{HD}	Data Hold Time	Fig. 1 and 2	50		ns
t_{SE}	EL Set-up Time	Fig. 1	100		ns
t_{HE}	EL Hold Time	Fig. 1	100		ns
t_{WE}	EL Pulse Width	Fig. 2	175		ns
t_{CE}	Clock to EL Time	Fig. 2	250		ns
t_{pd}	DO Propagation Delay	Fig. 1, 2 ; C_L = 55 pF		500	ns
f	Clock Rate	V_{DD} = 10 50 % Duty Cycle ;	DC	1.5	MHz

FONCTIONAL DESCRIPTION

LCD-AC-Generator

This block generates a 50 % duty cycle signal for the backplane output. The circuit can be used in two different modes : oscillator or driven.

OSCILLATOR MODE : In this mode the backplane frequency is determined by the internal RC oscillator together with an 8-stage frequency divider. For generating the backplane output signal of 50 % duty cycle the oscillator frequency is divided by 256. The RC oscillator requires an external capacitor to be connected between input OSC and V_{SS}. A value of 18 pF gives a backplane frequency of 80 Hz ± 30 % at V_{DD} = 5 V. The variation of the backplane frequency over the entire temperature and supply voltage range is ± 50 %.

DRIVEN MODE : In this mode the signal at the backplane output BP is in phase with an external driving signal applied to input OSC. This mode is used to synchronize the LCD drive of two or more cascaded driver circuits.

DETECTION LOGIC The circuit is able to distinguish between the conditions for oscillator or driven mode. If the circuit is to be in the oscillator mode, the OSC pin has a capacitor connected to it. The oscillator will start as soon as the supply voltage exceed a certain minimum value. The signal at pin OSC swings within a range from 0.3 V_{DD} to 0.7 V_{DD}. If the circuit is to be in the driven mode, the OSC pin has to be forced to logic levels by an external source. The transition time between the logic levels must be short, so that the circuit does not react on the voltage level in between. In the driven mode the 8-stage frequency divider is by-passed.

Segment outputs

A logic 0 at the data input DI causes a segment output signal to be in phase with the backplane signal and turns the segment off. A logic 1 causes a segment output to be in opposite phase to the backplane signal and turns the segment on.

Microprocessor interface

The circuit can operate in two different data transfer modes : Enable mode and latch mode. One of either mode can be chosen with the mode select input MS. An internal pull up device is provided between this input and V_{DD}. Enable mode is selected if MS is left open or connected to V_{DD}.

Latch mode is selected if MS is connected to V_{SS}. **The input MS is not available, if the device is assembled in the 40 pin package, and is internally fixed to operate in ENABLE MODE.**

ENABLE MODE Fig. 3 shows a timing diagram of the enable mode. Data is serially shifted in and out of the shift register on the negative transition of the clock. Serial entry into the shift register is permitted when the enable/latch control EL is high. When EL is low it causes the shift register clock to be inhibited and the content of the shift register to be loaded into the latches that control the segment drivers.

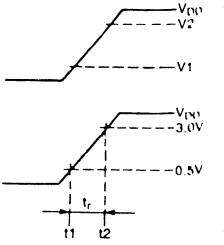
LATCH MODE Fig. 4 shows a timing diagram of the latch mode. Data is serially shifted in and out of the shift register on the negative transition of the clock. Serial entry into the shift register is permitted independently of the enable/latch control EL. When EL is high it causes a parallel load of the content in the shift register into the latches. It is acceptable to lie the EL line high. Then the latches are transparent and only two lines, clock and data input, would then be needed for data transfer.

Power-on logic

A power on reset pulse is generated internally when the supply voltage is being turned on. The generation of the reset pulse is level dependent and will occur even on a slowly rising supply voltage. The power on reset pulse resets all shift register stages and the latches that control the segment drivers. Therefore all segment outputs are initially in phase with the backplane output. This causes the display to be blanked and no arbitrary data to show up. This condition is maintained until data is shifted into the register and loaded into the latches.

CONDITIONS FOR POWER-ON RESET FUNCTION ; The POR circuit triggers on the rising slope of the positive supply voltage V_{DD}. A reset pulse will be generated, if conditions a) through d) are given :

a) Level
Rising slope from
V1 to V2
V1 max = 0.5 V
V2 min = 3.0 V



b) Rise time
t_r min = 10 µs
t_r max = 1 s

c) Rise function
The function of V_{DD} between t1 and t2 may be nonlinear, but should not show a maximum and should not exceed 0.25 V/µs.

d) Recovery time
The minimum time between turn-off and turn-on of V_{DD} is 1 s.

FONCTIONAL DESCRIPTION (continued)

Cascade configuration

Several LCD drivers can be cascaded if a liquid crystal display with more than 32 segments is to be connected.

The phase correlation between all segment outputs is achieved by using the second (and any other) device in the driven mode.

Two different cascade configurations can be chosen depending whether the LCD frequency is to be determined by the internal RC oscillator or by an external signal.

Figure 3 shows the connection scheme for a self oscillating configuration, figure 4 shows the connection of an externally controlled one.

Figure 1 : Timing Diagram of Enable Mode : Set-up and Hold Time.

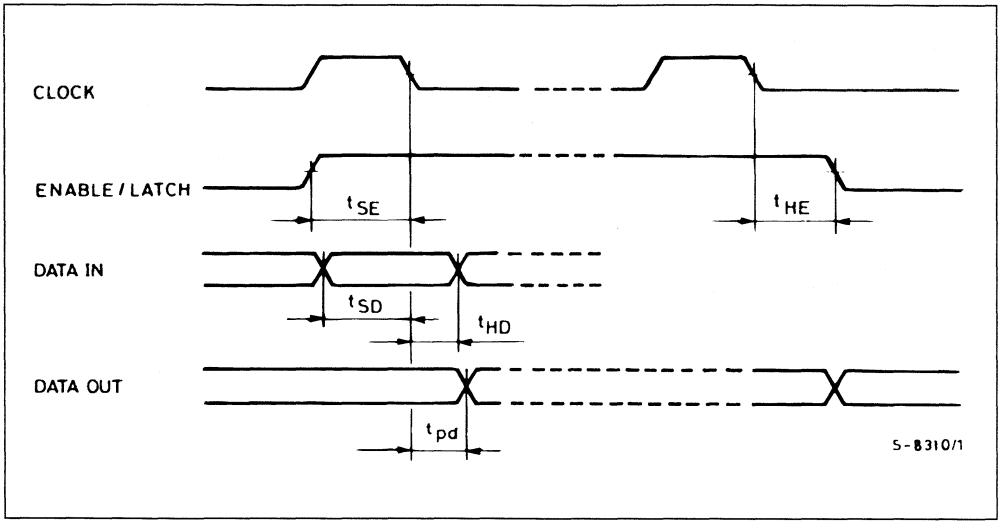


Figure 2 : Timing Diagram of Latch Mode : Set-up and Hold Time.

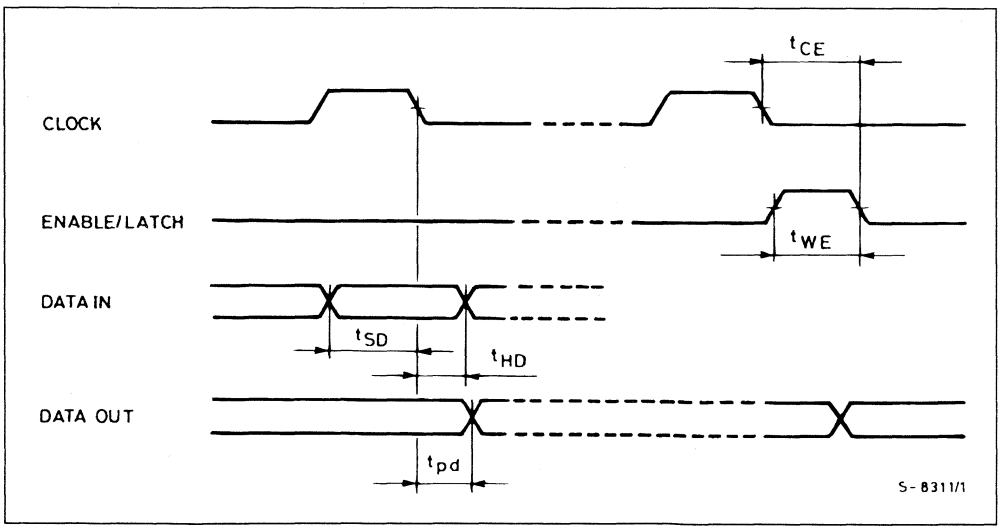


Figure 3 : Timing Diagram of Enable Mode : Serial Load into SR and Parallel Transfer to LCD.

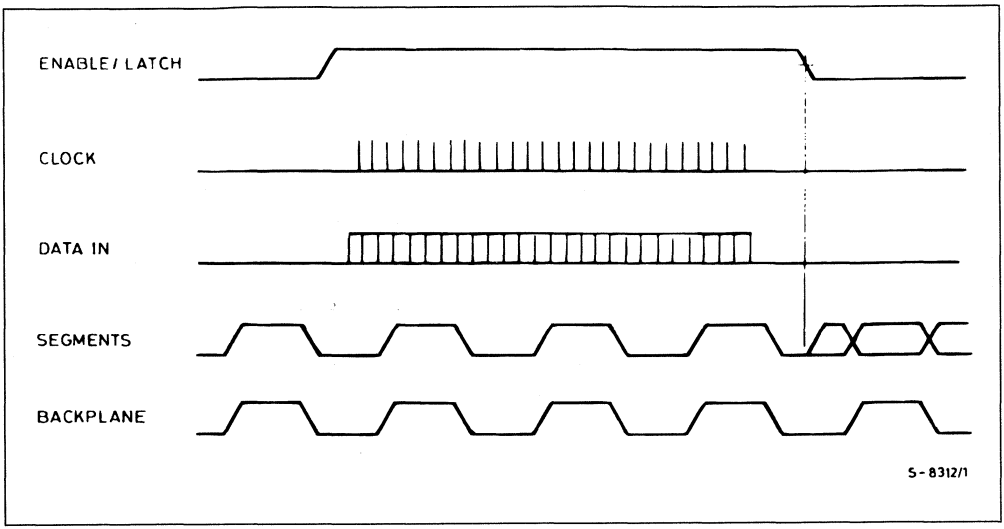


Figure 4 : Timing Diagram of Latch Mode : Serial Load into SR and Parallel Transfer to LCD.

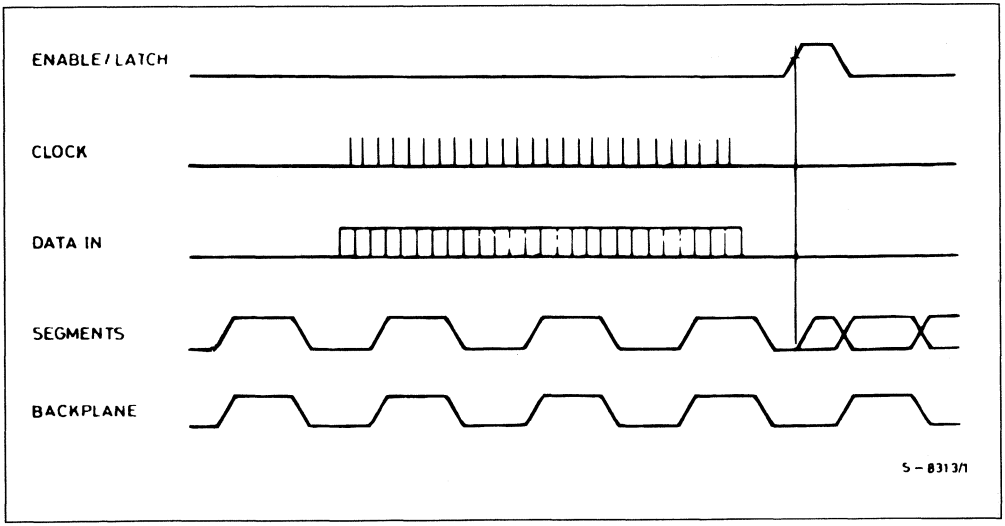


Figure 5 : Cascade Configuration, Self Oscillating.

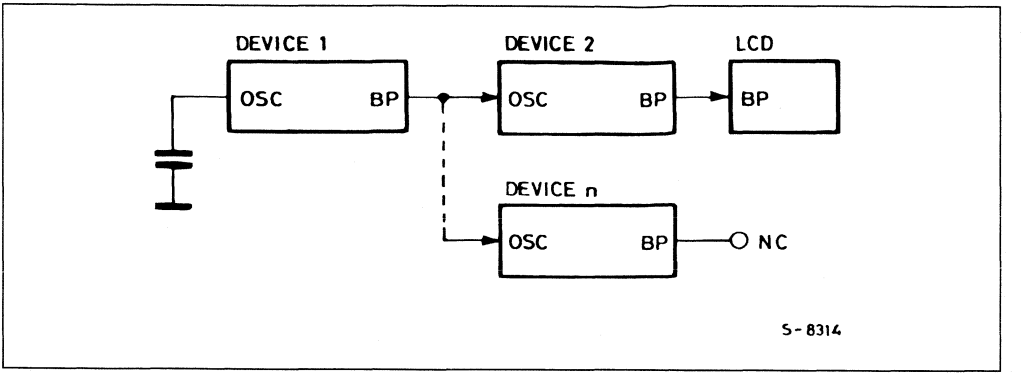
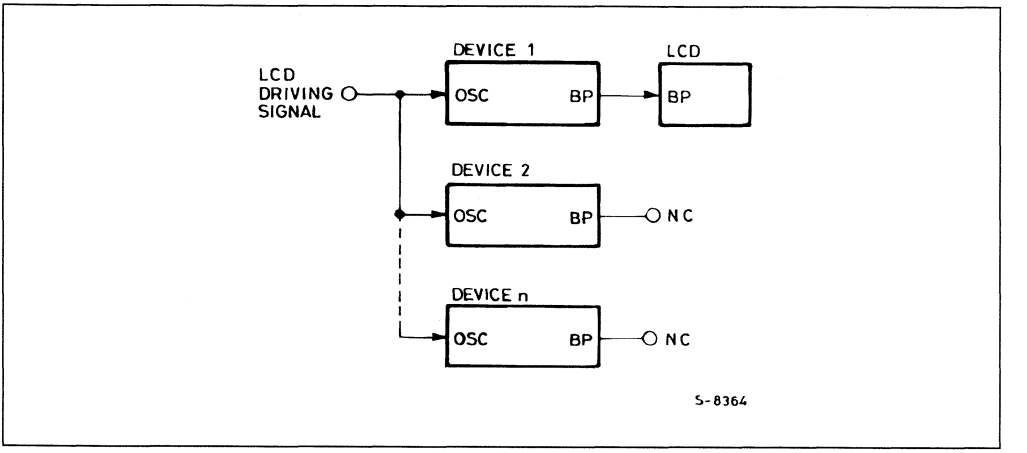


Figure 6 : Cascade Configuration, Drive by External Signal.

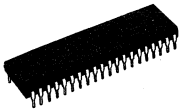


SGS-THOMSON MICROELECTRONICS

M8439

SERIAL INPUT LCD DRIVER

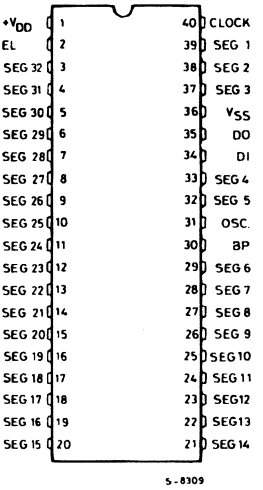
- DRIVES UP TO 32 LCD SEGMENTS
- DATA TRANSFER : LATCH MODE
- INPUTS ARE CMOS, NMOS AND TTL COMPATIBLE
- CASCADABLE
- REQUIRES ONLY 3 CONTROL LINES
- ON CHIP OSCILLATOR
- CMOS TECHNOLOGY FOR WIDE SUPPLY VOLTAGE RANGE
- – 40 TO 85 °C TEMPERATURE RANGE



DIP-40
(Plastic)

ORDER CODES : M8439 B6
M8439 DIE 1

PIN CONNECTION



5-8309

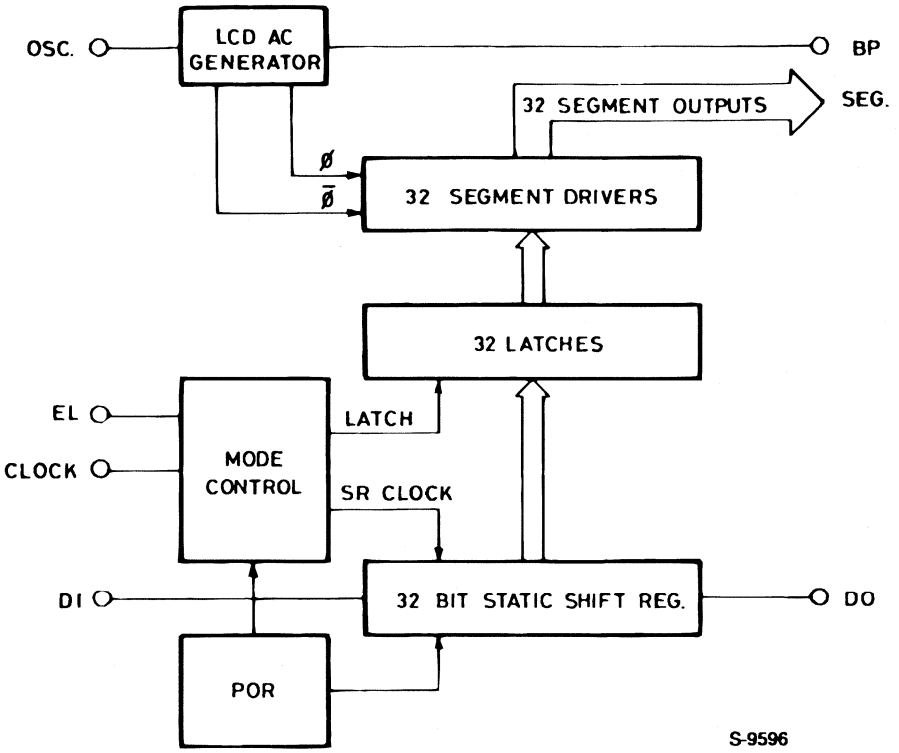
DESCRIPTION

The M8439 is a CMOS integrated circuit that drives an LCD display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.

The M8439 can drive any standard or custom parallel drive LCD whether it be field effect or dynamic scattering. Several drivers can be cascaded, if more than 32 segments are to be driven. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the OSC input which determines the frequency of an internal oscillator.

The M8439 is available in DIE form and assembled in 40 pin dual-in line plastic.

BLOCK DIAGRAM



OSC : Oscillator (capacitor or drive signal)
EL : Enable / Latch control input
DI : Serial data input
DO : Serial data output
BP : Backplane output
SEG : Segment output signal

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$(V_{DD}-V_{SS})$	Supply Voltage	– 0.3 to + 12	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
P_D	Power Dissipation	250	mW
T_{stg}	Storage Temperature	– 55 to + 125	°C
T_A	Operating Temperature	– 40 to + 85	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise noted)

Symbol	Parameter		Test conditions	Min.	Max.	Unit
STATIC ELECTRICAL CHARACTERISTICS						
V_{DD}	Supply Voltage			3	10	V
I_{DD}	Supply Current		Oscillator f < 15 kHz		60	µA
I_Q	Quiescent Current		V_{DD} = 10 V		10	µA
V_{IH}	Input High Level	CLOCK, DI, EL		.5 V_{DD}	V_{DD}	V
V_{IL}	Input Low Level	CLOCK, DI, EL		0	.2 V_{DD}	V
I_{IN}	Input Current	CLOCK, DI, EL			± 5	µA
C_I	Input Capacitance	CLOCK, DI, EL			5	pF
V_{IH}	Input High Level	OSC	Driven Mode	.9 V_{DD}		V
V_{IL}	Input Low Level	OSC	Driven Mode		.1 V_{DD}	V
I_{IN}	Input Current	OSC	Driven Mode		± 10	µA
R_{ON}	Segment Output Impedance		I_{IL}= 10 µA		40	kΩ
R_{ON}	Backplane Output Impedance		I_L = 100 µA		3	kΩ
V_{OFF}	Output Offset Voltage		C_L = 250 pF between Each SEG Output and BP		± 50	mV
R_{ON}	Data Output Impedance		I_L = 100 µA		3	kΩ
DYNAMIC ELECTRICAL CHARACTERISTICS						
t_{TR}	Transition Time OSC		Driven Mode		500	ns
t_{SD}	Data Set-up Time		Fig. 1 and 2	150		ns
t_{HD}	Data Hold Time		Fig. 1 and 2	50		ns
t_{SE}	EL Set-up Time		Fig. 1	100		ns
t_{HE}	EL Hold Time		Fig. 1	100		ns
t_{WE}	EL Pulse Width		Fig. 2	175		ns
t_{CE}	Clock to EL Time		Fig. 2	250		ns
t_{pd}	DO Propagation Delay		Fig. 1, 2 ; C_L = 55 pF		500	ns
f	Clock Rate		V_{DD} = 10 50 % Duty Cycle ;	DC	1.5	MHz

FUNCTIONAL DESCRIPTION

LCD-AC-GENERATOR

This block generates a 50 % duty cycle signal for the backplane output. The circuit can be used in two different modes : oscillator or driven.

OSCILLATOR MODE : In this mode the backplane frequency is determined by the internal RC oscillator together with an 8-stage frequency divider. For generating the backplane output signal of 50 % duty cycle the oscillator frequency is divided by 256. The RC oscillator requires an external capacitor to be connected between input OSC and V_{SS}. A value of 18 pF gives a backplane frequency of 80 Hz ± 30 % at V_{DD} = 5 V. The variation of the backplane frequency over the entire temperature and supply voltage range is ± 50 %.

DRIVEN MODE : In this mode the signal at the backplane output BP is in phase with an external driving signal applied to input OSC. This mode is used to synchronize the LCD drive of two or more cascaded driver circuits.

DETECTION LOGIC The circuit is able to distinguish between the conditions for oscillator or driven mode. If the circuit is to be in the oscillator mode, the OSC pin has a capacitor connected to it. The oscillator will start as soon as the supply voltage exceeds a certain minimum value. The signal at pin OSC swings within a range from 0.3 V_{DD} to 0.7 V_{DD}. If the circuit is to be in the driven mode, the OSC pin has to be forced to logic levels by an external source. The transition time between the logic levels must be short, so that the circuit does not react on the voltage level in between. In the driven mode the 8-stage frequency divider is by-passed.

SEGMENT OUTPUTS

A logic 0 at the data input DI causes a segment output signal to be in phase with the backplane signal and turns the segment off. A logic 1 causes a segment output to be in opposite phase to the backplane signal and turns the segment on.

MICROPROCESSOR INTERFACE

Fig. 2 shows a timing diagram.

Data is serially shifted in and out of the shift register on the negative transition of the clock.

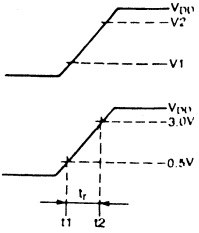
Serial entry into the shift register is permitted independently of the enable/latch control EL. When EL is high it causes a parallel load of the content in the shift register into the latches. It is acceptable to tie the EL line high. Then the latches are transparent and only two lines, clock and data input, would then be needed for data transfer.

POWER-ON LOGIC

A power on reset pulse is generated internally when the supply voltage is being turned on. The generation of the reset pulse is level dependent and will occur even on a slowly rising supply voltage. The power on reset pulse resets all shift register stages and the latches that control the segment drivers. Therefore all segment outputs are initially in phase with the backplane output. This causes the display to be blanked and no arbitrary data to show up. This condition is maintained until data is shifted into the register and loaded into the latches.

CONDITIONS FOR POWER-ON RESET FUNCTION The POR circuit triggers on the rising slope of the positive supply voltage V_{DD}. A reset pulse will be generated, if conditions a) through d) are given :

a) Level
Rising slope from
V1 to V2
V1 max = 0.5 V
V2 min = 3.0 V



b) Rise time
t_r min = 10 µs
t_r max = 1 s

c) Rise function
The function of V_{DD} between t1 and t2 may be nonlinear, but should not show a maximum and should not exceed 0.25 V/µs.

d) Recovery time
The minimum time between turn-off and turn-on of V_{DD} is 1s.

CASCADE CONFIGURATION

Several LCD drivers can be cascaded if a liquid crystal display with more than 32 segments is to be connected.

The phase correlation between all segments outputs is achieved by using the second (and any other) device in the driven mode.

Two different cascade configurations can be chosen depending whether the LCD frequency is to be determined by the internal RC oscillator or by an external signal.

Figure 3 shows the connection scheme for a self oscillating configuration, figure 4 shows the connection of an externally controlled one.

Figure 1 : Timing Diagram of Latch Mode : Set-up and Hold Time.

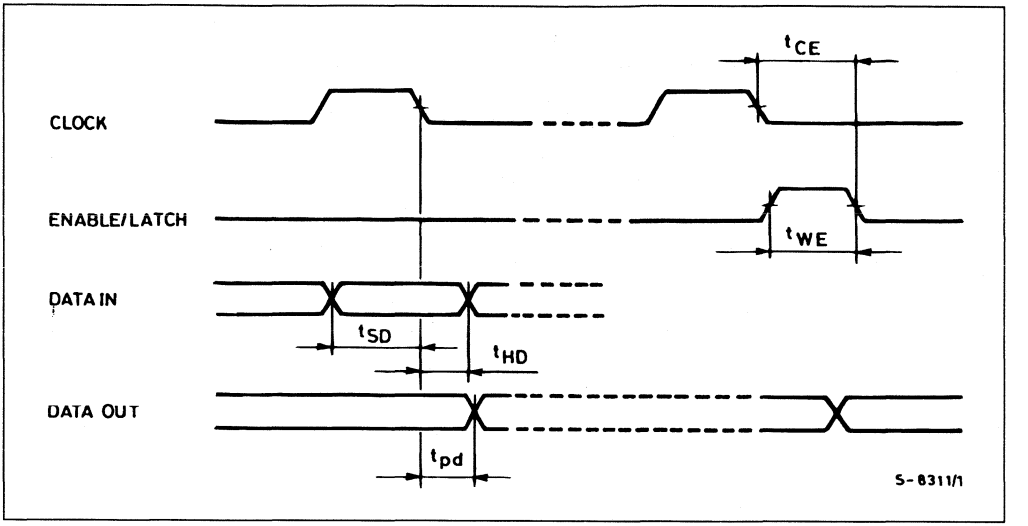


Figure 2 : Timing Diagram of Latch Mode : Serial Load into SR and Parallel Transfer to LCD.

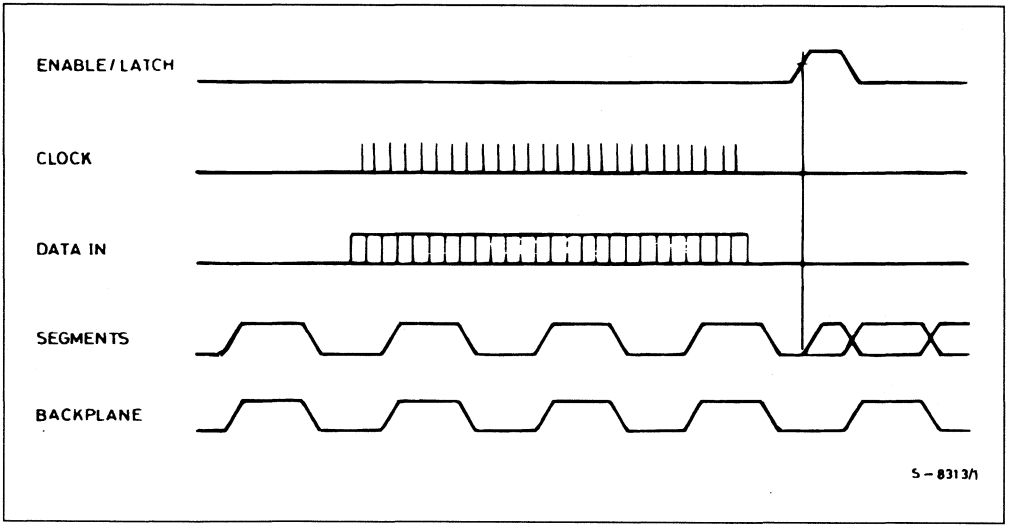


Figure 3 : Cascade Configuration, Self Oscillating.

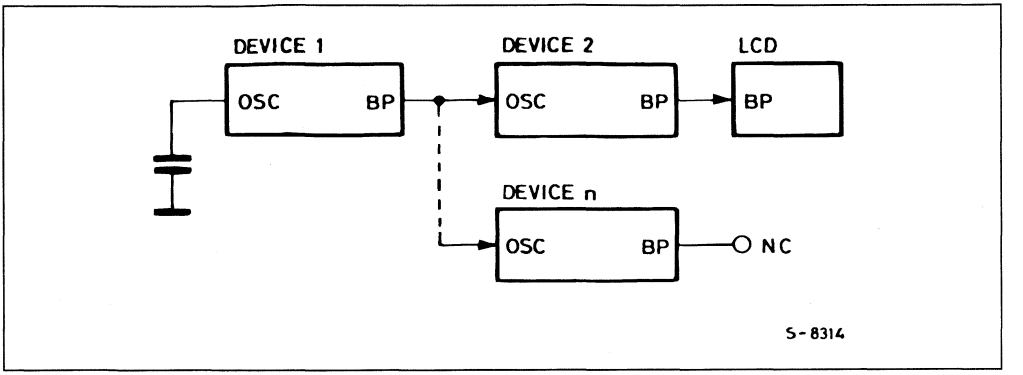
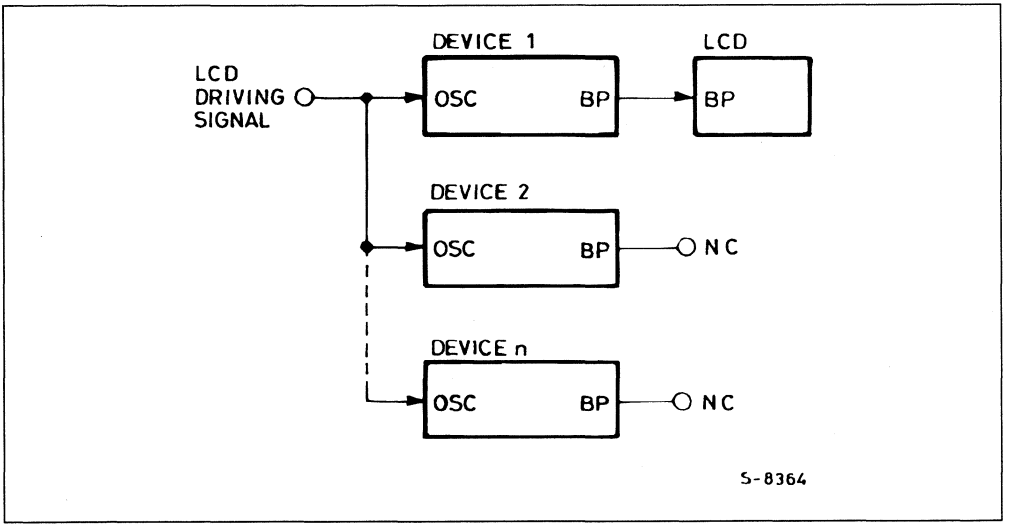


Figure 4 : Cascade Configuration, Drive by External Signal.



SGS-THOMSON MICROELECTRONICS

UCN4801A

BIMOS LATCH/DRIVERS

ADVANCE DATA

- HIGH-VOLTAGE, HIGH-CURRENT OUTPUTS
- OUTPUT TRANSIENT PROTECTION
- CMOS, PMOS, NMOS, TTL COMPATIBLE INPUTS
- INTERNAL PULL-DOWN RESISTORS
- LOW-POWER CMOS LATCHES

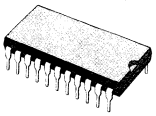
DESCRIPTION

The UCN4801A is a high-voltage, high-current latch/driver comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility.

The CMOS inputs are compatible with standard CMOS, PMOS and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power load.

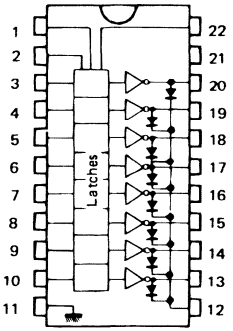
The unit feature open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

DIP-22
(Plastic)



ORDER CODE : UCN4801ADP

PIN CONNECTIONS (Top view)



1 - Clear
2 - Strobe
3 - Input 1
4 - Input 2
5 - Input 3
6 - Input 4
7 - Input 5
8 - Input 6
9 - Input 7
10 - Input 8
11 - GND

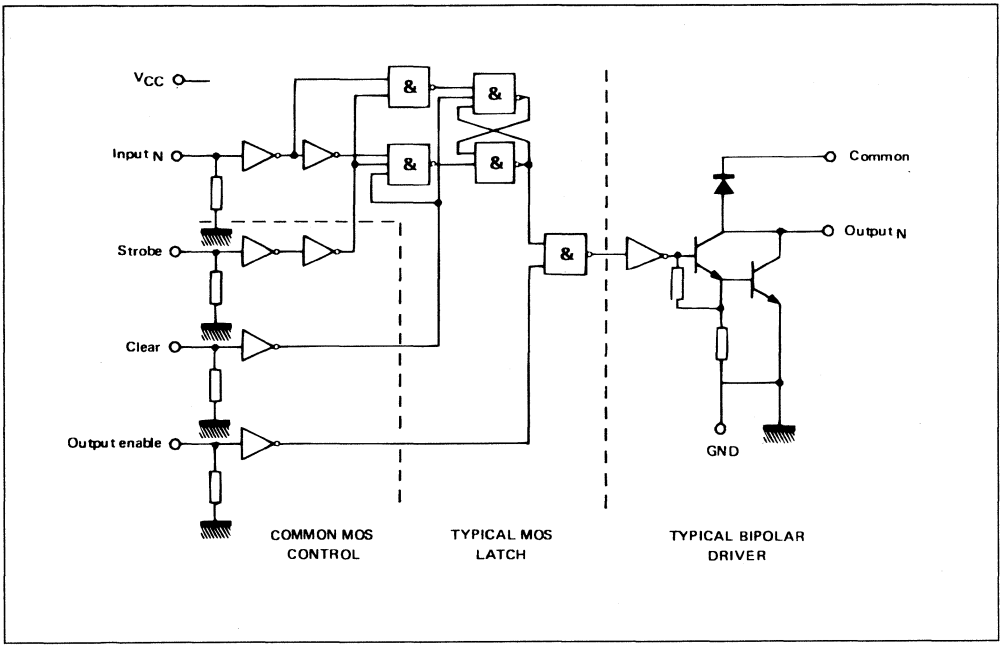
22 - Output enable
21 - V_{CC}
20 - Output 1
19 - Output 2
18 - Output 3
17 - Output 4
16 - Output 5
15 - Output 6
14 - Output 7
13 - Output 8
12 - Common

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_O	Output Voltage	50	V
V_{CC}	Supply Voltage	18	V
V_I	Input Voltage Range	− 0.3 to V_{CC} + 0.3	V
I_C	Continuous Collector Current	500	mA
P_{tot}	Power Dissipation*	2.0	W
T_{op}	Operating Ambient Temperature Range	− 20 to + 85	°C
T_{stg}	Storage Temperature	− 55 to + 125	°C

* Derate at the rate of 20 m/°C above T_{amb} = + 25 °C

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS T_{amb} = + 25 °C, V_{CC} = 5 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_O	Output Leakage Current (V_O = 50 V)				µA
	T_{amb} = + 25 °C	–	–	50	
	T_{amb} = + 70 °C	–	–	100	
$V_{O(Sat)}$	Collector-emitter Saturation Voltage				V
	I_O = 100 mA	–	0.9	1.1	
	I_O = 200 mA	–	1.1	1.3	
	I_O = 350 mA, V_{CC} = 7 V	–	1.3	1.6	
$V_{I(O)}$	Input Voltage	–	–	1	V
$V_{I(1)}$	V_{CC} = 15 V	13.5	–	–	
	V_{CC} = 10 V	8.5	–	–	
	V_{CC} = 5 V - (note 1)	3.5	–	–	
R_{IN}	Input Resistance				KΩ
	V_{CC} = 15 V	50	200	–	
	V_{CC} = 10 V	50	300	–	
	V_{CC} = 5 V	50	600	–	
$I_{CC(on)}$	Supply Current - Outputs Open				mA
(each stage)	V_{CC} = 15 V	–	1	2	
	V_{CC} = 10 V	–	0.9	1.7	
	V_{CC} = 5 V	–	0.7	1	
$I_{CC(off)}$	All Drivers off, All Inputs = 0 V	–	50	100	µA
I_R	Clamp Diode Leakage Current (V_R = 50 V)				µA
	T_{amb} = + 25 °C	–	–	50	
	T_{amb} = + 70 °C	–	–	100	
V_F	Clamp Diode Forward Voltage I_F = 350 mA	–	1.7	2	V

Note : 1. Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "I".

TRUTH TABLE

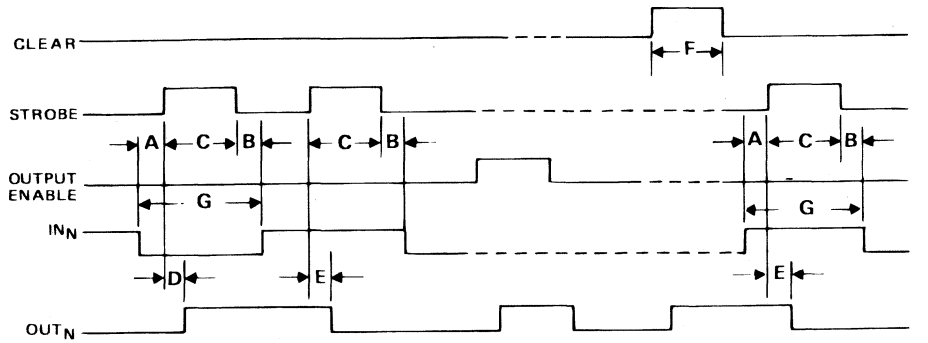
			Output	OUT_N	
IN_N	Strobe	Clear	Enable	t–1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON

X = irrelevant
t-1 = previous output state
t = present output state

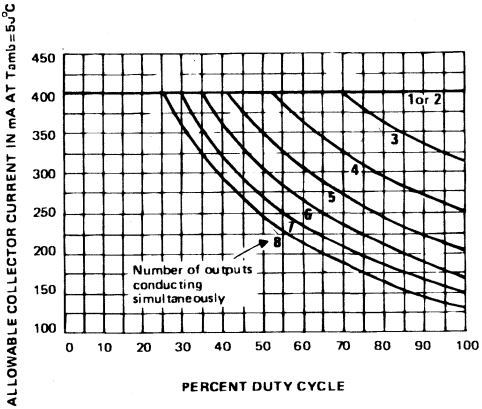
Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TIMING CONDITIONS

(Logic levels are V_{CC} and GND) V_{CC} = 5 V, Tamb + 25°C



A. Minimum data active time before strobe enabled (data set-up time)	100 ns
B. Minimum data active time after strobe disabled (data hold time)	100 ns
C. Minimum strobe pulse width	300 ns
D. Typical time between strobe activation and output on to off transition	500 ns
E. Typical time between strobe activation and output off to on transition	500 ns
F. Minimum clear pulse width	300 ns
G. Minimum data pulse width	500 ns



SGS-THOMSON MICROELECTRONICS

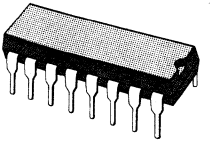
ULN2001A-ULN2003A
ULN2002A-ULN2004A

SEVEN DARLINGTON ARRAYS

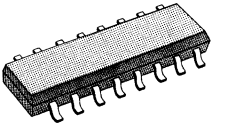
- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA PEAK)
- OUTPUT VOLTAGE 50 V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal printheads and high power buffers.

The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.



DIP-16 Plastic
(0.25)



SO-16J

ORDER CODES :
ULN2001A/2A/3A/4A (DIP-16)
ULN2001D/2D/3D/4D (SO-16)

DESCRIPTION

The ULN2001A, ULN2002A, ULN2003 and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

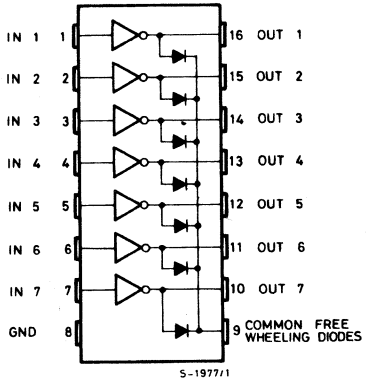
The four versions interface to all common logic families :

ULN2001A	General Purpose, DTL, TTL, PMOS, CMOS
ULN2002A	14-25 V PMOS
ULN2003A	5 V TTL, CMOS
ULN2004A	6–15 V CMOS, PMOS

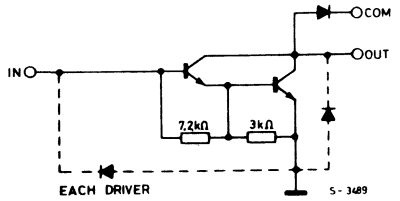
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULN2002A/D - 2003A/D - 2004A/D)	30	V
I_c	Continuous Collector Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
T_j	Junction Temperature	150	°C

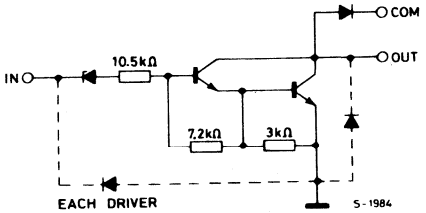
PIN CONNECTION



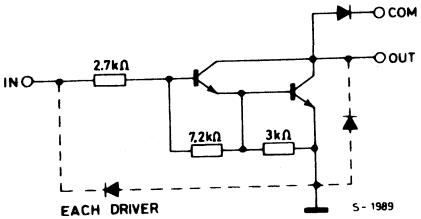
SCHEMATIC DIAGRAM



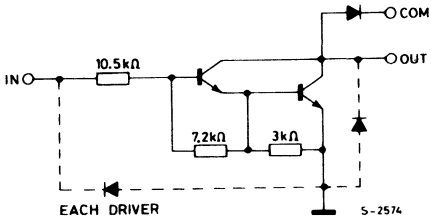
Series ULN-2001A
(each driver)



Series ULN-2002A
(each driver)



Series ULN-2003A
(each driver)



Series ULN-2004A
(each driver)

THERMAL DATA

			DIP–16	SO–16
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	70 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V			50	µA	1a
		T_{amb} = 70 °C V_{CE} = 50 V			100	µA	1a
		T_{amb} = 70 °C for **ULN2002A**					
		V_{CE} = 50 V V_i = 6 V			500	µA	1b
		for **ULN2004A**					
		V_{CE} = 50 V V_i = 1 V			500	µA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA I_B = 250 µA		0.9	1.1	V	2
		I_C = 200 mA I_B = 350 µA		1.1	1.3	V	2
		I_C = 350 mA I_B = 500 µA		1.3	1.6	V	2
$I_{i(on)}$	Input Current	for **ULN2002A** V_i = 17 V		0.82	1.25	mA	3
		for **ULN2003A** V_i = 3.85 V		0.93	1.35	mA	3
		for **ULN2004A** V_i = 5 V		0.35	0.5	mA	3
		V_i = 12 V		1	1.45	mA	3
$I_{i(off)}$	Input Current	T_{amb} = 70 °C I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULN2002A**					
		V_{CE} = 2 V I_C = 300 mA			13	V	5
		for **ULN2003A**					
		V_{CE} = 2 V I_C = 200 mA			2.4	V	5
		V_{CE} = 2 V I_C = 250 mA			2.7	V	5
		V_{CE} = 2 V I_C = 300 mA			3	V	5
		for **ULN2004A**					
		V_{CE} = 2 V I_C = 125 mA			5	V	5
		V_{CE} = 2 V I_C = 200 mA			6	V	5
		V_{CE} = 2 V I_C = 275 mA			7	V	5
		V_{CE} = 2 V I_C = 350 mA			8	V	5
h_{FE}	DC Forward Current Gain	for **ULN2001A**					
		V_{CE} = 2 V I_C = 350 mA	1000			–	2
C_i	Input Capacitance			15	25	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50 V			50	µA	6
		T_{amb} = 70 °C V_R = 50 V			100	µA	6
V_F	Clamp Diode Forward Voltage	I_F = 350 mA		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

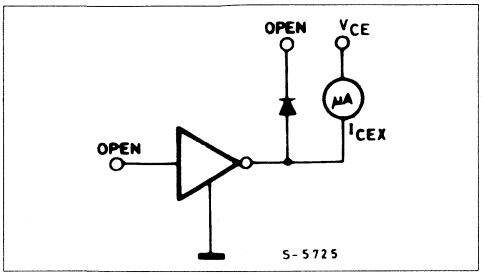


Figure 1b.

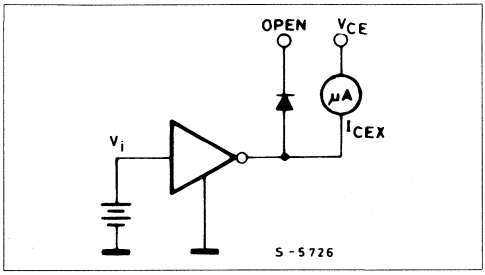


Figure 2.

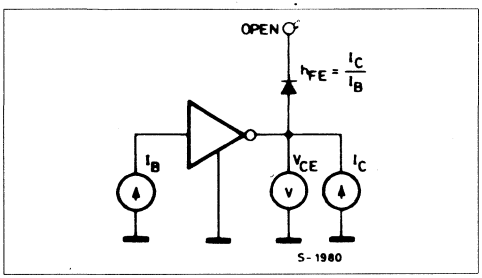


Figure 3.

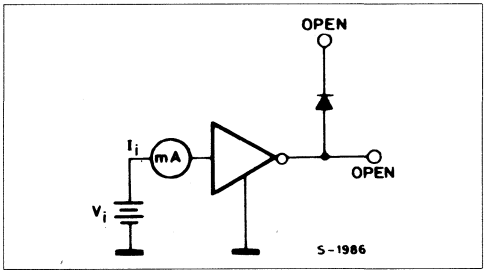


Figure 4.

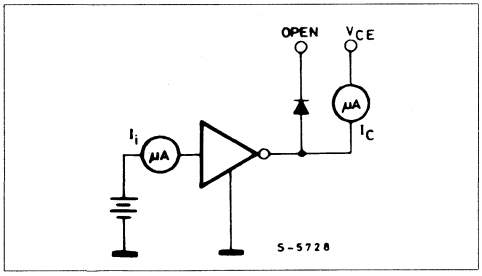


Figure 5.

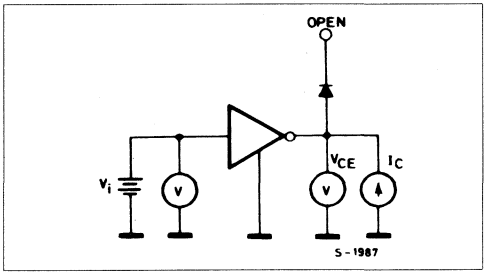


Figure 6.

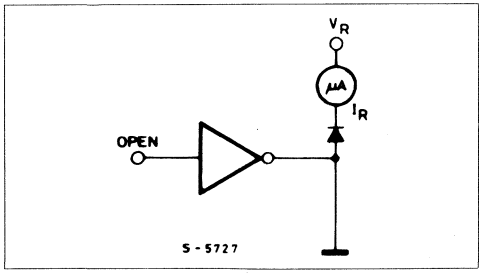
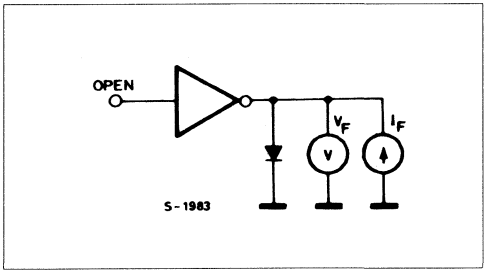


Figure 7.

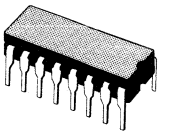


SGS-THOMSON MICROELECTRONICS

ULQ2001R/2R ULQ2003R/4R

SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA PEAK)
- OUTPUT VOLTAGE 50 V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUT CAN BE PARRALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT



DIP-16 Ceramic

DESCRIPTION

The ULQ2001R, ULQ2002R, ULQ2003R and ULQ2004R are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

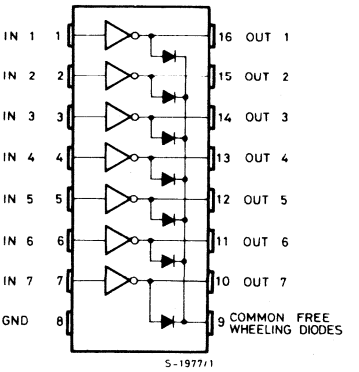
The four versions interface to all common families.

ULQ2001R	General Purpose, DTL, TTL, CMOS
ULQ2002R	15-25 V PMOS
ULQ2003R	5 V TTL, CMOS
ULQ2004R	6-15 V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.

The ULQ2001R, ULQ2002R, ULQ2003R and ULQ 2004R are supplied in 16 pin ceramic DIP packages.

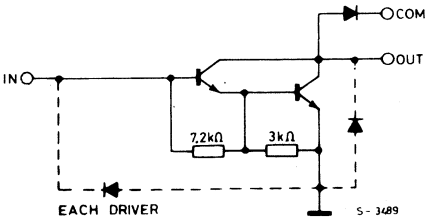
PIN CONNECTION



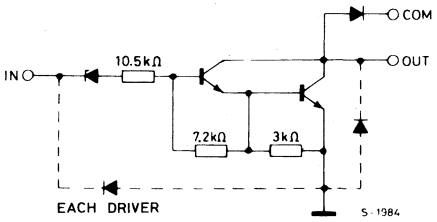
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULQ2002R/2003R/2004R)	30	V
I_c	Continuous Collector Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	− 20 to + 85	°C
T_{stg}	Storage Temperature Range	− 55 to 150	°C

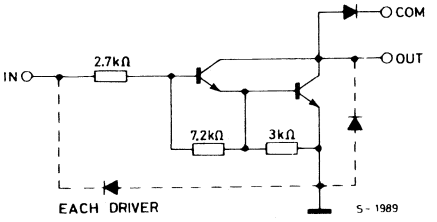
SCHEMATIC DIAGRAM



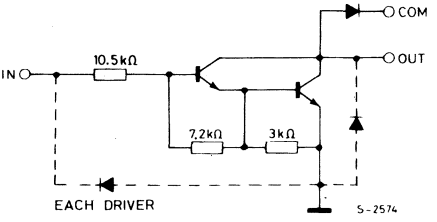
Series ULQ2001R
(each driver)



Series ULQ2002R
(each driver)



Series ULQ2003R
(each driver)



Series ULQ2004R
(each driver)

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	150	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25° C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V				50	µA	1a
		T_{amb} = 70 °C	V_{CE} = 50 V			100	µA	1a
		T_{amb} = 70 °C for **ULQ2002R**						
		V_{CE} = 50 V	V_i = 6 V			500	µA	1b
		for **ULQ2004R**						
		V_{CE} = 50 V	V_i = 1 V			500	µA	1b
$V_{CE\ (sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA	I_B = 250 µA		0.9	1.1	V	2
		I_C = 200 mA	I_B = 350 µA		1.1	1.3	V	2
		I_C = 350 mA	I_B = 500 µA		1.3	1.6	V	2
$I_{i(on)}$	Input Current	for **ULQ2002R**	V_i = 17 V		0.82	1.25	mA	3
		for **ULQ2003R**	V_i = 3.85 V		0.93	1.35	mA	3
		for **ULQ2004R**	V_i = 5 V		0.35	0.5	mA	3
		V_i = 12 V			1	1.45	mA	3
$I_{i(off)}$	Input Current	T_{amb} = 70 °C	I_C = 500 µA	50	65		µA	4
$Vi_{(on)}$	Input Voltage	for **ULQ2002R**						
		V_{CE} = 2 V	I_C = 300 mA			13	V	5
		for **ULQ2003R**						
		V_{CE} = 2 V	I_C = 200 mA			2.4	V	5
		V_{CE} = 2 V	I_C = 250 mA			2.7	V	5
		V_{CE} = 2 V	I_C = 300 mA			3	V	5
		for **ULQ2004R**						
		V_{CE} = 2 V	I_C = 125 mA			5	V	
		V_{CE} = 2 V	I_C = 200 mA			6	V	5
		V_{CE} = 2 V	I_C = 275 mA			7	V	5
		V_{CE} = 2 V	I_C = 350 mA			8	V	5
h_{FE}	DC Forward Current Gain	for **ULQ2001R**						
		V_{CE} = 2 V	I_C = 350 mA	1000			-	2
C_i	Input Capacitance				15	25	pF	-
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			0.25	1	µs	-
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			0.25	1	µs	-
I_R	Clamp Diode Leakage Current	V_R = 50 V				50	µA	6
		T_{amb} = 70 °C	V_R = 50 V			100	µA	6
V_F	Clamp Diode Forward Voltage	I_F = 350 mA			1.7	2	V	7

TEST CIRCUITS

Figure 1a.

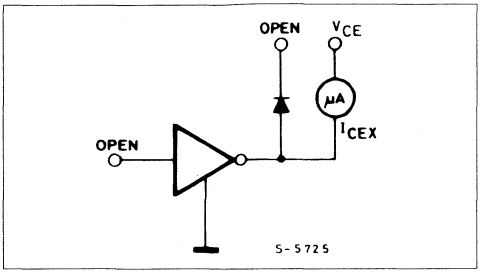


Figure 1b.

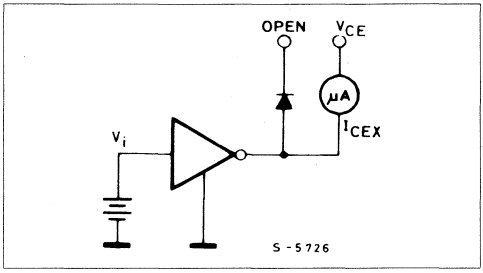


Figure 2.

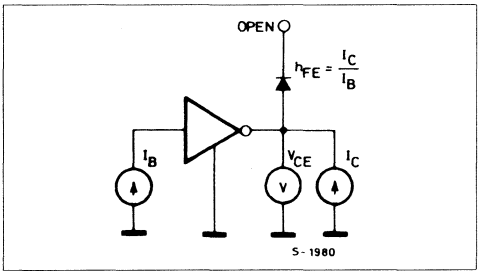


Figure 3.

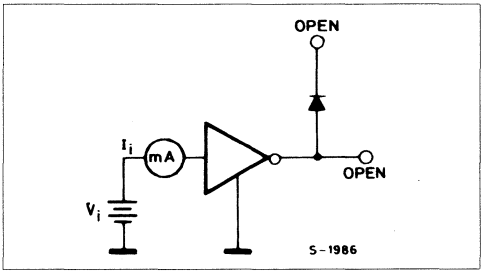


Figure 4.

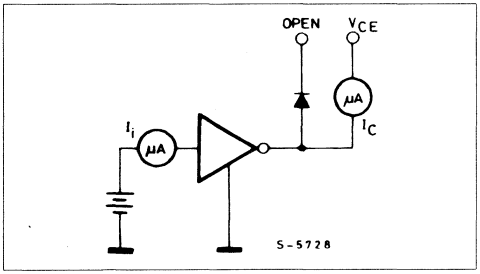


Figure 5.

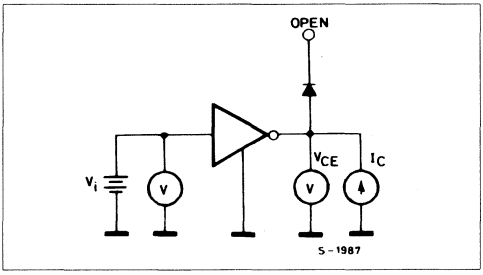


Figure 6.

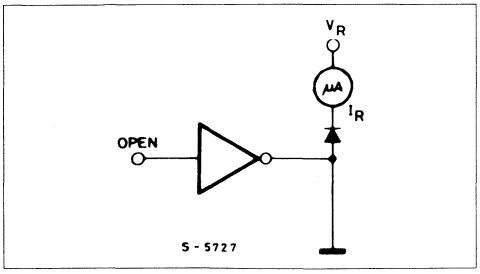
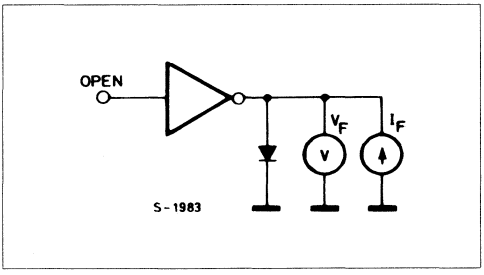


Figure 7.

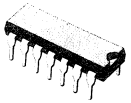


SGS-THOMSON MICROELECTRONICS

LM2901

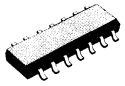
LOW POWER LOW OFFSET VOLTAGE QUAD COMPARATORS

- WIDE SINGLE SUPPLY VOLTAGE RANGE OR DUAL SUPPLIES FOR ALL DEVICES : + 2 V TO + 36 V OR ± 1 V TO ± 18 V
- VERY LOW SUPPLY CURRENT DRAIN (0.8 mA) INDEPENDENT OF SUPPLY VOLTAGE (2 mW/comparator at + 5 V)
- LOW INPUT BIAS CURRENT : 25 nA TYP.
- LOW INPUT OFFSET CURRENT : ± 5 nA TYP.
- LOW INPUT OFFSET VOLTAGE : ± 1 mV TYP.
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- LOW OUTPUT SATURATION VOLTAGE : 250 mV TYP. (I_O = 4 mA)
- DIFFERENTIAL INPUT VOLTAGE RANGE TO THE SUPPLY VOLTAGE
- TTL COMPATIBLE OUTPUTS



N
DIP14
(Plastic Package)

J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

This device consists of four independent precision voltage comparators. This comparator is designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible.

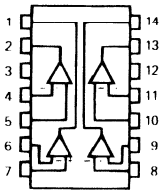
This comparator also have a unique characteris-tic in that the input common-mode voltage range includes ground even through operated from a single power supply voltage.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
LM2901	– 40 to + 105 °C	•	•	•
Example : LM2901D				

PIN CONNECTIONS (top view)

DIP14
CERDIP14
SO14



1 - Output 2
2 - Output 1
3 - V_{CC}
4 - Inverting input 1
5 - Non-inverting input 1
6 - Inverting input 2
7 - Non-inverting 2
8 - Inverting input 3
9 - Non-inverting input 3
10 - Inverting input 4
11 - Non-inverting input 4
12 - V_{CC}
13 - Output 4
14 - Output 3

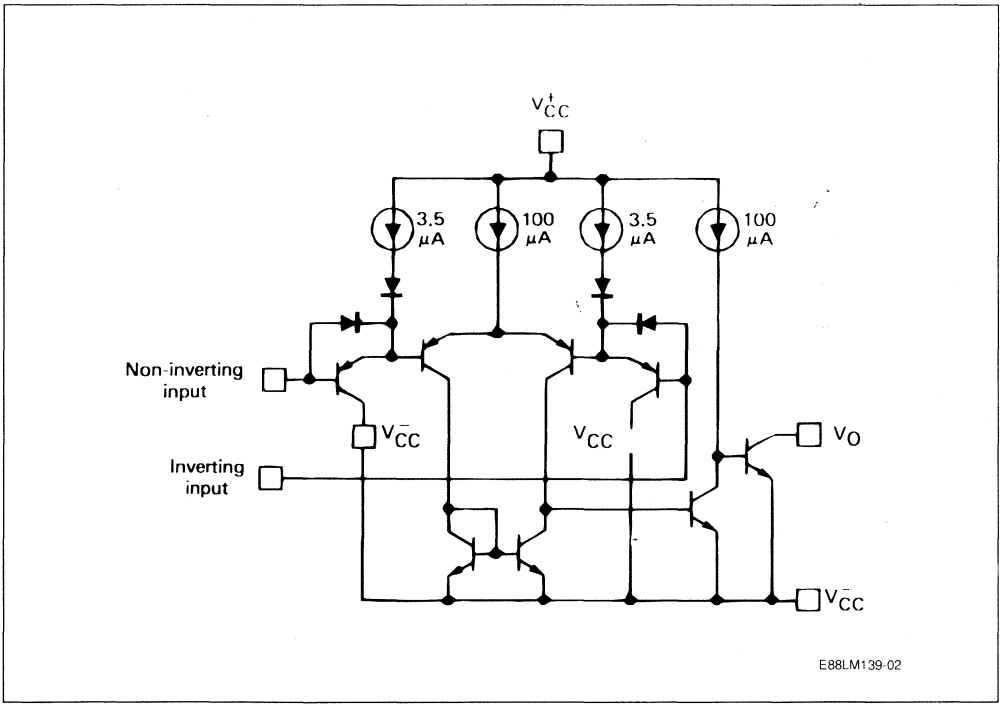
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM2901	Unit
V_{CC}	Supply Voltage	± 18 to 36	V
V_{ID}	Differential Input Voltage	36	V
V_I	Input Voltage	– 0.3 to + 36	V
	Output Short-circuit to Ground – (note 2)	Continuous	
P_{tot}	Power Dissipation – (note 1)	570	mW
T_{oper}	Operating Free-air Temperature Range	– 40 to + 105	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

Notes : 1. Short-circuit from the output to V_{CC}^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA, independent of the magnitude of V_{CC}^+.

2. For operating at high temperatures, the LM2901 must be derated based on a + 125 C max junction temperature and a thermal resistance of 175 C/W which applies for the device soldered on a printed circuit board, operating in a still air ambient.
$R_{th(j\text{-}a)}$ = 250 °C/W. Devices bonded on a 6 x 3 x 0.15 cm glass-epoxy substrate with 30 mm^2 of 35 µm thick copper.

SCHEMATIC DIAGRAM (1/4 LM2901)



CASE	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^-	V_{CC}^+
DIP14 CERDIP14 SO14	1, 2, 13, 14	4, 6, 8, 10	5, 7, 9, 11	12	3

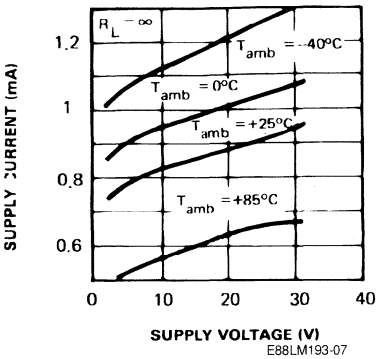
ELECTRICAL CHARACTERISTICS

LM2903 : $-40\ °C \leq T_{amb} \leq +105\ °C$
* = $\geq V_{CC}^{+} = +5$ V, $V_{CC}^{-} =$ GND

Symbol	Parameter	LM2903			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage – (note 3) $T_{amb} = +25\ °C$ $T_{min} \leq T_{amb} \leq T_{max}$	 – 5 – 9	 ± 1	 + 5 + 9	mV
I_{IB}	Input Bias Current – (note 4) $T_{amb} = +25\ °C$ $T_{min} \leq T_{amb} \leq T_{max}$	 – 250 – 400	 ± 25	 + 250 + 400	nA
I_{IO}	Input Offset Current $T_{amb} = +25\ °C$ $T_{min} \leq T_{amb} \leq T_{max}$	 – 50 – 150	 ± 5	 + 50 + 150	nA
A_{VD}	Large Signal Voltage Gain* ($V_{CC} = +15$ V, $V_a = +10$ V, $R_L > 15\ k\Omega$) $T_{amb} = +25\ °C$	 25	 200		V/mV
I_{CC}	Supply Current, no Load $V_{CC} = +30$ V (all comparators) $T_{amb} = 25\ °C$ $T_{min} \leq T_{amb} \leq T_{max}$		 0.4 1	 1 2.5	mA
V_I	Input Voltage Range – (note 5) $T_{amb} = +25\ °C$ $T_{min} \leq T_{amb} \leq T_{max}$		 0 0	 $V_{CC}^{+} - 1.5$ $V_{CC}^{+} - 2$	V
V_{ID}	Differential Input Voltage $V_I \geq 0$ V or if used $V_I^{-} = 0$ V (note 7)			 V_{CC}^{+}	V
I_{OS}	Output Sink Current $V_I^{+} = 0$ V, $V_I^{-} \geq = 1$ V, $V_O \leq = +1.5$ V $T_{amb} = 25\ °C$	 6	 16		mA
V_{OL}	Saturation Voltage $V_I^{-} \geq = 1$ V, $V_I^{+} = 0$ V, $I_{OS} \leq = 4$ mA $T_{amb} = 25\ °C$ $T_{min} < T_{amb} < T_{max}$	 250	 400 700		mV
I_{OH}	High Level Output Current $V_I^{+} \geq = 1$ V, $V_I^{-} = 0$ V $T_{amb} = 25\ °C$, $V_O = +5$ V $T_{min} \leq T_{amb} \leq T_{max}$, $V_O = +30$ V	 	 0.1 	 1000	nA
t_{re}	Response Time $V_L = +5$ V, $R_L = 5;6\ k\Omega$ – (note 6) $T_{amb} = +25\ °C$	 	 1.3	 	µs
t_{rel}	Large Signal Response Time $e_I =$ TTL, $V_{re} = +1.4$ V, $V_L = 5$ V $T_{amb} = 25\ °C$	 	 300	 	ns

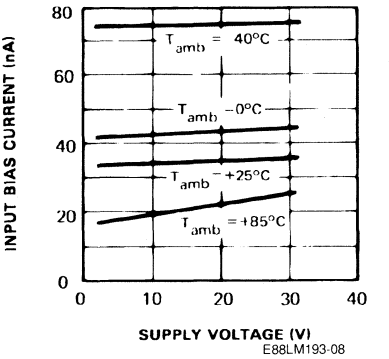
Notes :
3. At output switch point, $V_O = 1.4$ V, $R_S = 0$ with V_{CC}^{-} from 5 V to 30 V the full input common-mode range (0 V to V_{CC}^{+} - 1.5 V).
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading charge exists on the reference or input lines.
5. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC}^{+} - 1.5$ V, but either or both inputs can go to + 30 V without damage.
6. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.
7. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range the comparator will provide a proper output state. The low input voltage state must not be less than – 0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

SUPPLY CURRENT



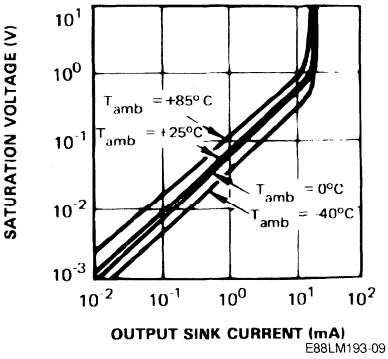
E88LM193-07

INPUT CURRENT



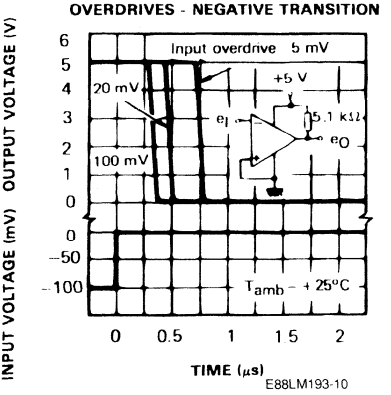
E88LM193-08

OUTPUT SATURATION VOLTAGE



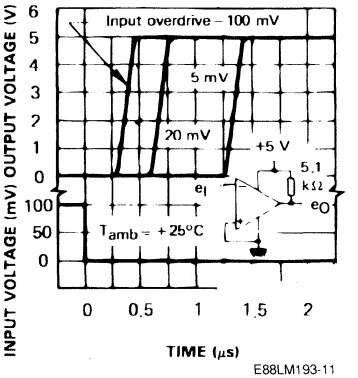
E88LM193-09

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - NEGATIVE TRANSITION



E88LM193-10

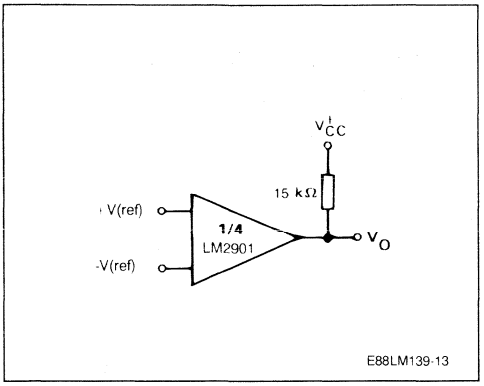
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - POSITIVE TRANSITION



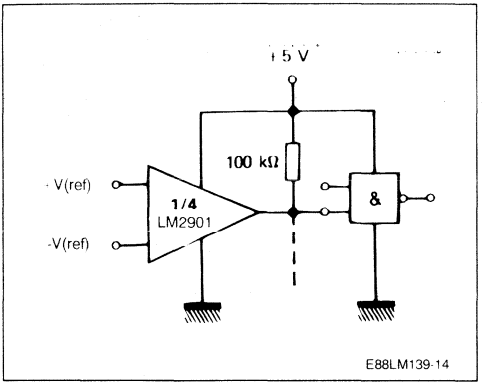
E88LM193-11

TYPICAL APPLICATIONS V_{CC}^{+} = + 5V

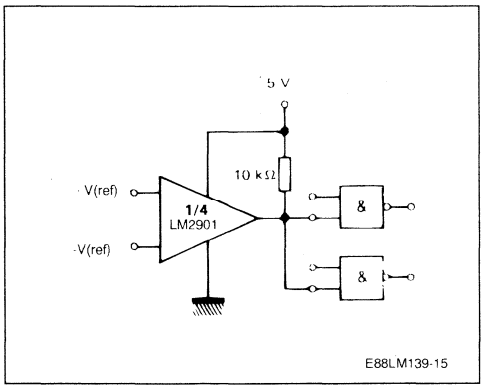
BASIC COMPARATOR



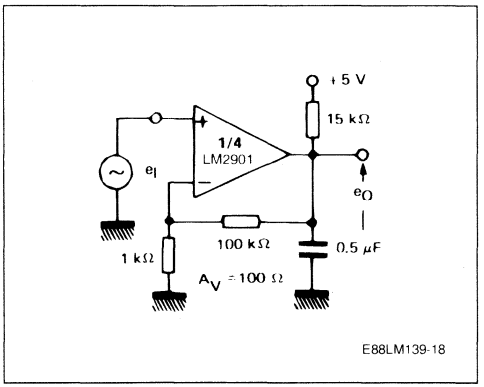
DRIVING CMOS



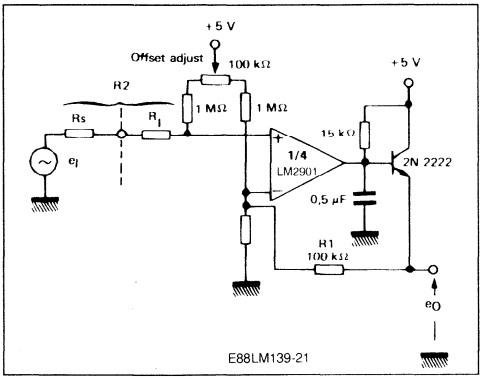
DRIVING TTL



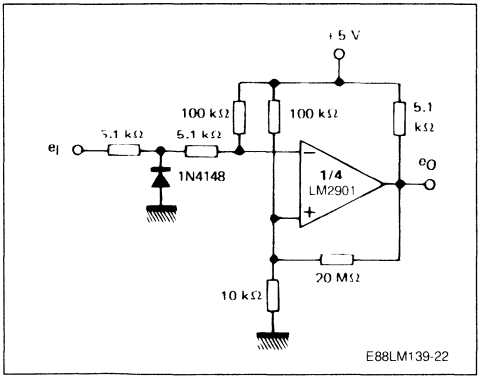
LOW FREQUENCY OP AMP



LOW FREQUENCY OP AMP WITH OFFSET ADJUST

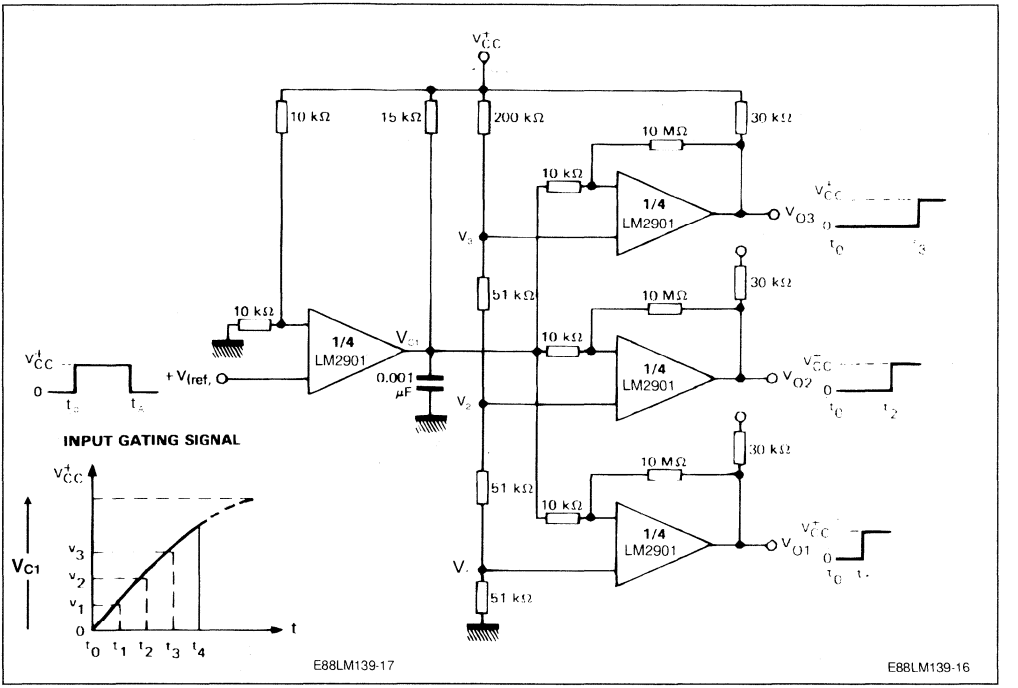


ZERO CROSSING DETECTOR (single power supply)

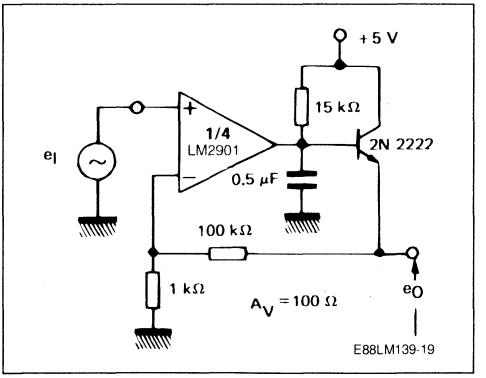


TYPICAL APPLICATIONS (continued)

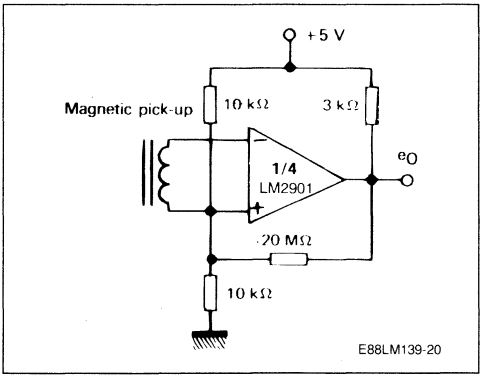
TIME DELAY GENERATOR



LOW FREQUENCY OP AMP

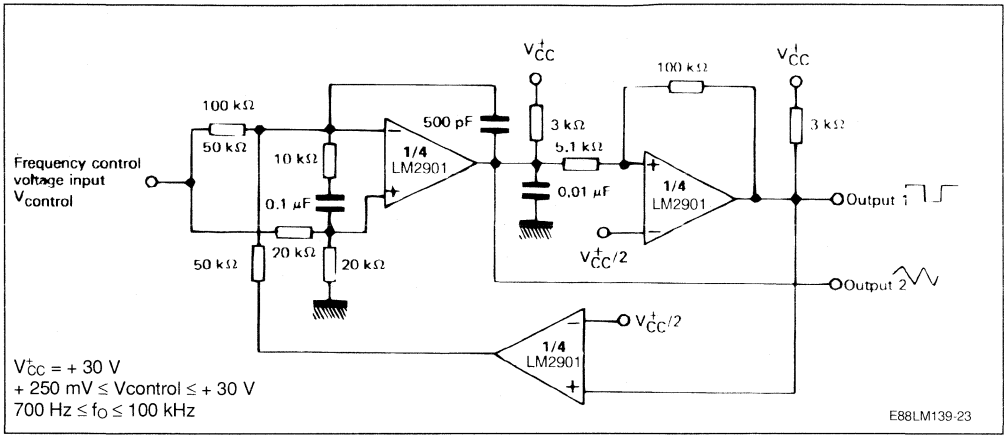


TRANSDUCER AMPLIFIER

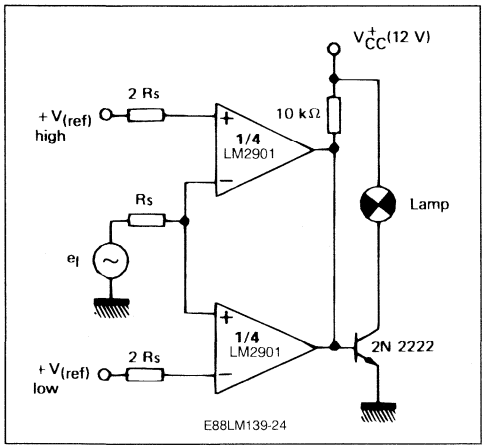


TYPICAL APPLICATIONS (continued)

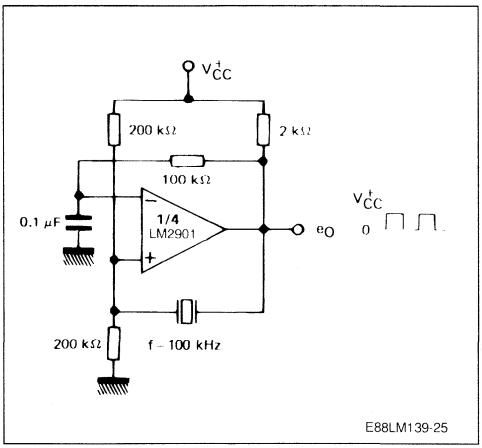
TWO-DECADE HIGH-FREQUENCY VCO



LIMIT COMPARATOR

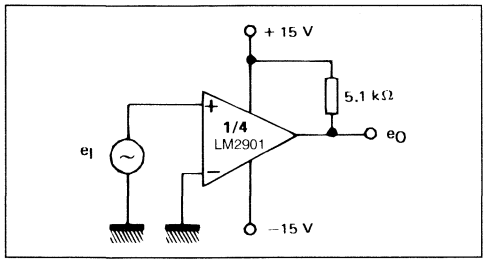


CRYSTAL CONTROLLED OSCILLATOR

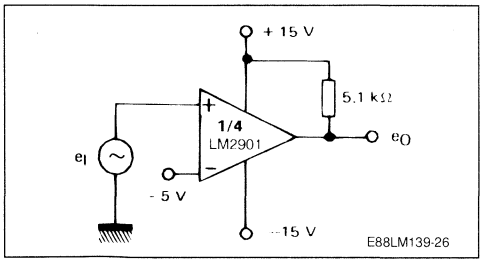


SPLIT-SUPPLY APPLICATIONS

ZERO CROSSING DETECTOR

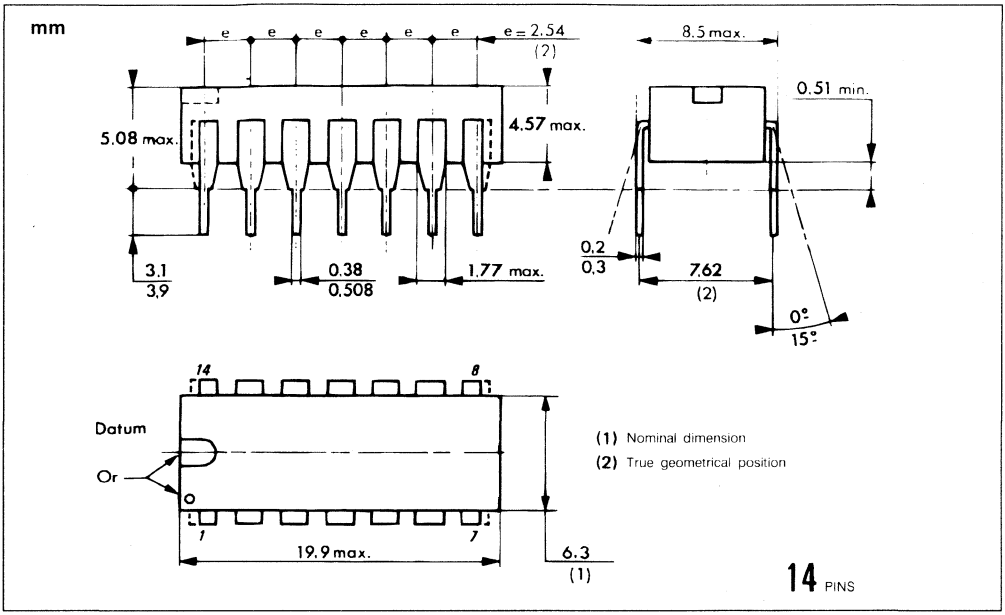


COMPARATOR WITH A NEGATIVE REFERENCE

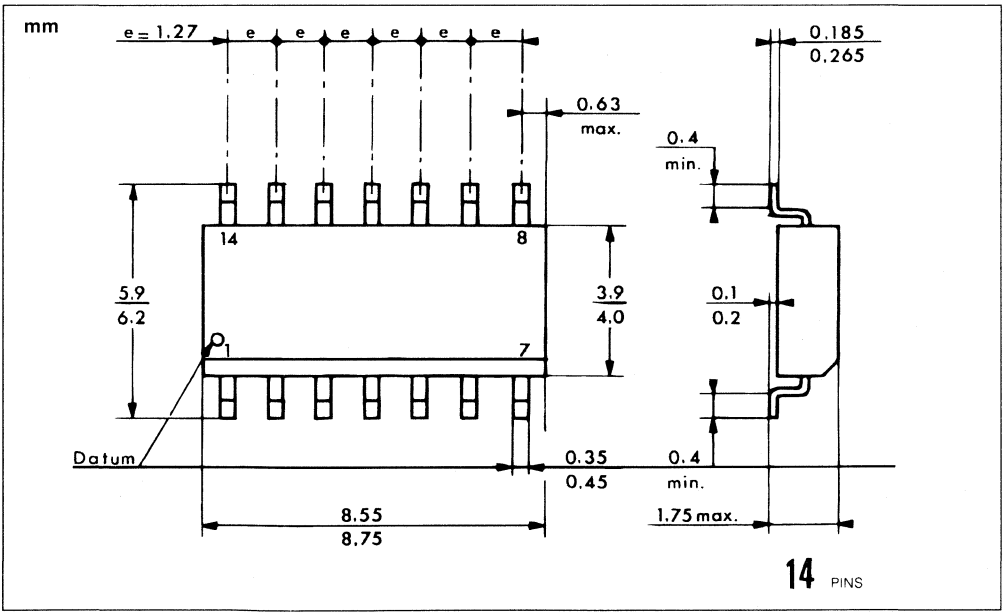


PACKAGE MECHANICAL DATA

14 PINS – PLASTIC DIP OR CERDIP

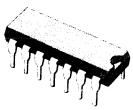


14 PINS – PLASTIC MICROPACKAGE (SO)



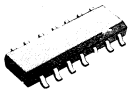
LOW POWER QUAD OPERATIONAL AMPLIFIER

- LARGE VOLTAGE GAIN : 100 dB
- VERY LOW SUPPLY CURRENT/AMPLI : 375 µA
- LOW INPUT BIAS CURRENT : 20 nA
- LOW INPUT OFFSET VOLTAGE : 2 mV
- LOW INPUT OFFSET CURRENT : 2 nA
- WIDE POWER SUPPLY RANGE :
  - SINGLE SUPPLY : + 3 V TO + 30 V
  - DUAL SUPPLIES : 1.5 V TO ± 15 V



N
DIP14
(Plastic Package)

J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

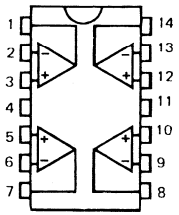
This circuit consists of four independent, high gain, internally frequency compensated operational amplifier which is designed specifically for automotive and industrial control systems. It operates from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
LM2902	– 40 °C to + 105 °C	•	•	•
Example : LM2902J				

PIN CONNECTIONS (top view)

DIP14
CERDIP14
SO14



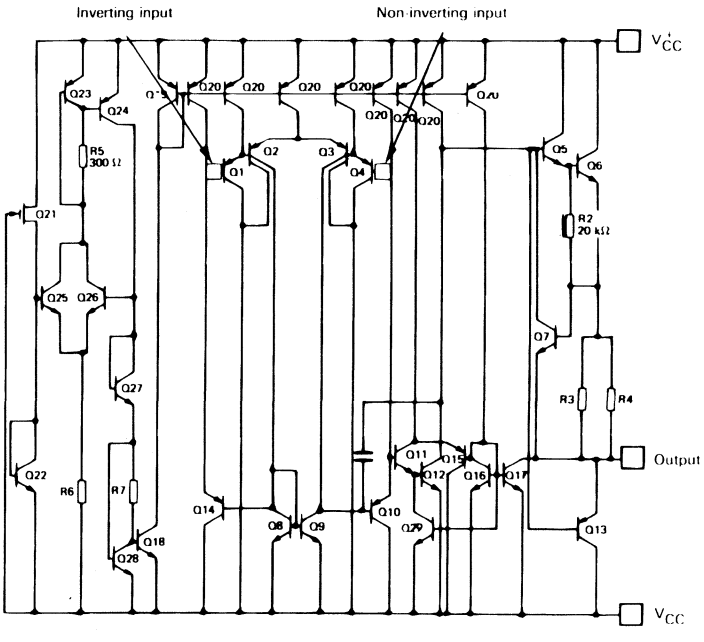
1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2

8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - V_{CC}^+
12 - Non inverting input 4
13 - Inverting input 4
14 - Output 4

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		LM2902	Unit
V_{cc}	Supply Voltage		± 16 or 32	V
V_i	Input Voltage		– 0.3 to + 32	V
V_{id}	Differential Input Voltage		+ 32	V
P_{tot}	Power Dissipation	N, J Suffix D Suffix	500 400	mW
–	Output Short-circuit Duration		INDEFINITE	–
I_{id}	Input Current – (note 6)		50	mA
T_{oper}	Operating Free Air Temperature Range		– 40 to + 105	°C
T_{stg}	Storage Temperature Range		– 65 to + 150	°C

SCHEMATIC DIAGRAM (1/4 LM2902)



E88LM124-01

CASE	Inverting Inputs	Non-inverting Inputs	V_{CC}^-	V_{CC}^+	Outputs
DIP14 CERDIP14 SO14	2, 6, 9, 13	3, 5, 10, 12	11	4	1, 7, 8, 14

ELECTRICAL CHARACTERISTICS

V_{CC}^{+} = + 5 V, V_{CC}^{-} = Ground, V_O = 1.4 V
LM2902 : $-40 \leq T_{amb} \leq +105$ °C
(unless otherwise specified)

Symbol	Parameter		LM2902 Min.	LM2902 Typ.	LM2902 Max.	Unit
V_{IO}	Input Offset Voltage (note 3) T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$			2	5 7	mV
I_{IO}	Input Offset Current T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$			2	20 40	nA
I_{IB}	Input Bias Current (note 2) T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$			20	100 200	nA
A_{VD}	Large Signal Voltage Gain (V_{CC}^{+} = + 15 V, R_L = 2 kΩ) (V_O = 1.4 V to 11.4 V) T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		 50 25	 100		V/mV
S_{VR}	Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ) T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		 65 65	 110		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$ 	V_{CC} = + 5 V V_{CC} = + 30 V V_{CC} = + 5 V V_{CC} = + 30 V		 0.7 1.5 0.8 1.5	 1.2 3 1.2 3	mA
V_I	Input Voltage Range (note 4) T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	V_{CC} = + 30 V	 0 0		 V_{CC} − 1.5 V_{CC} − 2	V
CMR	Common-mode Rejection Ratio ($R_S \leq 10$ kΩ) T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		 70 60	 80		dB
I_O	Output Short-circuit Current (V_I^+ = + 1 V, V_I^- = 0 V, V_{CC} = + 15 V) T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		 20 10	 40	 60	mA
I_{sink}	Output Current Sink (V_I^+ = − 1 V, V_I^- = 0 V) V_{CC} = + 15 V V_O = + 0.2 V 	T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$ T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 10 10 12 12	 20 50 	 	 mA µA
V_{OPP}	Output Voltage Swing T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	$R_L \geq 2$ kΩ $R_L \geq 2$ kΩ	 0 0		 V_{CC} − 1.5 V_{CC} − 2	V
V_{OH}	High Level Output Voltage (V_{CC} = + 30 V) T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$ T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 R_L = 2 kΩ R_L = 10 kΩ 	 26 26 27 27	 27 28 		V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	LM2902			Unit
		Min.	Typ.	Max.	
V_{OL}	Low Level Output Voltage (R_L < 10 kΩ) T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		 5	 20 20	V
S_{VO}	Slew-rate (V_I = 0.5 to 3 V, R_L = 2 kΩ C_L < 100 pF, T_{amb} = + 25 °C, unity gain, V_{CC} = 15 V)	0.2	0.4		V/µs
GBP	Gain Bandwidth Product, V_{CC} = 30 V (f = 100 kHz, T_{amb} = + 25 °C, V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	0.7	1.3	1.8	MHz
THD	Total Harmonic Distortion (f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ, V_O = 2 V_{pp}, C_L < 100 pF, T_{amb} = + 25 °C, V_{CC} = 30 V)		 0.015		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω, V_{CC} = 30 V)		 40		$nV/\sqrt{Hz}$
DV_{io}	Average Temperature Coefficient of Input Offset Voltage $T_{min} \leq T_{amb} \leq T_{max}$		 7	 30	µV/°C
DI_{IO}	Average Temperature Coeff. of Input Offset Current $T_{min} \leq T_{amb} \leq 25$ °C		 10	 300	pA/°C
V_O1/V_O2	Channel Separation – (note 5) 1 kHz ≤ f ≤ 20 kHz		 120		dB

Notes : 1 - Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15 V. The maximum output current is approximatively 40 mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.

2 - The direction of the input current is out of the IC. This current is essentialy constant, independent of the state of the output so no loading change exists on the input lines.

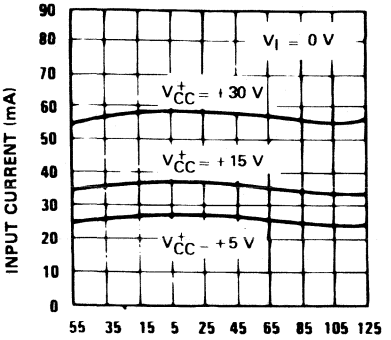
3 - V_o = 1.4 V, R_S = 0, 5 V < V_{CC} < 30 V, 0 < V_I < V_{CC} – 1.5 V.

4 - The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} – 1.5 V, but either or both inputs can go to + 32 V without damage.

5 - Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequences.

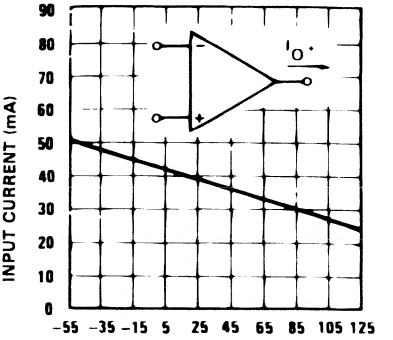
6 - This input only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative.
This is not destructive and normal output will set up again for input voltage higher than – 0.3 V.

INPUT CURRENT (Note 8)



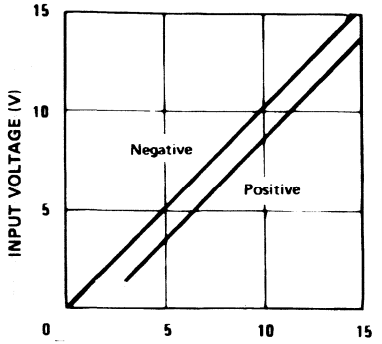
E88LM124-02

CURRENT LIMITING (Note 8)



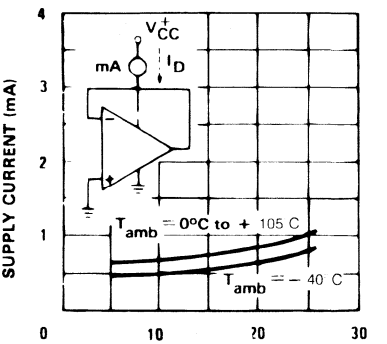
E88LM124-03

INPUT VOLTAGE RANGE



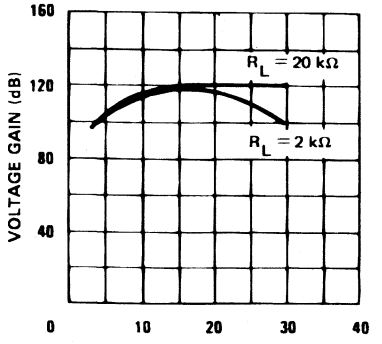
E88LM124-04

SUPPLY CURRENT



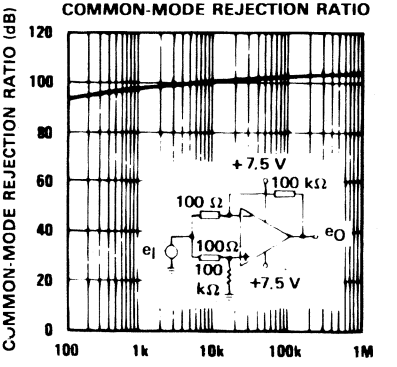
E88LM124-05

VOLTAGE GAIN



E88LM124-06

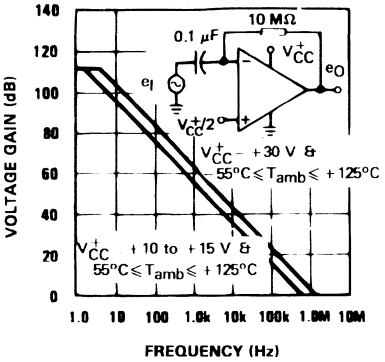
COMMON-MODE REJECTION RATIO



E88LM124-07

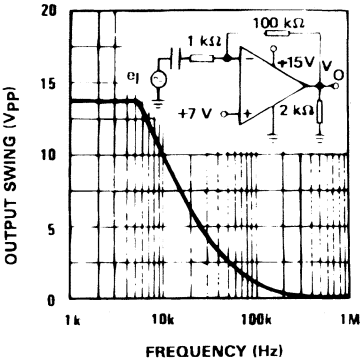
Note : 8 - **LM2902** : − 40 °C ≤ T_{amb} ≤ + 105 °C

REPONSE EN FREQUENCE EN BOUCLE OUVERTE



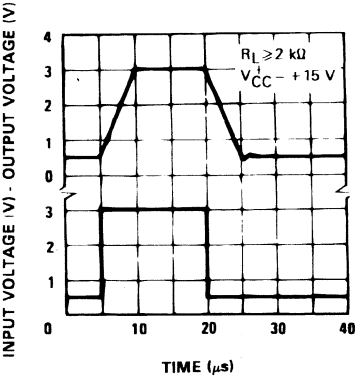
E88LM124-08

LARGE SIGNAL FREQUENCY RESPONSE



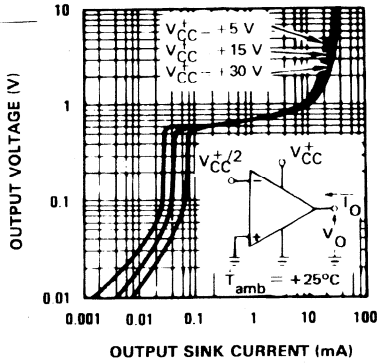
E88LM124-09

VOLTAGE FOLLOWER PULSE RESPONSE



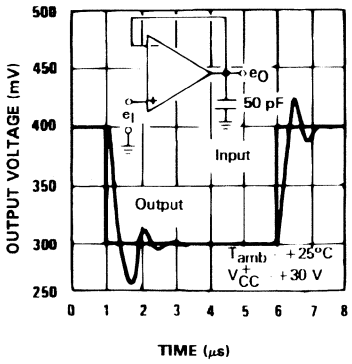
E88LM124-10

OUTPUT CHARACTERISTICS (CURRENT SINKING)



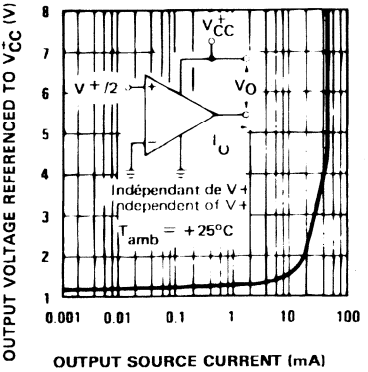
E88LM124-11

VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



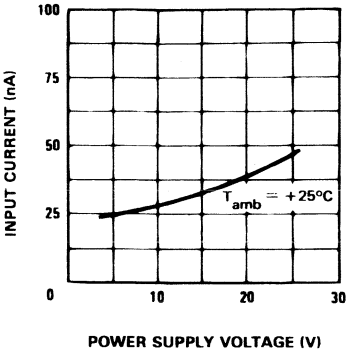
E88LM124-12

OUTPUT CHARACTERISTICS (CURRENT SOURCING)



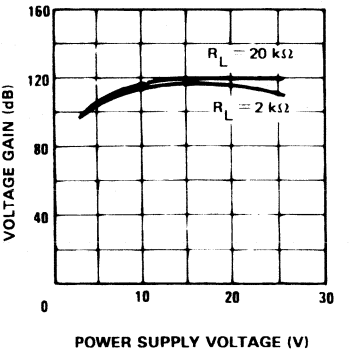
E88LM124-13

INPUT CURRENT



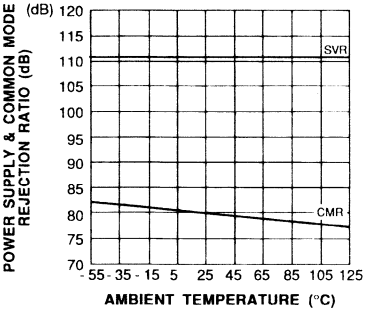
E88LM124-14

VOLTAGE GAIN



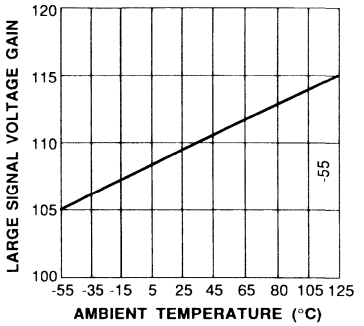
E88LM124-15

POWER SUPPLY & COMMON MODE REJECTION RATIO



E88LM124-16

LARGE SIGNAL VOLTAGE GAIN

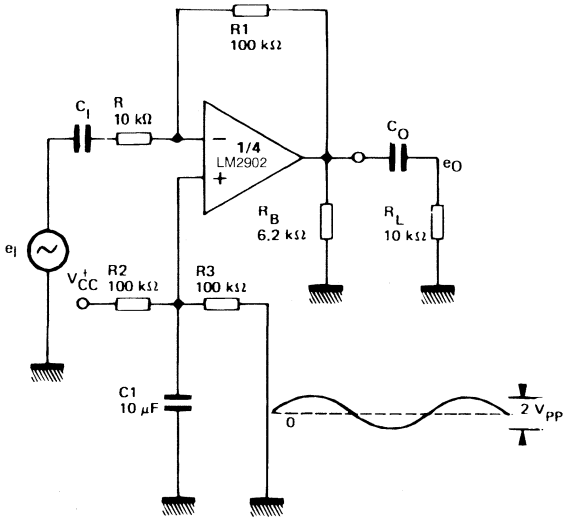


E88LM124-17

TYPICAL SINGLE - SUPPLY APPLICATIONS

AC COUPLED INVERTING AMPLIFIER

$$A_V = \frac{-R}{R1} \text{ (As shown } A_V = -10)$$

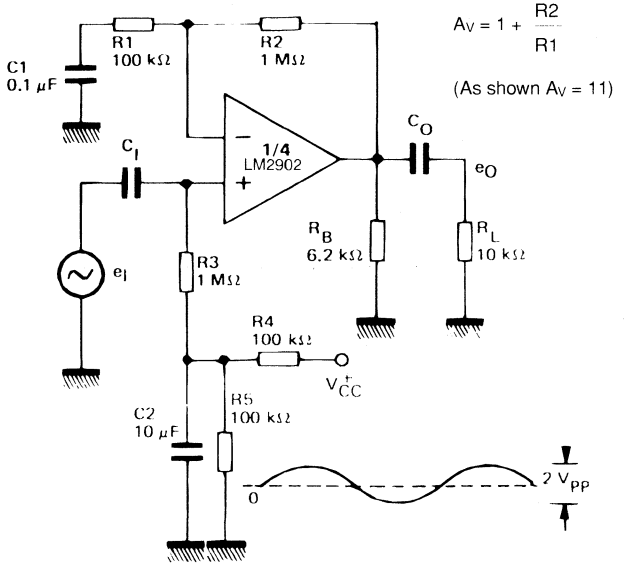


E88LM124-18

AC COUPLED NON-INVERTING AMPLIFIER

$$A_V = 1 + \frac{R2}{R1}$$

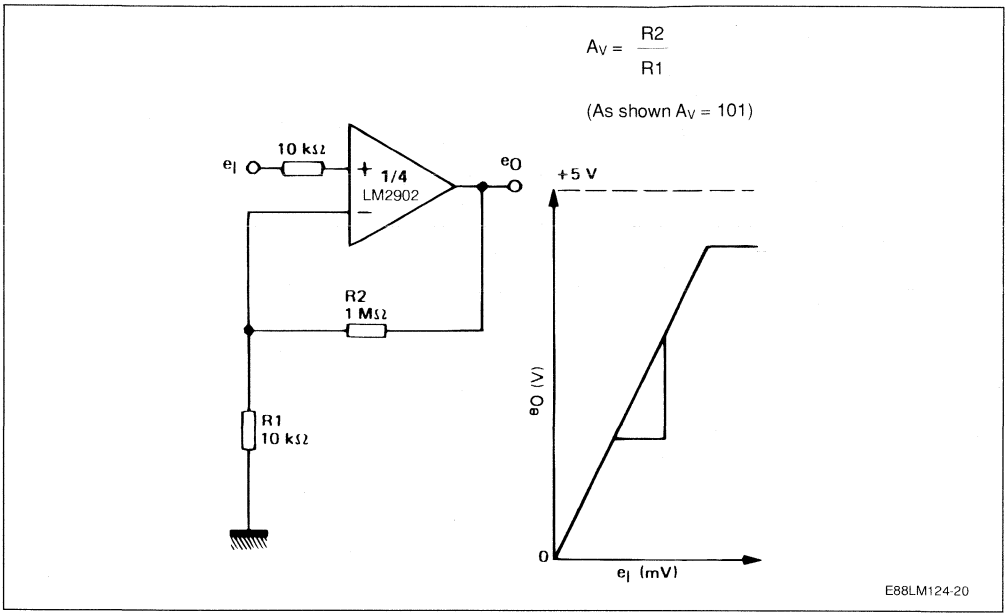
(As shown $A_V = 11$)



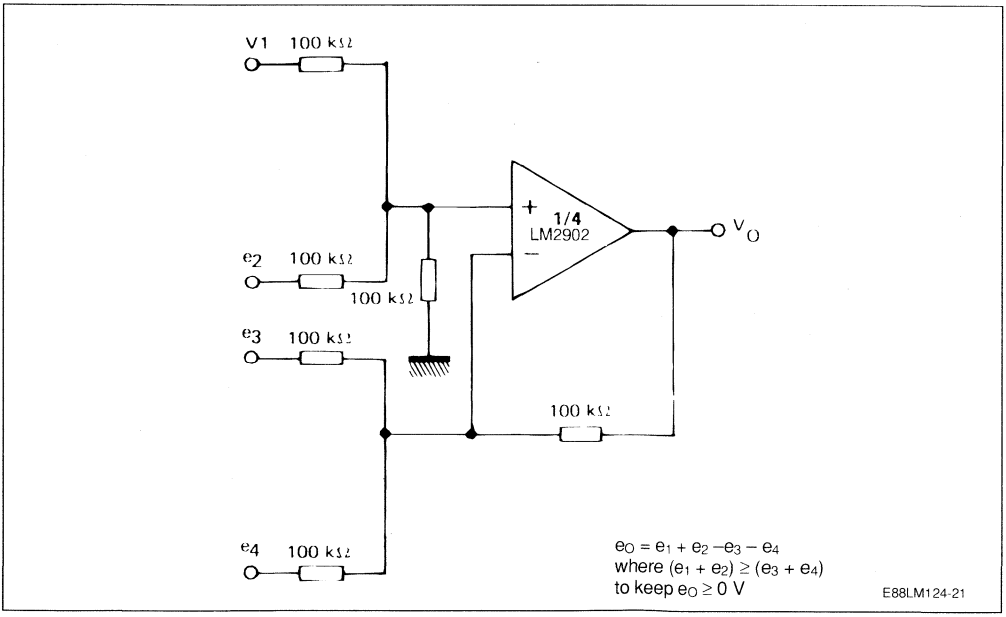
E88LM124-19

TYPICAL SINGLE - SUPPLY APPLICATIONS (continued)

NON-INVERTING DC GAIN

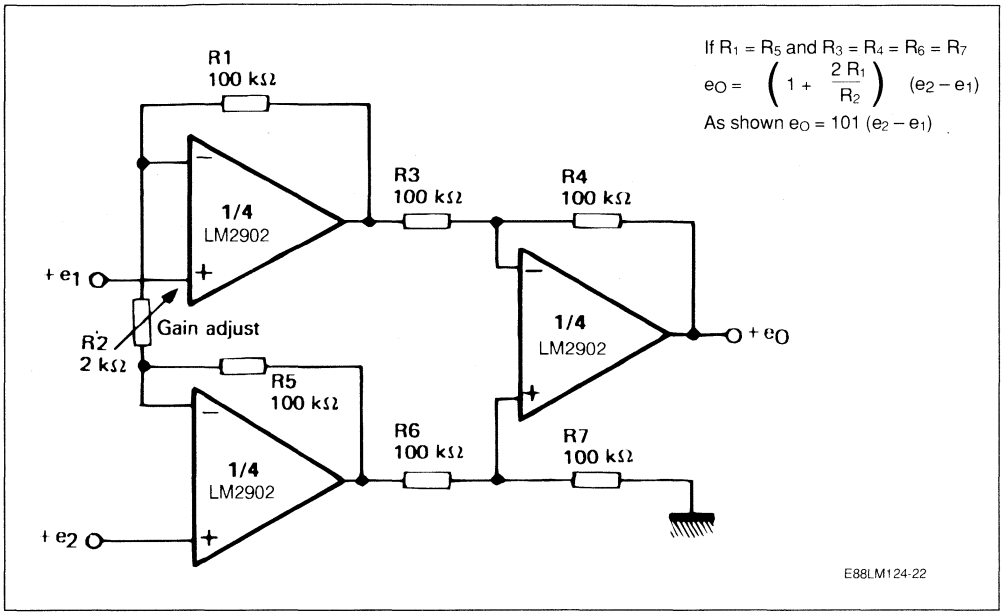


DC SUMMING AMPLIFIER

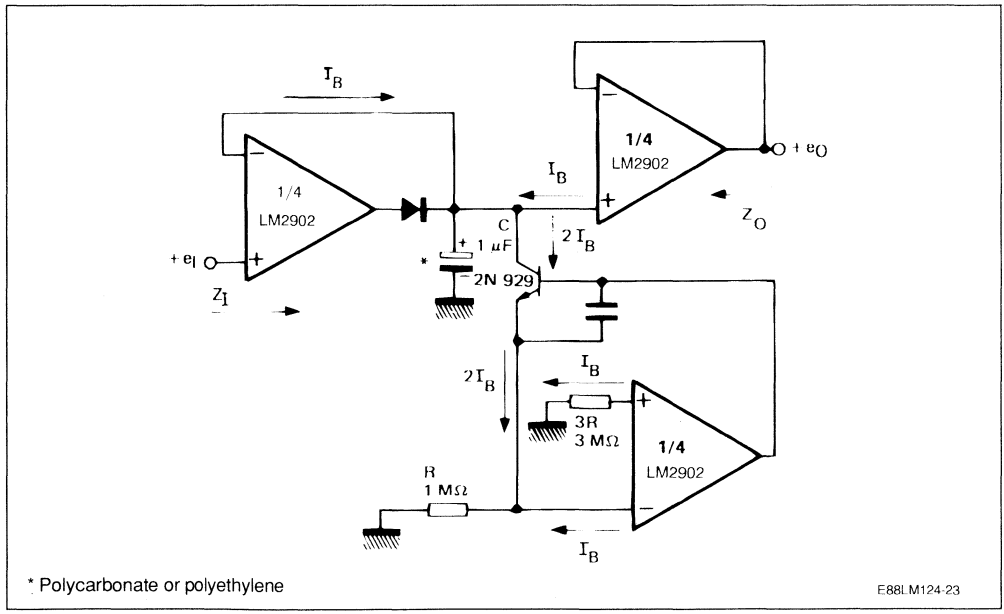


TYPICAL SINGLE SUPPLY APPLICATIONS (continued)

HIGH INPUT Z ADJUSTABLE GAIN DC INSTRUMENTATION AMPLIFIER

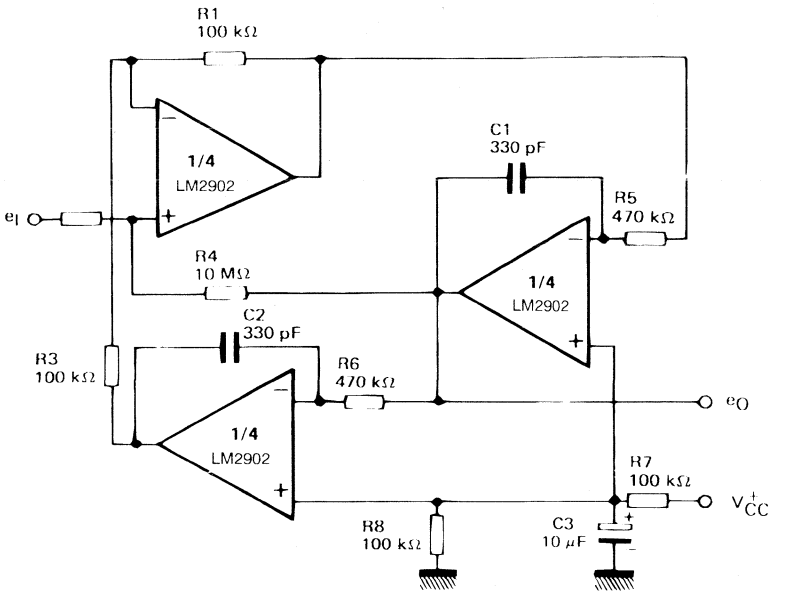


LOW DRIFT PEAK DETECTOR



TYPICAL SINGLE SUPPLY APPLICATIONS (continued)

ACTIVE BANDPASS FILTER



f_O = 1 kHz
Q = 50
A_V = 100 (40 dB)

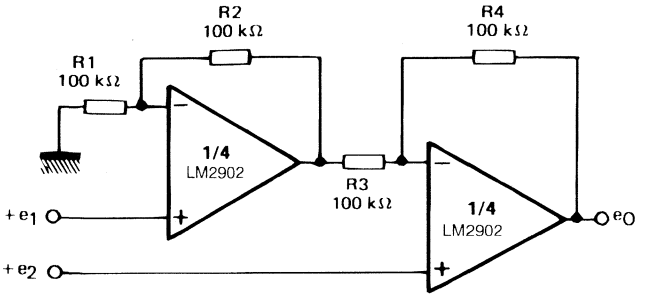
E88LM124-24

HIGH INPUT Z, DC DIFFERENTIAL AMPLIFIER

For $\frac{R_1}{R_2} = \frac{R_4}{R_3}$ (CMRR depends on this resistor ratio match)

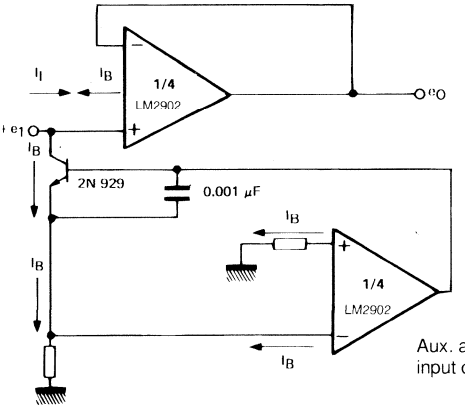
$$e_O = \left(1 + \frac{R_4}{R_3}\right)(e_2 - e_1)$$

As shown $e_O = 2(e_2 - e_1)$



E88LM124-25

USING SYMMETRICAL AMPLIFIERS TO REDUCE INPUT CURRENT (GENERAL CONCEPT)

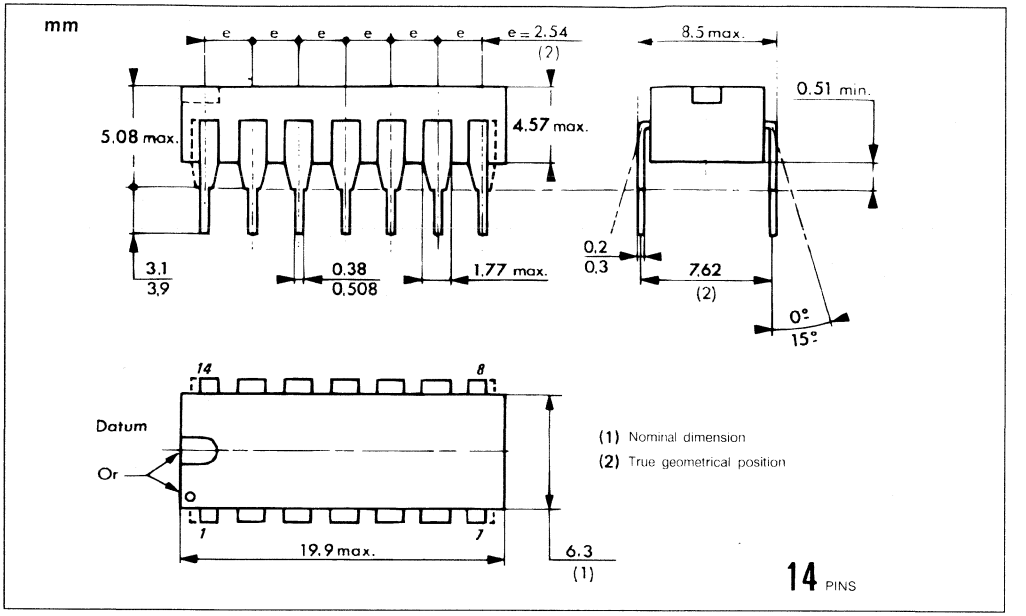


Aux. amplifier for
input current compensation

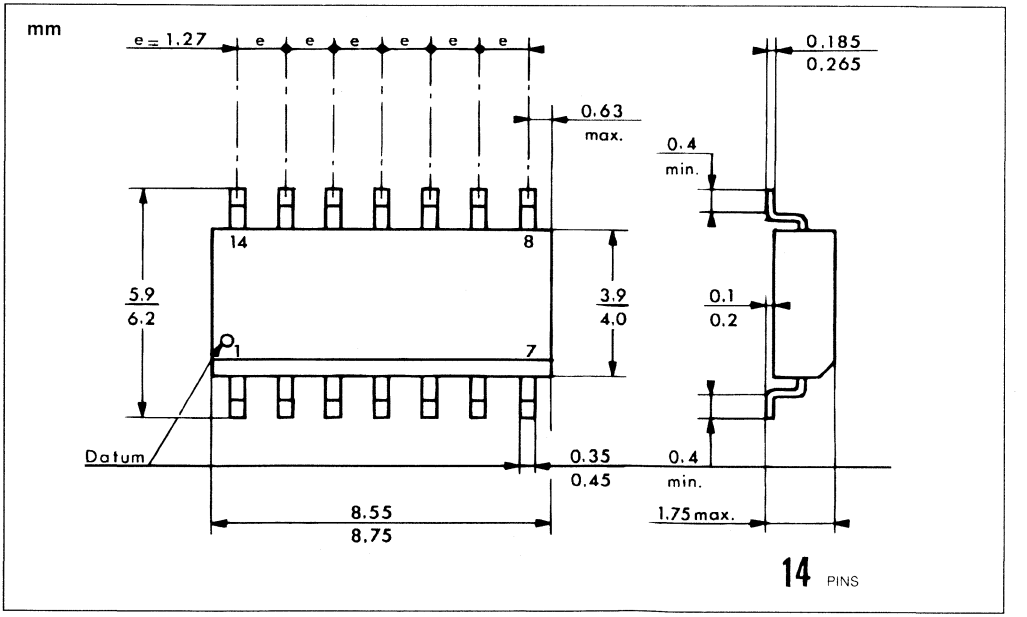
E88LM124-26

PACKAGE MECHANICAL DATA

14 PINS – N SUFFIX – PLASTIC PACKAGE – J SUFFIX – CERDIP PACKAGE



14 PINS – D SUFFIX – PLASTIC MICROPACKAGE



SGS-THOMSON MICROELECTRONICS

LM2903

LOW POWER LOW OFFSET VOLTAGE DUAL COMPARATOR

- WIDE SINGLE SUPPLY VOLTAGE RANGE OR DUAL SUPPLIES + 2 V TO + 36 V OR ± 1 V TO ± 18 V
- VERY LOW SUPPLY CURRENT DRAIN (0.8 mA) INDEPENDENT OF SUPPLY VOLTAGE (2 mW/comparator at + 5 V)
- LOW INPUT BIAS CURRENT : 25 nA TYP.
- LOW INPUT OFFSET CURRENT : ± 5 nA TYP.
- LOW INPUT OFFSET VOLTAGE : ± 1 mV TYP.
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- LOW OUTPUT SATURATION VOLTAGE : 250 mV TYP. (I_O = 4 mA)
- DIFFERENTIAL INPUT VOLTAGE RANGE TO THE SUPPLY VOLTAGE
- TTL, DTL, ECL, MOS, CMOS COMPATIBLE OUTPUTS

D
SO8
(Plastic Micropackage)

N
MINIDIP
(Plastic Package)

J
MINICERDIP
(Cerdip Package)

DESCRIPTION

This device consists of two independent precision voltage comparators.

This comparator is designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible.

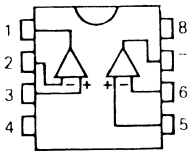
This comparator also have a unique characteris-tics in that the input common-mode voltage range includes ground even through operated from a single power supply voltage.

ORDER CODES

Part Number	Temperature Range	Package		
		N	D	J
LM2903	– 40 to + 105 °C	•	•	•
Example : LM2903N				

PIN CONNECTIONS (top view)

MINIDIP8
MINICERDIP8
SO8



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}

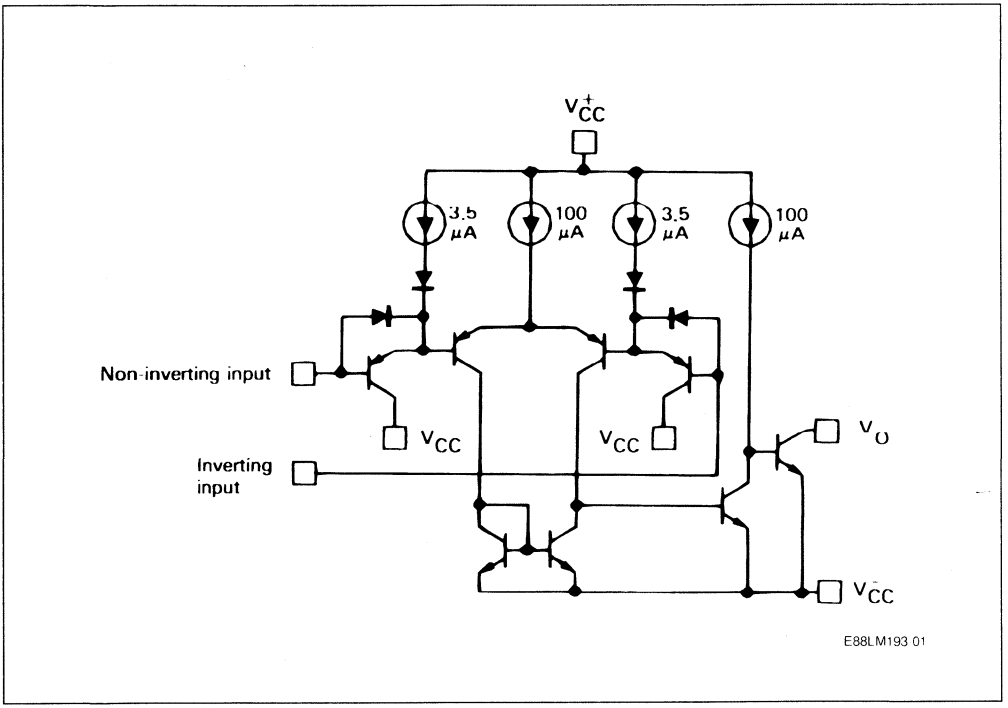
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM2903	Unit
V_{CC}	Supply Voltage	± 18 to 36	V
V_{ID}	Differential Input Voltage	36	V
V_I	Input Voltage	– 0.3 to + 36	V
–	Output Short-circuit to Ground – (note 2)	Continuous	–
P_{tot}	Power Dissipation – (note 1)	570	mW
T_{oper}	Operating Free-air Temperature Range	– 40 to + 105	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

Notes : 1. For operating at high temperatures the LM2903 must be derated based on a + 125 C max junction temperature and a thermal resistance of 175 C/W which applies for the devices soldered on a printed circuit board, operating in a still air ambient.
2. Short-circuit from the output to V_{CC} can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA, independent of the magnitude of V_{CC}.

SCHEMATIC DIAGRAM (1/2 LM2903)



CASE	Outputs	Inverting Inputs	Non–inverting Inputs	V_{CC}^-	V_{CC}^+
MINICERDIP8 SO8 MINIDIP8	1, 7	3, 5	2, 6	4	8

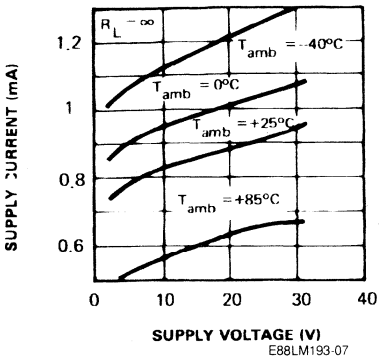
ELECTRICAL CHARACTERISTICS

LM2903 : $-40\ °C \leq T_{amb} \leq +105\ °C$
* = $\geq V_{CC}^{+} = +5$ V, $V_{CC}^{-} =$ GND

Symbol	Parameter	LM2903			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage – (note 3) $T_{amb} = +25\ °C$ $T_{min} \leq T_{amb} \leq T_{max}$	 – 5 – 9	 ± 1	 + 5 + 9	mV
I_{IB}	Input Bias Current – (note 4) $T_{amb} = +25\ °C$ $T_{min} \leq T_{amb} \leq T_{max}$	 – 250 – 400	 ± 25	 + 250 + 400	nA
I_{IO}	Input Offset Current $T_{amb} = +25\ °C$ $T_{min} \leq T_{amb} \leq T_{max}$	 – 50 – 150	 ± 5	 + 50 + 150	nA
A_{VD}	Large Signal Voltage Gain* ($V_{CC} = +15$ V, $V_a = +10$ V, $R_L > 15\ k\Omega$) $T_{amb} = +25\ °C$	 25	 200		V/mV
I_{CC}	Supply Current, no Load $V_{CC} = +30$ V (all comparators) $T_{amb} = 25\ °C$ $T_{min} \leq T_{amb} \leq T_{max}$		 0.4 1	 1 2.5	mA
V_I	Input Voltage Range – (note 5) $T_{amb} = +25\ °C$ $T_{min} \leq T_{amb} \leq T_{max}$		 0 0	 V_{CC}^{+} – 1.5 V_{CC}^{+} – 2	V
V_{ID}	Differential Input Voltage $V_I \geq 0$ V or if used $V_I^{-} = 0$ V (note 7)			 V_{CC}^{+}	V
I_{OS}	Output Sink Current $V_I^{+} = 0$ V, $V_I^{-} \geq = 1$ V, $V_O \leq = +1.5$ V $T_{amb} = 25\ °C$	 6	 16		mA
V_{OL}	Saturation Voltage $V_I^{-} \geq = 1$ V, $V_I^{+} = 0$ V, $I_{OS} \leq = 4$ mA $T_{amb} = 25\ °C$ $T_{min} < T_{amb} < T_{max}$	 250	 400 700		mV
I_{OH}	High Level Output Current $V_I^{+} \geq = 1$ V, $V_I^{-} = 0$ V $T_{amb} = 25\ °C$, $V_O = +5$ V $T_{min} \leq T_{amb} \leq T_{max}$, $V_O = +30$ V		 0.1	 1000	nA
t_{re}	Response Time $V_L = +5$ V, $R_L = 5;6\ k\Omega$ – (note 6) $T_{amb} = +25\ °C$		 1.3		µs
t_{rel}	Large Signal Response Time $e_I =$ TTL, $V_{re} = +1.4$ V, $V_L = 5$ V $T_{amb} = 25\ °C$		 300		ns

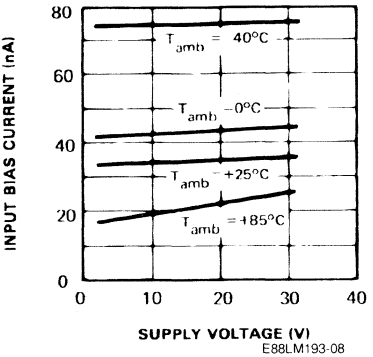
Notes :
3. At output switch point, $V_O = 1.4$ V, $R_S = 0$ with V_{CC}^{+} from 5 V to 30 V the full input common-mode range (0 V to V_{CC}^{+} - 1.5 V).
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading charge exists on the reference or input lines.
5. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC}^{+} - 1.5$ V, but either or both inputs can go to + 30 V without damage.
6. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.
7. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range the comparator will provide a proper output state. The low input voltage state must not be less than – 0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

SUPPLY CURRENT



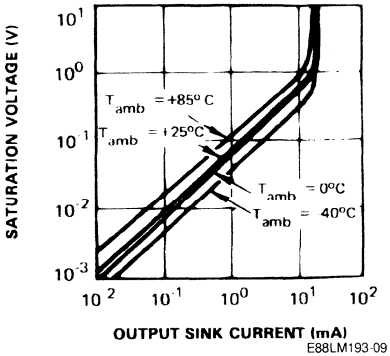
E88LM193-07

INPUT CURRENT



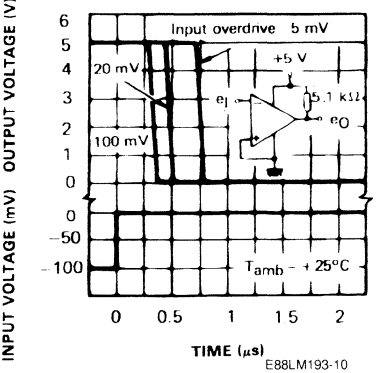
E88LM193-08

OUTPUT SATURATION VOLTAGE



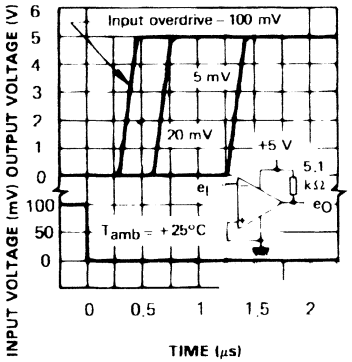
E88LM193-09

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - NEGATIVE TRANSITION



E88LM193-10

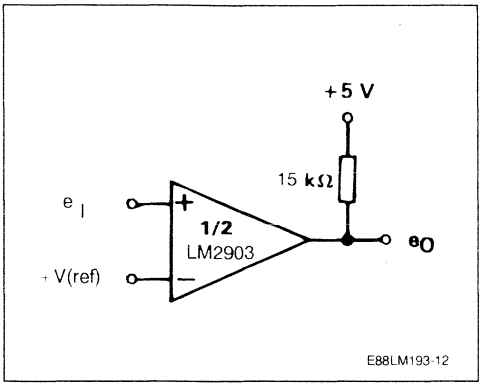
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - POSITIVE TRANSITION



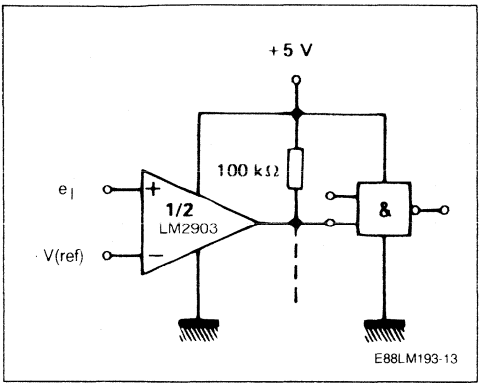
E88LM193-11

TYPICAL APPLICATIONS

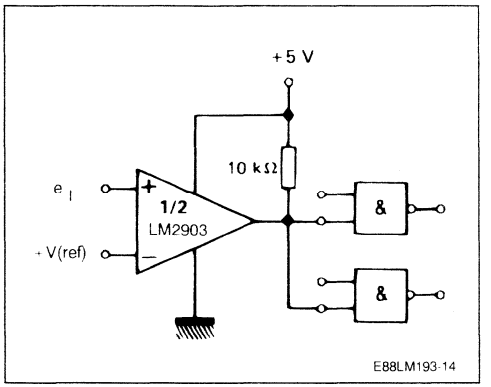
BASIC COMPARATOR



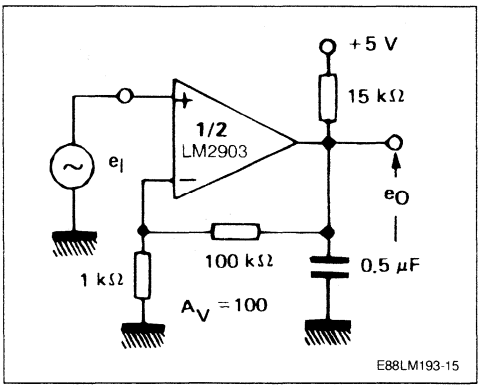
DRIVING CMOS



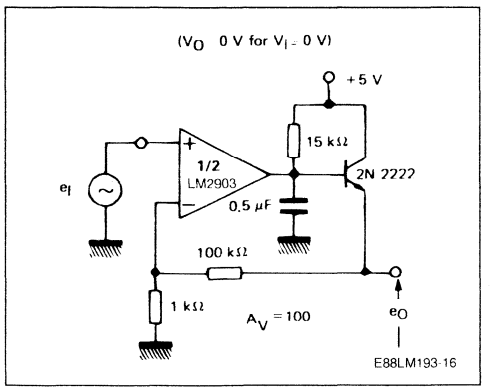
DRIVING TTL



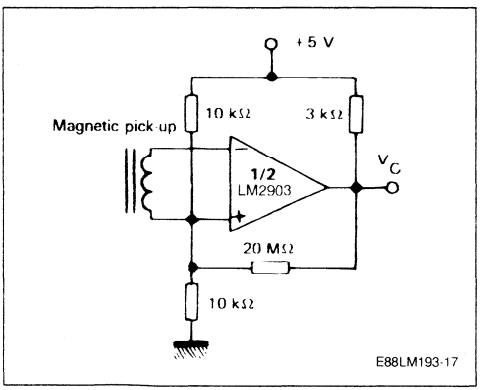
LOW FREQUENCY OP AMP



LOW FREQUENCY OP AMP

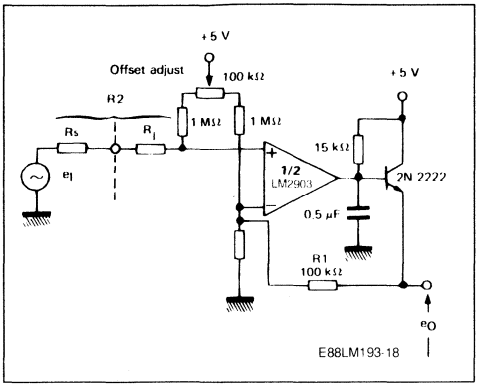


TRANSDUCER AMPLIFIER

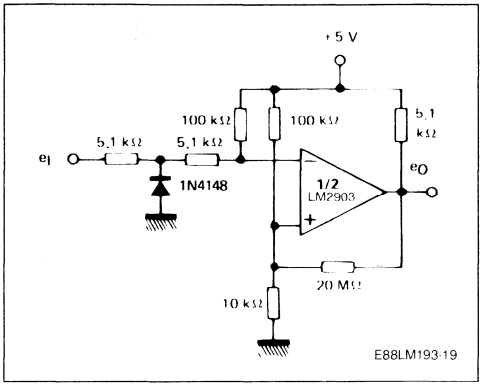


TYPICAL APPLICATIONS (continued)

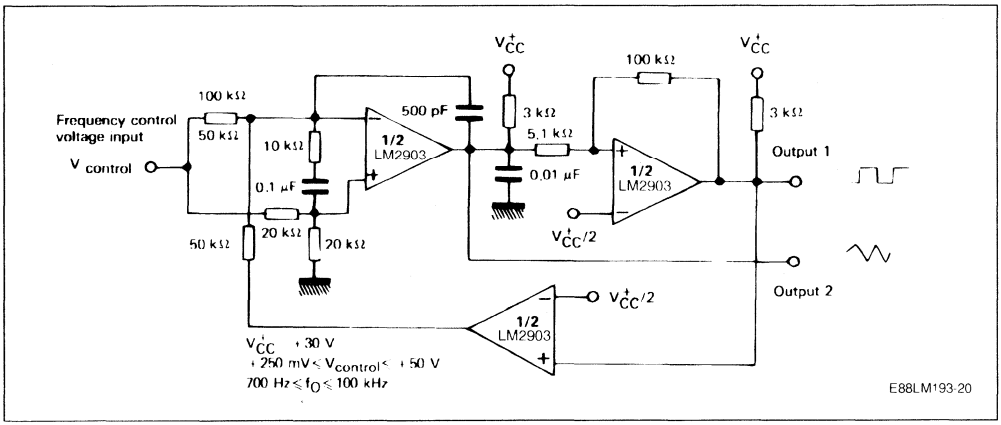
LOW FREQUENCY OP AMP WITH OFFSET ADJUST



ZERO CROSSING DETECTOR (SINGLE POWER SUPPLY)

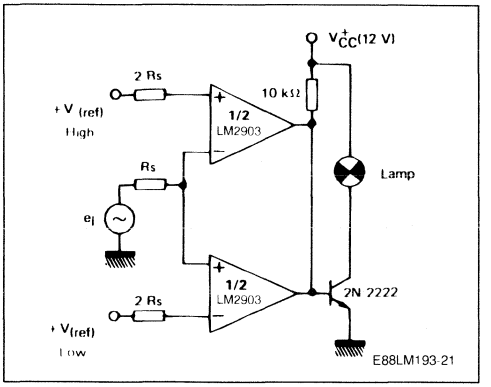


TWO DECADE HIGH FREQUENCY VCO

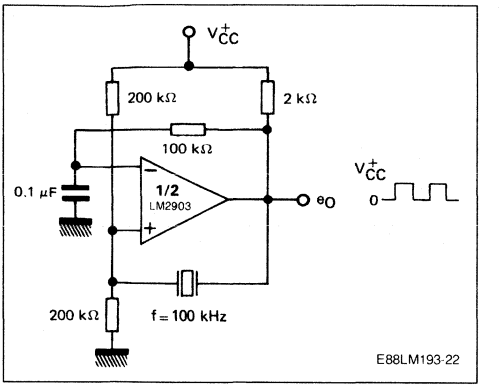


TYPICAL APPLICATIONS (continued)

LIMIT COMPARATOR

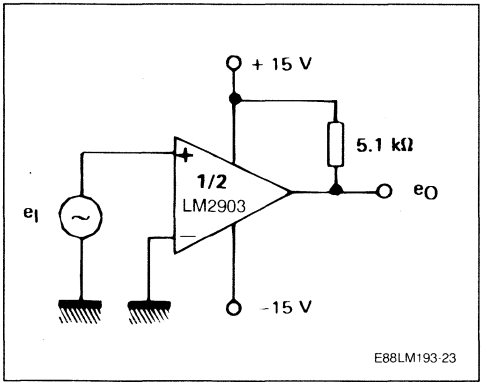


CRYSTAL CONTROLLED OSCILLATOR

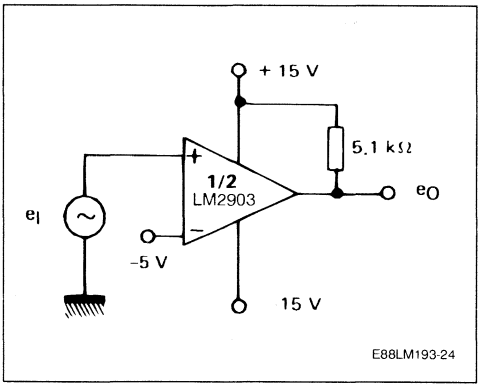


SPLIT-SUPPLY APPLICATIONS

Zero Crossing Detector

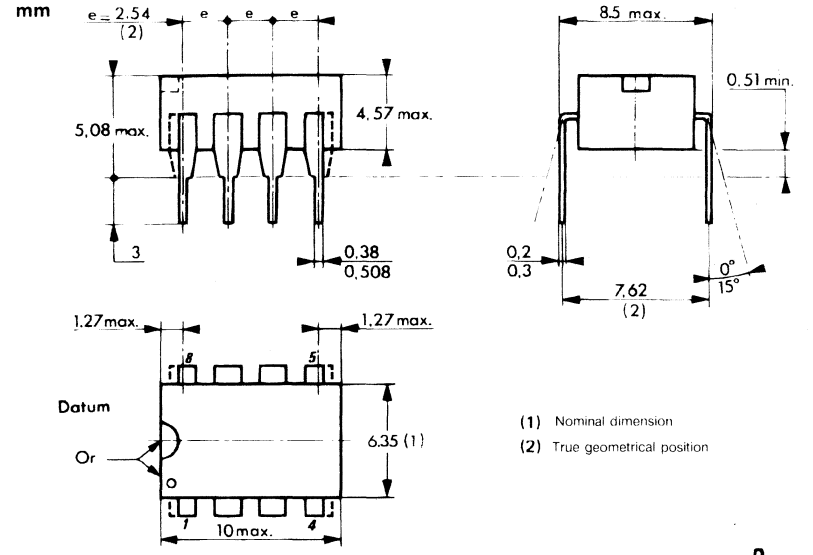


Comparator with a Negative Reference

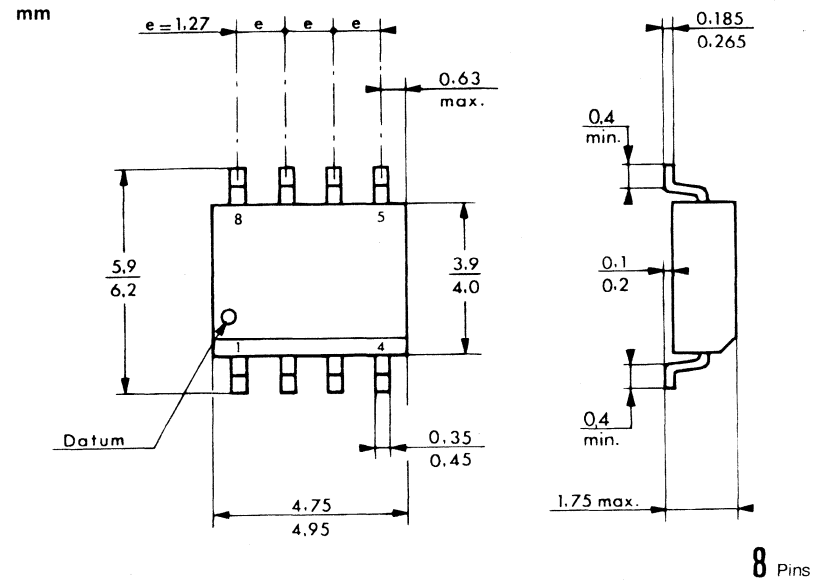


PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP



8 PINS – PLASTIC MICROPACKAGE (SO)



SGS-THOMSON MICROELECTRONICS

LM2904

LOW POWER DUAL OPERATIONAL AMPLIFIER

- INTERNALLY FREQUENCY COMPENSATED
- LARGE DC VOLTAGE GAIN : 100 dB
- WIDE BANDWIDTH (unity gain) : 1.1 MHz (temperature compensated)
- VERY LOW SUPPLY CURRENT/AMPLI 500 µA) - ESSENTIALLY INDEPENDENT OF SUPPLY VOLTAGE
- LOW INPUT BIAS CURRENT : 20 nA (temperature compensated)
- LOW INPUT OFFSET VOLTAGE : 2 mV
- LOW INPUT OFFSET CURRENT : 2 nA
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LARGE OUTPUT VOLTAGE SWING 0 V TO (V_{CC} – 1.5 V)

D
SO8
(Plastic Micropackage)

N
MINIDIP
(Plastic Package)
J
MINICERDIP
(Cerdip Package)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
LM2904	– 40 °C to + 105 °C	•	•	•

Example : LM2904D

DESCRIPTION

This circuit consists of two independent, high gain, internally frequency compensated which is designed specifically to operate from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, this circuit can be directly operated off the standard + 5 V power supply voltage which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

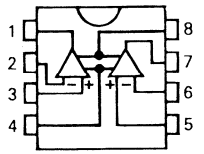
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even through operated from only a single power supply voltage.

The gain-bandwidth product is temperature compensated.

The input bias current is temperature compensated.

PIN CONNECTIONS (top view)

MINIDIP8
MINICERDIP8
SO8

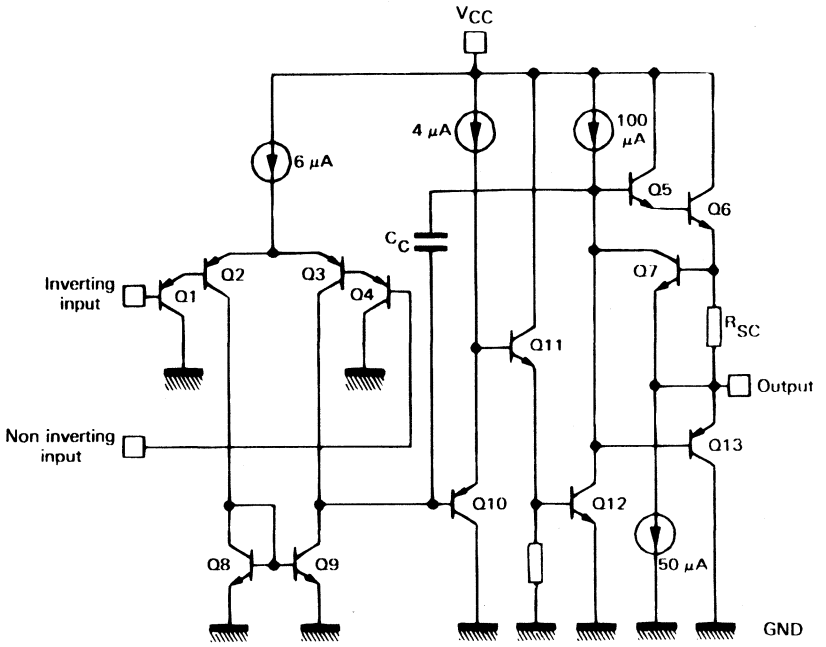


1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - Ground
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM2904	Unit
V_{CC}	Supply Voltage	+ 32	V
V_I	Input Voltage	– 0.3 to + 32	V
V_{ID}	Differential Input Voltage	+ 32	V
–	Output Short-circuit Duration (note 2)	Indefinite	–
P_{tot}	Power Dissipation	500	mW
I_{ID}	Input Current (note 1)	50	mA
T_{oper}	Operating Free-air Temperature Range	– 40 to +105	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

SCHEMATIC DIAGRAM (1/2 LM2904)



– Single Supply 3 V to 30 V
– Dual supplies ± 1.5 V to ± 15 V

CASE	Inverting Inputs	Non - inverting Inputs	GND	V_{CC}	Outputs
MINIDIP8 MINICERDIP8 - SO8	2-6	3-5	4	8	1-7

ELECTRICAL CHARACTERISTICS

$V_{\overset{+}{C}C}$ = + 5 V, $V_{\overset{-}{C}C}$ = Ground, V_O = 1.4 V
(unless otherwise specified)

LM2904 : $-40 \leq T_{amb} \leq +105$ °C

Symbol	Parameter		LM2904 Min.	LM2904 Typ.	LM2904 Max.	Unit
V_{IO}	Input Offset Voltage (note 3) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$			2	5 7	mV
I_{IO}	Input Offset Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$			2	20 40	nA
I_{IB}	Input Bias Current (note 4) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$			20	100 200	nA
A_{VD}	Large Signal Voltage Gain (V_{CC} = + 15 V, $R_L \geq 2$ kΩ) (V_O = 1.4 V to 11.4 V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10$ KΩ) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		65 65	100		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25 °C, V_{CC} = + 5 V $T_{min} \leq T_{amb} \leq T_{max}$ T_{amb} = 25 °C, V_{CC} = + 30 V $T_{min} \leq T_{amb} \leq T_{max}$			0.7 1	1.2 1.2 2 2	mA
V_I	Input Voltage Range (note 6) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		0 0		V_{CC} – 1.5 V_{CC} – 2	V
CMR	Common-mode Rejection Ratio (R_S < 10 kΩ) (note 3) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		70 60	85		dB
I_O	Output Short-circuit Current (V_I^+ = + 1 V, V_I = 0 V) T_{amb} = 25 °C, V_{CC} = + 15 V (note 2) $T_{min} \leq T_{amb} \leq T_{max}$		20 10	40	60	mA
I_{sink}	Output Current Sink (V_I^+ = - 1 V, V_I = 0 V) V_{CC} = + 15 V V_O = + 0.2 V	T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$ T_{amb} = + 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	10 10 12 12	20 50		mA µA
V_{OPP}	Output Voltage Swing T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	$R_L \geq 2$ kΩ $R_L \geq 2$ kΩ	0 0		V_{CC} – 1.5 V_{CC} – 2	V

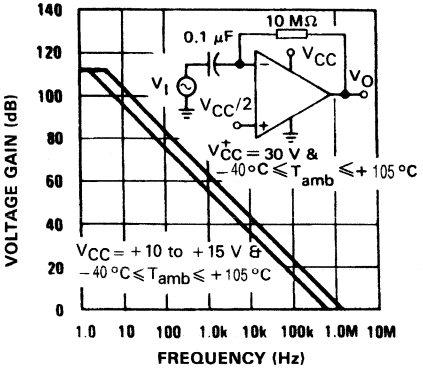
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		LM2904			Unit
			Min.	Typ.	Max.	
V_{OH}	High Level Output Voltage (V_{CC} = 30 V)					V
	T_{amb} = 25 °C	R_L = 2 kΩ	26	27		
	$T_{min} \leq T_{amb} \leq T_{max}$		26			
	T_{amb} = 25 °C	R_L = 10 kΩ	27	28		
	$T_{min} \leq T_{amb} \leq T_{max}$		27			
V_{OL}	Low Level Output Voltage ($R_L \geq 10$ kΩ)					mV
	T_{amb} = 25 °C			5	20	
	$T_{min} \leq T_{amb} \leq T_{max}$				20	
S_{VO}	Slew-rate (V_I = 0.5 to 3 V, R_L = 2 kΩ, $C_L \leq$ 100 pF, T_{amb} = 25 °C, unity gain) V_{CC} = 15 V		0.3	0.6		V/µs
GBP	Gain Bandwidth Product (f = 100 kHz, T_{amb} = 25 °C, V_{CC} = 30 V V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)		0.7	1.1	1.6	MHz
THD	Total Harmonic Distortion (f = 1 kHz, A_v = 20 dB, R_L = 2 kΩ, V_{CC} = 30 V $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_O = 2 V_{PP})			0.02		%
V_n	Equivalent Input Noise Voltage (f = 1 kHz, R_g = 100 Ω, V_{CC} = 30 V)			55		nV/√Hz
DV_{io}	Input Offset Voltage Drift $T_{min} \leq T_{amb} \leq T_{max}$			7	30	µV/°C
DI_{io}	Input Offset Current Drift $T_{min} \leq T_{amb} \leq$ 25 °C			10	300	pA/°C
V_{O1}/V_{O2}	Channel Separation (note 5) 1 kHz ≤ f ≤ 20 kHz			120		dB

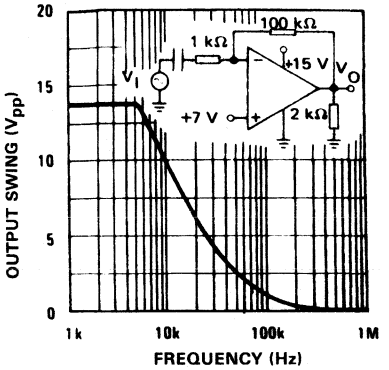
Notes : 1. This input only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps.
In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative.
This is not destructive and normal output will set up again for input voltage higher than – 0.3V.

2. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15V. The maximum output current is approximatively 40mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
3. V_O = 1.4V, R_S = 0, 5V < V_{CC} < 30V, 0 < V_I < V_{CC} – 1.5V.
4. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
5. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequences.
6. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC} – 1.5V.
But either or both inputs can go to + 32V without damage.

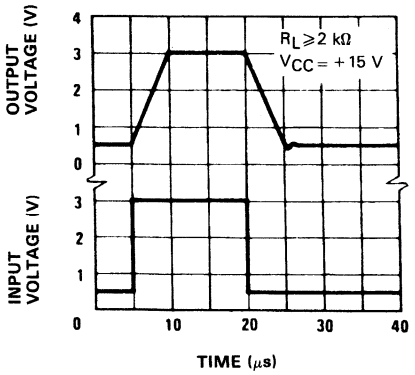
OPEN LOOP FREQUENCY RESPONSE (Note 3)



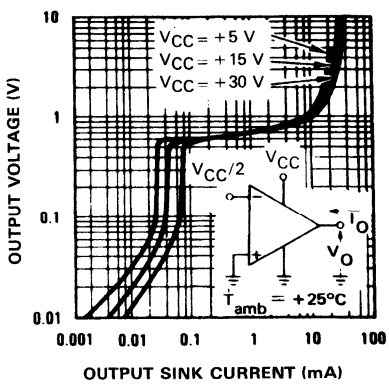
LARGE SIGNAL FREQUENCY RESPONSE



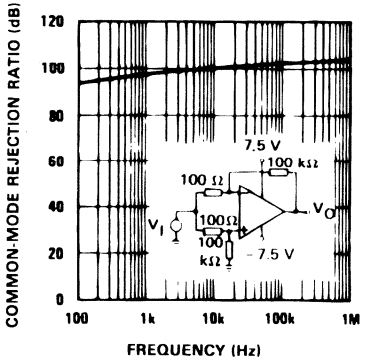
VOLTAGE FOLLOWER PULSE RESPONSE



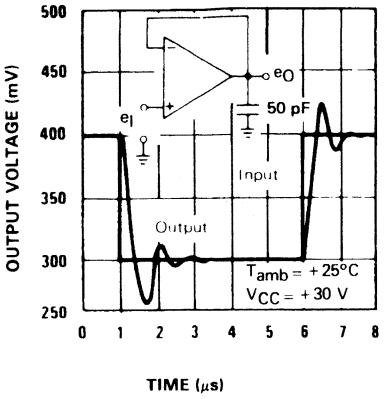
OUTPUT CHARACTERISTICS



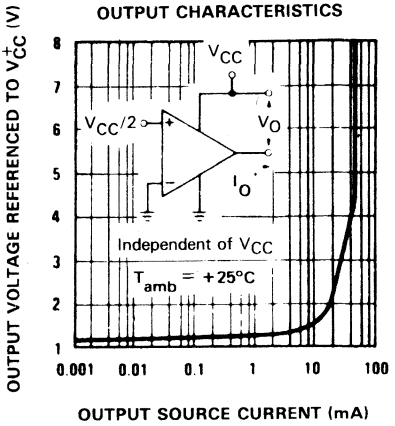
COMMON-MODE REJECTION RATIO



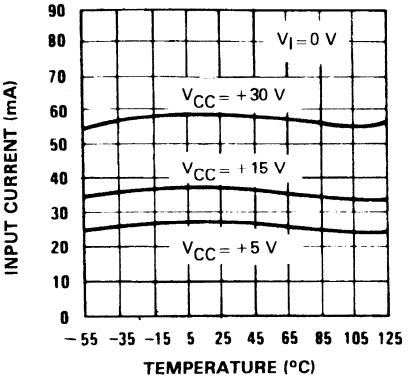
VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



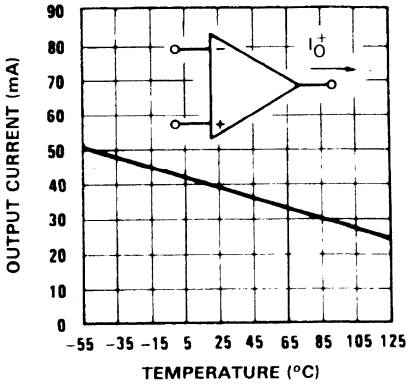
OUTPUT CHARACTERISTICS



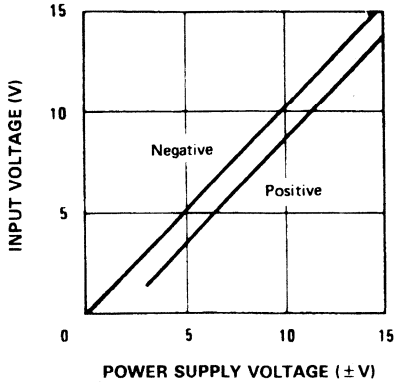
INPUT CURRENT (Note 1)



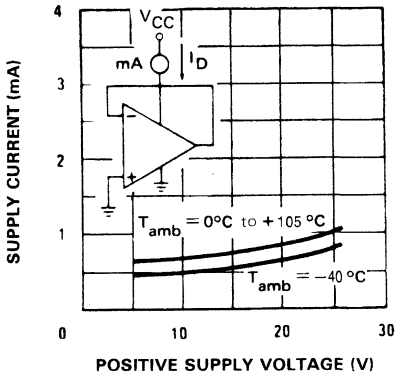
CURRENT LIMITING (Note 1)



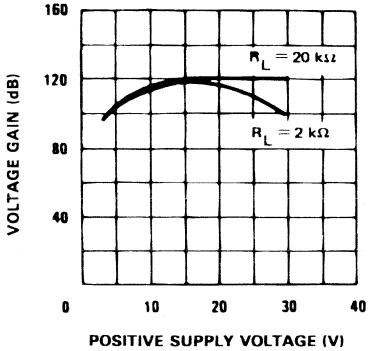
INPUT VOLTAGE RANGE



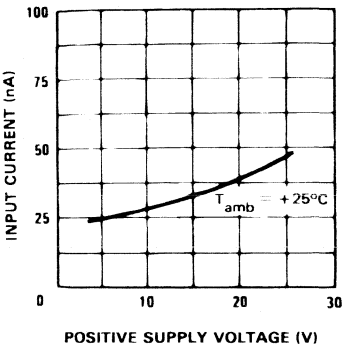
SUPPLY CURRENT



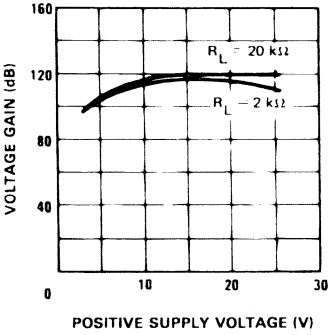
VOLTAGE GAIN



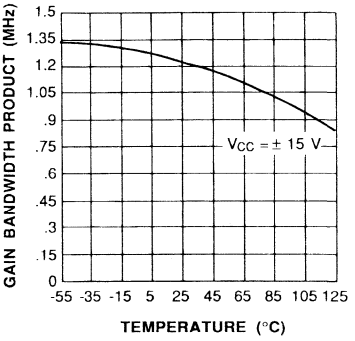
INPUT CURRENT



VOLTAGE GAIN

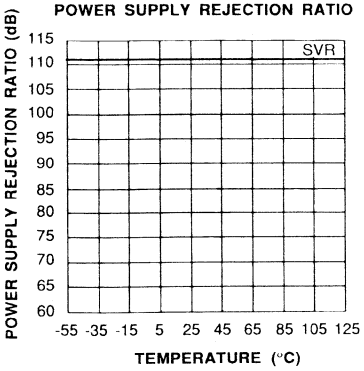


GAIN BANDWIDTH PRODUCT

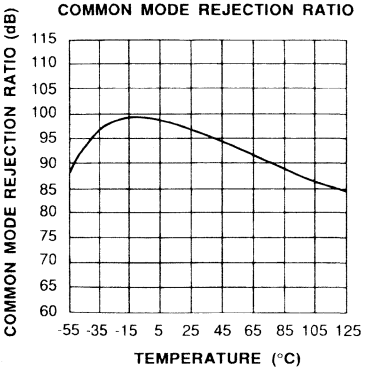


E88LM108-28

POWER SUPPLY REJECTION RATIO



COMMON MODE REJECTION RATIO

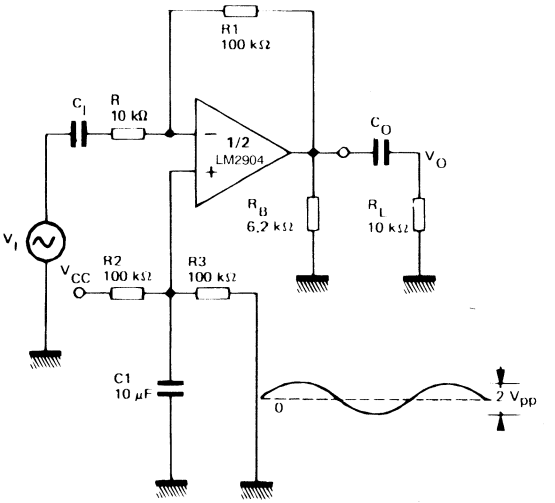


E88LM108-27

TYPICAL APPLICATIONS (single supply voltage) V_{CC} = + 5 V_{DC}

AC COUPLED INVERTING AMPLIFIER

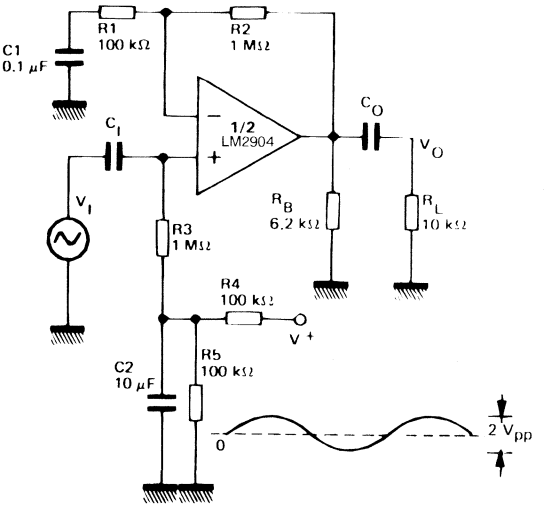
$$A_V = \frac{-R1}{R} \quad \text{(As shown } A_V = -10\text{)}$$



E88LM108-21

AC COUPLED NON INVERTING AMPLIFIER

$$\text{Gain} = +1\ \frac{R2}{R1} \quad \text{(As shown, Gain = 11)}$$



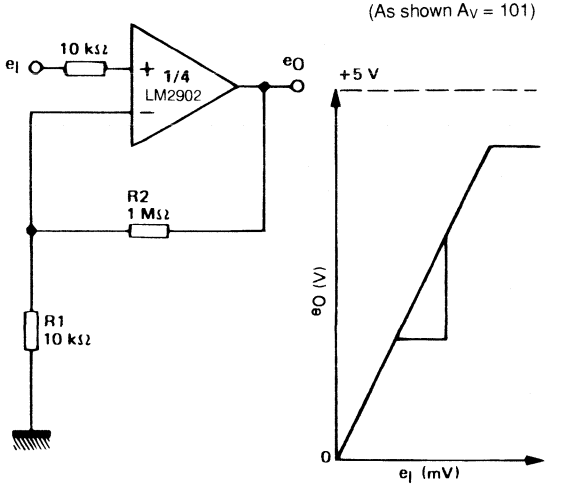
E88LM108-22

TYPICAL SINGLE - SUPPLY APPLICATIONS (continued)

NON-INVERTING DC GAIN

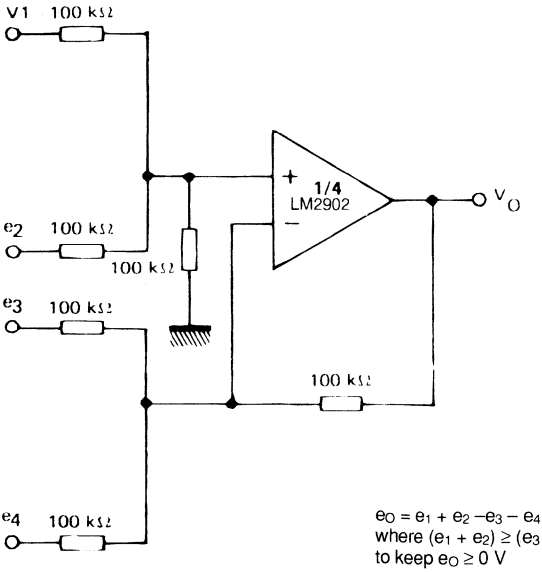
$$A_V = \frac{R2}{R1}$$

(As shown $A_V = 101$)



E88LM124-20

DC SUMMING AMPLIFIER

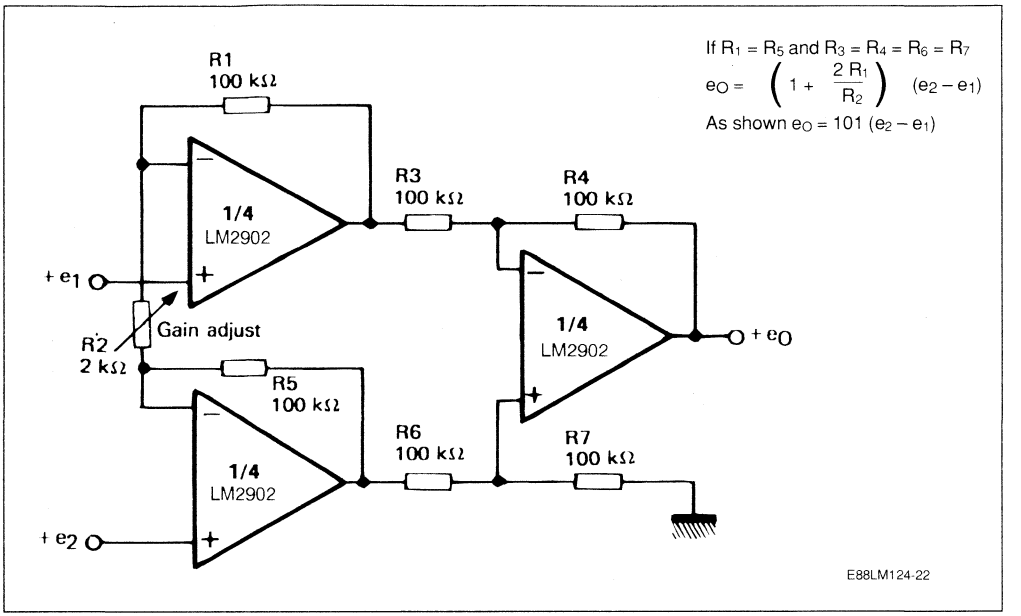


$e_O = e_1 + e_2 - e_3 - e_4$
where $(e_1 + e_2) \geq (e_3 + e_4)$
to keep $e_O \geq 0$ V

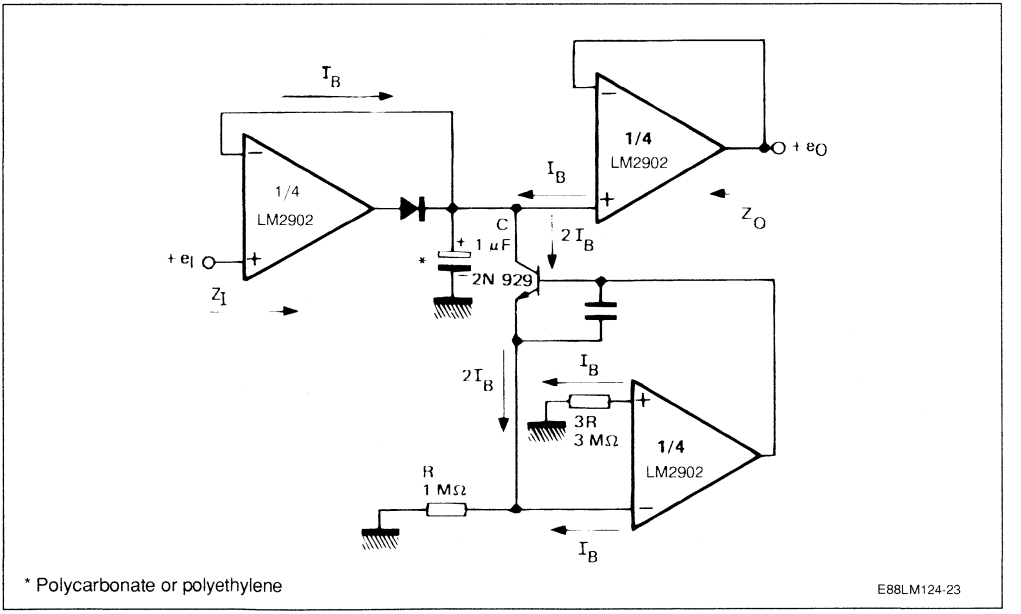
E88LM124-21

TYPICAL SINGLE SUPPLY APPLICATIONS (continued)

HIGH INPUT Z ADJUSTABLE GAIN DC INSTRUMENTATION AMPLIFIER

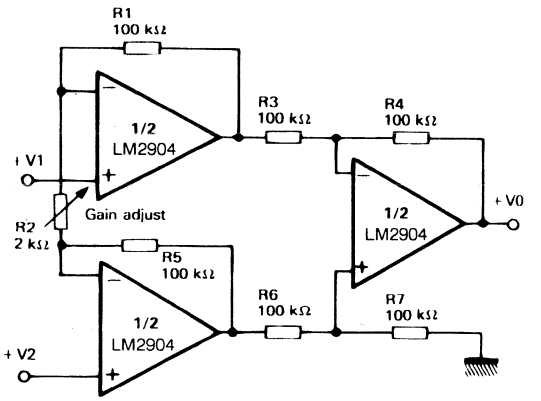


LOW DRIFT PEAK DETECTOR



TYPICAL APPLICATIONS (single supply voltage) V_{CC} = + 5 V_{DC} (continued)

HIGH INPUT Z ADJUSTABLE-GAIN DC INSTRUMENTATION AMPLIFIER



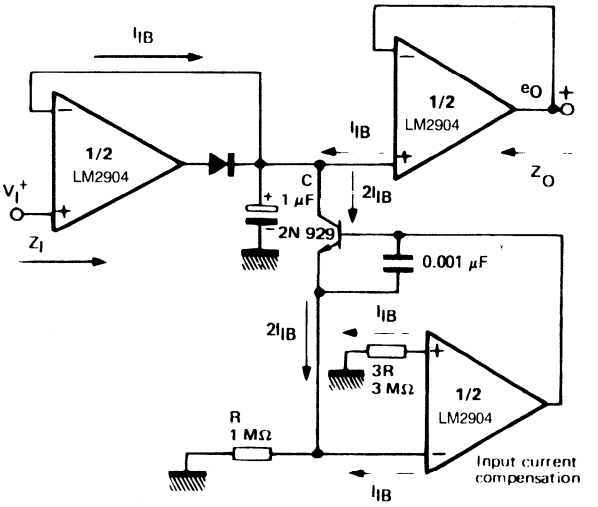
If R1 = R5 and R3 = R4 = R6 = R7

$$V_O = \left(1 + \frac{2R1}{R2}\right)(V2 - V1)$$

As shown : $V_O - 101\ (V2 - V1)$

E88LM108-27

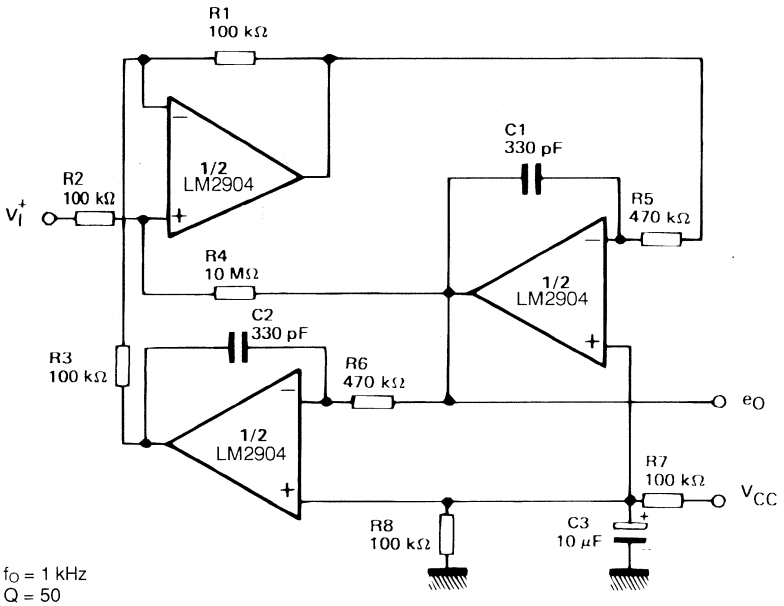
LOW DRIFT PEAK DETECTOR



E88LM108-28

TYPICAL APPLICATIONS (single supply voltage) V_{CC} = + 5 V_{DC} (continued)

ACTIVE BAND-PASS FILTER

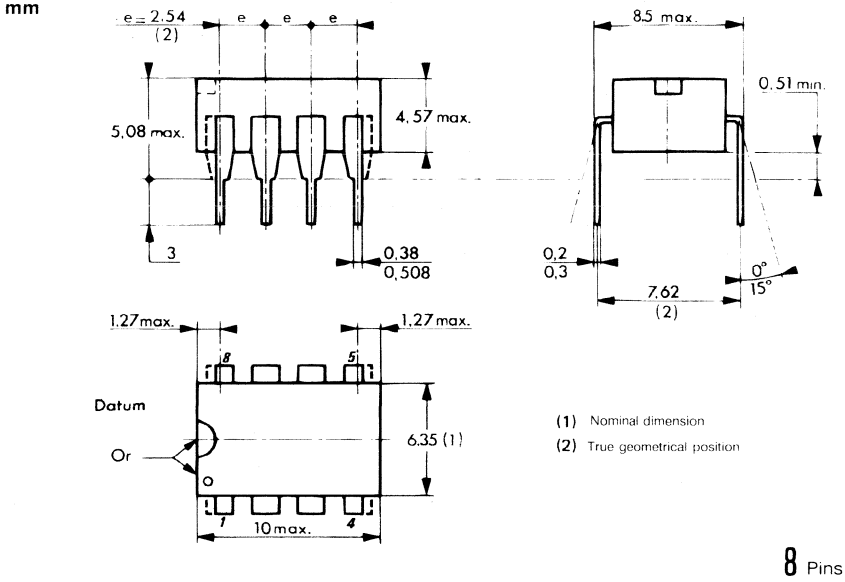


f_O = 1 kHz
Q = 50
A_V = 100 (40 dB)

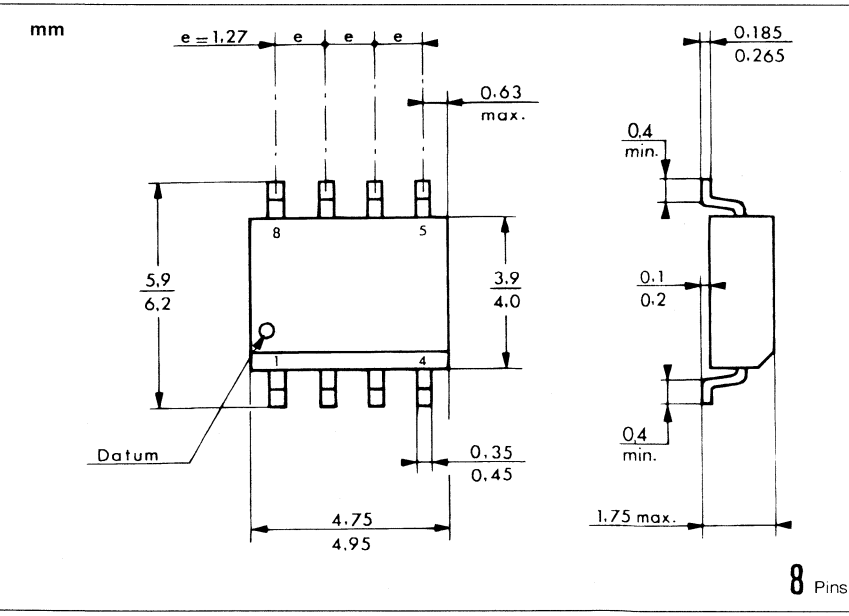
E88LM108-29

PACKAGE MECHANICAL DATA (continued)

8 PINS - PLASTIC DIP OR CERDIP



8 PINS – PLASTIC MICROPACKAGE (SO)



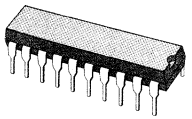
SGS-THOMSON MICROELECTRONICS

ST6010/11/12 ST6013/14

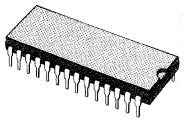
8 BIT HCMOS MICROCONTROLLERS WITH A/D CONVERTER

PRELIMINARY DATA

- 8-BIT ARCHITECTURE
- STATIC HCMOS OPERATION
- 3.0 TO 6.0V SUPPLY OPERATING RANGE
- 3.25µS TCYCLE (with 4MHz clock)
- RUN, WAIT & STOP MODES
- USER ROM : 1828 BYTES
- RESERVED ROM : 220 BYTES
- DATA ROM : 32 BYTES
- DATA RAM : 32 BYTES
- 20-PIN DIP OR SO PLASTIC PACKAGE (ST6010, ST6011,ST6014)
- 28-PIN DIP ON SO PACKAGE (ST6012, ST6013)
- 6 PUSH-PULL BIDIRECTIONAL INPUTS/OUTPUTS WITH 5mA DRIVING CAPABILITY (ST6010)
- 7 PUSH-PULL BIDIRECTIONAL INPUTS/OUTPUTS WITH 5mA DRIVING CAPABILITY (ST6011,ST6012)
- 8 PUSH-PULL BIDIRECTIONAL INPUTS/OUTPUTS WITH 5mA DRIVING CAPABILITY (ST6013, ST6014)
- 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER (Timer)
- HARDWARE ACTIVATED DIGITAL WATCHDOG FUNCTION (ST6010, ST6012, ST6013, ST6014)
- SOFTWARE ACTIVATED DIGITAL WATCHDOG/TIMER (ST6011)
- 8-BIT A/D CONVERTER WITH 3 (ST6011, ST6014), 7 (ST6010) AND 9 (ST6012, ST6013) ANALOG INPUTS AND SEPARATE ANALOG REFERENCE VOLTAGE (not available in ST6010)
- ONE LEVEL OR EDGE SENSITIVE EXTERNAL INTERRUPT INPUT
- ON-CHIP CLOCK OSCILLATOR
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- WAIT, STOP (ST6011 only) AND BIT MANIPULATION INSTRUCTIONS
- TRUE LIFO 4 LEVEL STACK
- 9 POWERFUL ADDRESSING MODES
- THE ACCUMULATOR, THE X, Y, V & W REGISTERS, THE PORT AND PERIPHERALS DATA/CONTROL REGISTERS ARE ADDRESSED IN THE DATA SPACE AS RAM LOCATIONS
- THE DEVELOPMENT TOOL OF THE ST601X MICROCONTROLLER FAMILY CONSISTS OF THE EMS6-HW/B1X EMULATION AND DEVELOPMENT PACKAGE CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN IBM PC. THE ST60P1X PIGGYBACK ROMLESS VERSION IS AVAILABLE



DIP-20



DIP-28

(Order Codes at the end of the datasheet)

Figure 1 : ST6010 - ST6011 - ST6012 Pin Configurations.

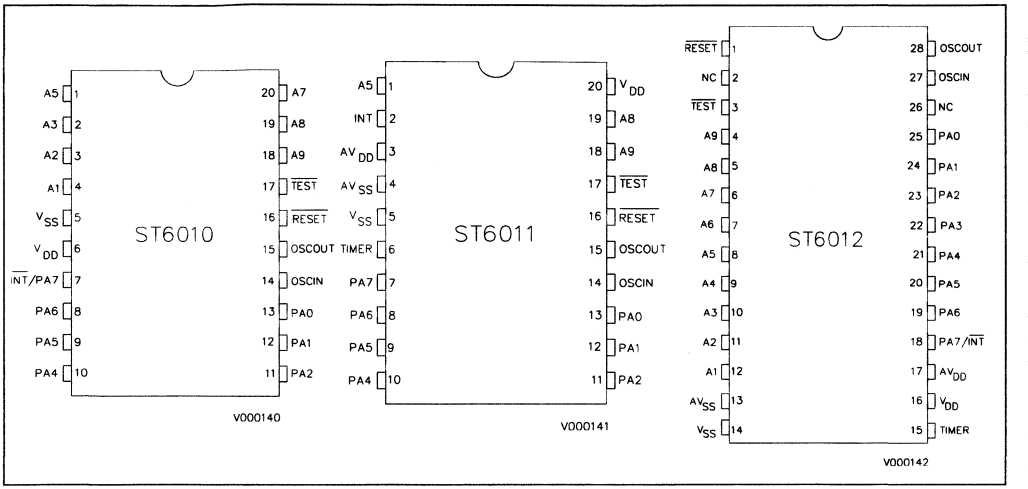
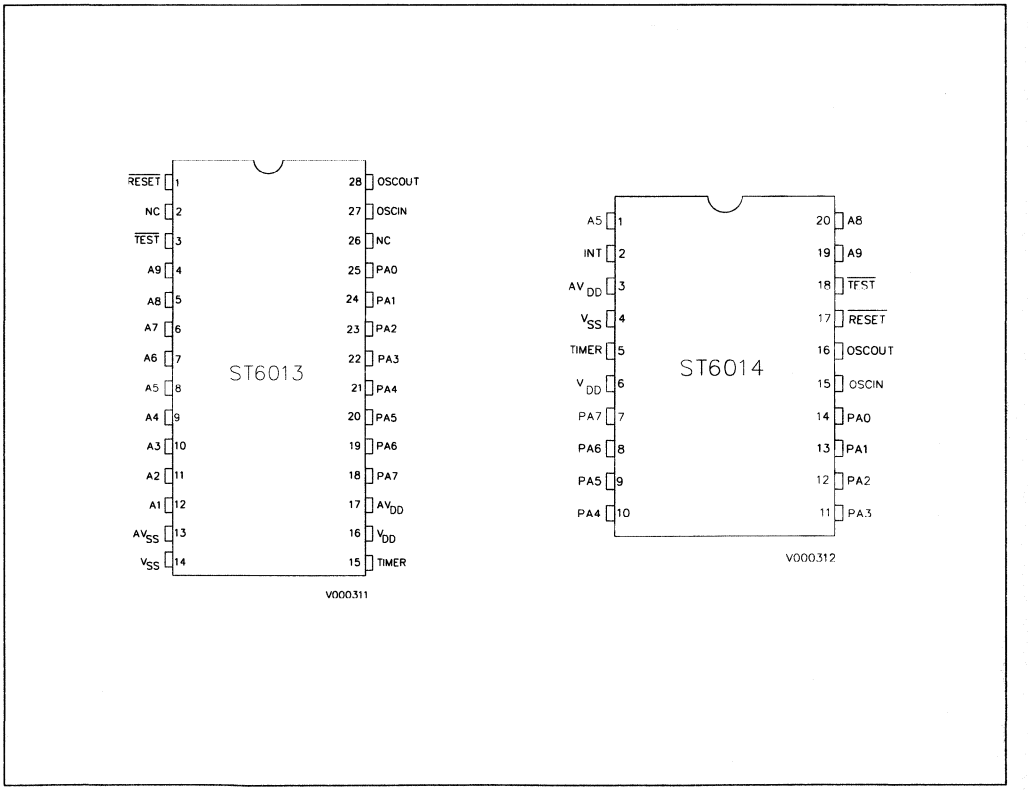


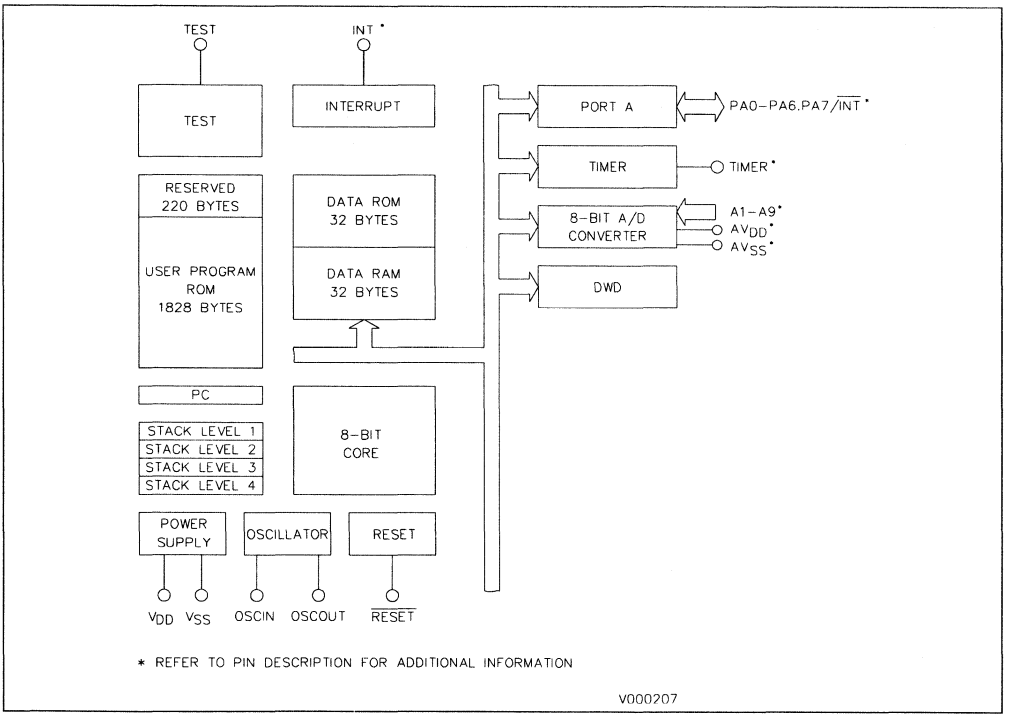
Figure 2 : ST6013 - ST6014 Pin Configurations.



GENERAL DESCRIPTION

The ST6010, ST6011, ST6012, ST6013 and ST6014 microcontrollers are members of the 8-bit HCMOS ST60XX family, a series of devices oriented to low-medium complexity applications. All ST60XX members are based on a building block approach: to a common core is associated a combination of on-chip peripherals (macrocells) available from a standard library to form around the core all the existing and future ST6 devices. These peripherals are designed with the same core technology giving full compatibility, short design and testing time. The macrocells of the ST6010/11/12/13/14 are: the Timer that includes an 8-bit counter with a 7-bit software programmable prescaler (Timer), the 8-bit A/D Converter with a different number of analog inputs (ADC) with separate analog reference voltage (ST6012, ST6014 only), the hardware (ST6010/12/13/14) or software (ST6011) activated digital watchdog/timer (DWD). Thanks to these peripherals these devices are well suited for automotive and industrial controls applications.

Figure 3 : ST601X Block Diagram.



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN, OSCOUT. These pins are internally connected to the on-chip oscillator circuit. A crystal quartz or a ceramic resonator has to be connected between these two pins in order to allow a right operating of the MCU. A signal can be also provided to the OSCIN pin as external clock. The OSCIN pin is the input pin, the OSCOUT pin is the output pin.

$\overline{\text{RESET}}$. The active low RESET pin is used to restart the microcontroller at the beginning of its program.

$\overline{\text{TEST}}$. The TEST (mode select) pin is used to place the MCU into special operating mode. If TEST is held at +5V the MCU enters the normal operating mode. If TEST is held at zero when reset is active the test operating mode is automatically selected (the user should connect this pin to V_{DD} for normal operation).

INT/PA7 (*). The INT pin provides the capability for asynchronous applying an external interrupt to the MCU. This pin is active low on ST6010, ST6012 and is connected together with the I/O line PA7. On ST6014 is active low but is not connected to I/O line PA7. On ST6011 the interrupt pin is falling edge sensitive while on ST6013 the external interrupt line is not available. (*) The PA7/INT connection is implemented only on ST6010 and ST6012.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input or an output under software control of the data direction register. Port A has a push-pull output configuration with 5mA drive capability and schmitt trigger inputs. (*) PA3 is not available in ST6010 and ST6011. On ST6010 and ST6012 PA7 and the external interrupt line are connected together.

A1-A9. These 9 pins are the analog inputs for the on-chip 8-bit A/D converter. The user can select by software which analog channel has to be converted. The following table summarizes the A/D pins available for the different devices.

Table 1 : A/D Available Inputs for Different ST601X Products.

A/D Input	ST6010	ST6011	ST6012	ST6013	ST6014
A1	Pin 4	NA	Pin 12	Pin 12	NA
A2	Pin 3	NA	Pin 11	Pin 11	NA
A3	Pin 2	NA	Pin 10	Pin 10	NA
A4	NA	NA	Pin 9	Pin 9	NA
A5	Pin 1	Pin 1	Pin 8	Pin 8	Pin 1
A6	NA	NA	Pin 7	Pin 7	NA
A7	Pin 20	NA	Pin 6	Pin 6	NA
A8	Pin 19	Pin 19	Pin 5	Pin 5	Pin 20
A9	Pin 18	Pin 18	Pin 4	Pin 4	Pin 19

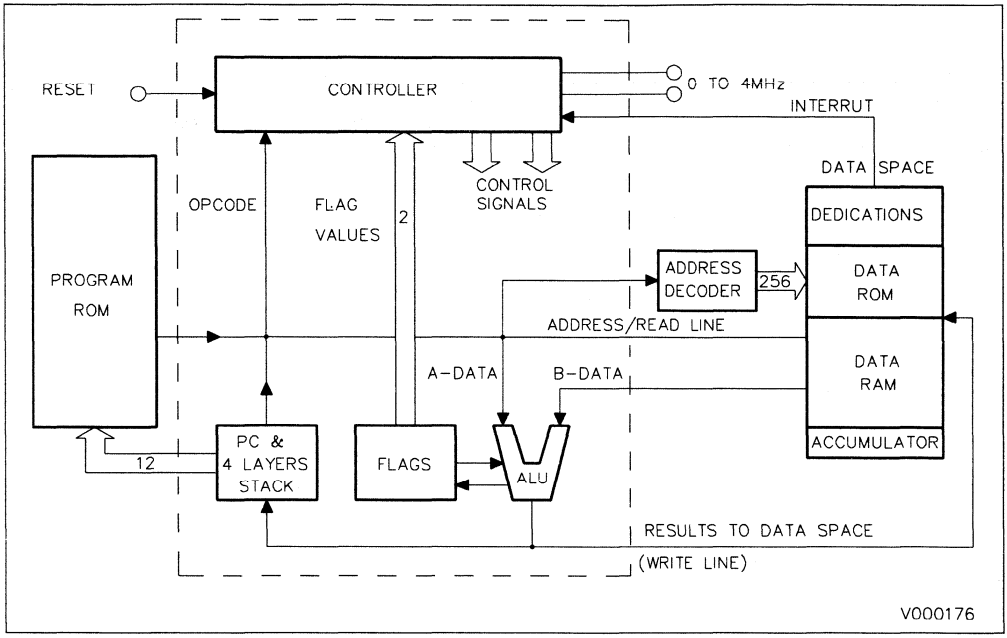
AV_{DD},AV_{SS}. These pins are used to provide a separate reference voltage to the A/D converter in order to allow high precision conversion.These pins are not available on ST6010. On ST6014 only AV_{DD} is available.

TIMER. This is the timer I/O pin. In input mode it is connected to the prescaler and acts as external timer clock (DOUT=TOUT=0) or as control gate for the internal timer clock (DOUT=1,TOUT=0). In the output mode the timer pin outputs the data bit when a time out occurs. This pin is not available in ST6010.

ST60XX CORE

The CORE of the ST60XX Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control buses. The in-core communications are arranged as shown in the following block diagram figure; the controller being externally linked to both the reset and the oscillator while the core is linked to the dedicated on-chip macrocells peripherals via the serial data bus and indirectly for interrupt purposes, through the control registers.

Figure 4 : ST60XX Core Block Diagram.



INPUT/OUTPUT PORT

The ST601X has one I/O port (A), each I/O line can be individually programmed either in the input mode or the output mode. ST6010 has 6 I/O lines, while 7 are available on ST6011 and ST6012 and 8 on ST6013 and ST6014. The input mode allows configuring the lines in the high impedance state. The lines are organized in one port (port A). The port occupies two registers in the data space, there being one register, the DATA register (DR, location 00H), used to read the logic level values of the lines programmed in the input mode or to write the logic value of the signal to be output on the lines configured in the output mode, and another, the DATA DIRECTION register (DDR, location 04H), that allows the selection of the direction of each pin (input or output). In input mode the data register remains unchanged as the logic value at port pins is read directly into the shift register of the port macrocell.

TIMER

The Timer peripheral consists of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes. The content of the 8-bit counter can be read/written in the Timer/Counter register TCR that can be addressed in the data space as RAM location at the 13H address. The state of the 7-bit prescaler can be read in the PSC register at the 12H address. The control logic device can be managed thanks to the TSCR register (14H address). On ST6011, ST6012, ST6013 and ST6014 the external Timer pin is available for the user.

DIGITAL WATCHDOG/TIMER

The digital watchdog/timer of the ST601X devices consists of a down counter that can be used to provide a controlled recovery from a software upset. On ST6010, ST6012, ST6013 and ST6014 it is automatically initialized after reset so that this function does not need to be activated by the user program. As the watchdog function is always activated this down counter can't be used as a timer. On the ST6011 the watchdog activation can be controlled by the user software so that the watchdog can be used as a simple 7-bit timer for general purpose counting.
The watchdog is using one data space register (DWDR location 18H) and the watchdog time can be programmed using the 6MSbits in the watchdog register.The check time can be set differently for different routines within the general program.

8-BIT A/D CONVERTER

The ST601X A/D converter is an 8-bit analog to digital converter with 3 (ST6011, ST6014), 7 (ST6010), 9 (ST6012, ST6013) analog inputs offering 8-bit resolution with $\pm$ 1/2 bit of linearity and a conversion time of 150uS (clock frequency of 4MHz). The A/D converter also offers separate analog reference voltage pins. The ST601X A/D peripheral converts by a process of successive approximations using a clock frequency from 100 to 500kHz. The clock is derived from the oscillator with a division factor of twelve.

DEVELOPMENT SUPPORT & EMULATION SYSTEM

The ST60XX development system offers powerful in-circuit emulator and easy-to-use sets (dedicated boards) of modular hardware and software tools to shorten the total system development time of the final application. The ST60XX emulator offers emulation power with plug-in flexibility in the selection of emulation hardware modules for the dedicated macrocells. The emulator can be interfaced with a standard RS232 serial link to industry standard MS-DOS

personal computers. The ST60P1X piggyback version is also available to provide flexibility in prototypes or pre-production.

ABSOLUTE MAXIMUM RATINGS

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages. For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller than V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
I_O	Current Drain per Pin Excluding V_{DD} & V_{SS}	± 10	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50	mA
PD	Total Power Dissipation	18	mW
ESD	ESD Susceptibility	2000(1)	V
T_{stg}	Storage Temperature	– 65 to 150	°C

Notes : 1. MIL 883B Mode, 100pF through 1.5KΩ.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_A	Operating Temperature	6 Version 7 Version	– 40 – 40		85 110	°C °C
V_{DD}	Operating Supply Voltage		3		6	V
f_{OSC}	Oscillator Frequency	V_{DD} = 4.5 – 6.0V	0		4	MHz
f_{OSC}	Oscillator Frequency	V_{DD} = 3.5V	0		1	MHz
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V	0		0.5	MHz
AV_{DD} AV_{SS}	Analog Supply Voltage		V_{SS}		V_{DD}	V

2. Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress

THERMAL CHARACTERISTICS

$R_{th(J-A)}$	Thermal Resistance Plastic DIP 20	Max.	130	°C/W
	Plastic DIP 28		80	
	Plastic SO 20		160	
	Plastic SO 28			

rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note : On ST6010 AV_{DD} and AV_{SS} are internally connected to digital V_{SS} and V_{DD}

POWER CONSIDERATIONS

The average chip-junction temperature, Tj, in Celsius can be obtain from :

$$Tj = TA + PD \times RthJA$$

where : TA = Ambient Temperature, RthJA = Package thermal resistance (junction-to ambient, PD = Pint + Pport,

Pint = $I_{DD} \times V_{DD}$ (chip internal power),

Pport = Port power dissipation (determined by the user).

For most applications, Pport < Pint and the former can be neglected. Pport may become significant if the device is configured to drive darlington bases or sink LED loads. An approximate relationship between PD and TJ (if Pport is neglected) is :

$$PD = K (TJ + 273).$$

Solving previous equations gives:

$$K = PD \times (TA + 273) + RthJA \times PD^2$$

DC ELECTRICAL CHARACTERISTICS

$T_A = -40$ to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_P	Positive Threshold	All I/O Lines V_{DD} = 3.0V	1.8	2.0	2.2	V
		V_{DD} = 4.5V	2.8	3.2	3.8	
		V_{DD} = 5.5V	3.6	4.0	4.4	
V_N	Negative Threshold	All I/O Lines V_{DD} = 3.0V	1.1	1.3	1.5	V
		V_{DD} = 4.5V	1.6	2.0	2.4	
		V_{DD} = 5.5V	2.0	2.4	2.8	
V_H	Hysteresis Voltage	All I/O Lines V_{DD} = 3.0V	0.6	0.8	0.9	V
		V_{DD} = 4.5V	0.9	1.2	1.4	
		V_{DD} = 5.5V	1.1	1.6	1.8	
V_{IL}	Input Low Level Voltage	RESET PIN V_{DD} = 3.0V			0.90	V
		V_{DD} = 4.5V			1.35	
		V_{DD} = 5.5V			1.65	
V_{IL}	Input Low Level Voltage	INT PIN V_{DD} = 3.0V			0.90	V
		V_{DD} = 4.5V			1.35	
		V_{DD} = 5.5V			1.65	
V_{IH}	Input High Level Voltage	RESET PIN V_{DD} = 3.0V	2.10			V
		V_{DD} = 4.5V	3.15			
		V_{DD} = 5.5V	3.85			
V_{IH}	Input High Level Voltage	INT PIN V_{DD} = 3.0V	2.10			V
		V_{DD} = 4.5V	3.15			
		V_{DD} = 5.5V	3.85			
V_{OL}	Low Level Output Voltage	All I/O Lines I_O < 1µA				V
		V_{DD} = 3.0V			0.1	
		V_{DD} = 5.5V			0.1	
V_{OL}	Low Level Output Voltage	All I/O Lines I_{OI} < 5mA				V
		V_{DD} = 4.5V			0.8	
		V_{DD} = 5.5V			0.8	
V_{OH}	High Level Output Voltage	All I/O Lines I_O < 1µA				V
		V_{DD} = 3.0V	2.9			
		V_{DD} = 5.5V	5.4			
V_{OH}	High Level Output Voltage	All I/O Lines I_{OH} = –5mA				V
		V_{DD} = 4.5V	3.0			
		V_{DD} = 5.5V	4.0			

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{IL}, I_{IH}	Input Leakage Current	All Digital Inputs Vin = V_{DD} or V_{SS} V_{DD} = 3.0V V_{DD} = 5.5V		 0.1 0.1	 1.0 1.0	µA
I_{IL}, I_{IH}	Input Leakage Current	All A/D Conv. Inputs Vin = V_{DD} or V_{SS} V_{DD} = 3.0V V_{DD} = 5.5V		 0.1 0.1	 1.0 1.0	µA
V_{ON}	Trigger Level ON Voltage	RESET V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V			1.0 1.5 1.7	V
V_{OFF}	Trigger Level OFF Voltage	RESET V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	2.0 3.0 3.8			V
I_{DD}	Supply Current RUN Mode	ILoad = 0mA Fosc = 0.5MHz V_{DD} = 3.0V Fosc = 4.0MHz V_{DD} = 5.5V			 2.0 3.0	 mA mA
I_{DD}	Supply Current WAIT Mode	ILoad = 0mA Fosc = 0.5MHz V_{DD} = 3.0V Fosc = 4.0MHz V_{DD} = 5.5V			 1.0 1.5	 mA mA
I_{DD}	Supply Current STOP Mode	Note 1 ILoad = 0mA V_{DD} = 3.0V V_{DD} = 5.5V			 3 10	 µA µA

AC ELECTRICAL CHARACTERISTICS

T_A = – 40 to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{OSC}	Oscillator Frequency	Crystal or External Clock V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	 DC DC DC		 0.5 4 4	MHz
t_{SU}	Oscillator Start-up Time	V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V			15 10 10	mS
t_{HI}	Level Interr. Hold Time	V_{DD} = 3.0V V_{DD} = 4.5V	5*tcyc			µs
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Output Pins			15	pF

A/D CONVERTER CHARACTERISTICS

T_A = – 40 to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Res	Resolution		8	8	8	Bit
Lin	Non Linearity	Max Deviation from the Best Straight Line			± 1/2	LSB
Qe	Quantization Error	Uncertainly due to converter resolution.			± 1/2	LSB
ZO	Zero Offset	$V_{in} = AV_{SS}$			1	LSB
FSO	Full Scale Offset	$V_{in} = AV_{DD}$			1	LSB
t_C	Conversion Time	f_{OSC} = 4MHz(1)		150		µs
V_{AN}	Conversion Range		AV_{SS}		AV_{DD}	V
ZIR	Zero Input Reading	Conversion result when $V_{in} = AV_{SS}$.	00			Hex
FSR	Full Scale Reading	Conversion result when $V_{in} = AV_{DD}$.			FF	Hex
AV_{SS} AV_{DD}	Analog Reference	(2)	V_{SS}		V_{DD}	V
AC_{IN}	Analog Input Capacitance				5	pF
ASI	Analog Source Impedance				30	KΩ
SSI	Analog Refer. Supply Imped.				2	KΩ

where K is constant pertaining to the particular part. K can be determined from the equation by measuring

TIMER CHARACTERISTICS

TA = – 40 to 85°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
tRes	Timer Resolution		$\frac{1}{fo} \cdot 12$			s
f_{IN}	Input Frequency on TIMER Pin	V_{DD} = 3.0V V_{DD} = 4.5V		1/4 f_{OSC}		MHz

ORDERING INFORMATION

The following chapter deals with the procedure for transfer the Program/Data ROM codes to SGS-THOMSON.

Communication of the ROM content. To communicate the contents of Program/Data ROM memories to SGS-THOMSON, the customer has to send one 2764 EPROM that must be programmed as follows:

0000H-087FH	Reserved (Should be filled with FFH)
0880H-0F9FH	User program
0FA0H-0FFBH	Reserved (Should be filled with FFH)
0FFCH	Interrupt vector LOW byte
0FFDH	Interrupt vector HIGH byte
0FFEH	Reset vector LOW byte
0FFFH	Reset vector HIGH byte

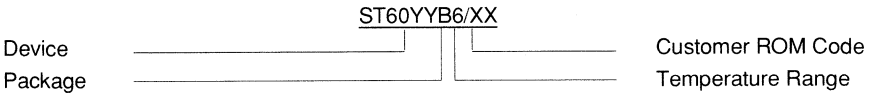
the Data ROM space (32 Bytes) of the microcontroller must be placed in the EPROM from:

1160H-117FH

All unused bytes must be filled with FFH. For shipment to SGS-THOMSON the EPROM should be placed in a conductive IC carrier and packaged carefully.

Listing Generation & Verification. When SGS-THOMSON receives the EPROM a computer listing is generated from the EPROM. This listing correspond exactly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. SGS-THOMSON will also program one 2764 EPROM from the data file corresponding to the listing to help the customer in its verification. The signed listing constitutes a part of the contractual agreement for the creation of the customer mask. SGS-THOMSON sales organization will provide detailed information on contractual points.

ST601X Part Number



Device : ST6010, ST6011, ST6012, ST6013, ST6014

Package: B:Pin Plastic Dual-in-Line, M:Plastic SO

Temperature range : – 40°C to 85°C 6

Temperature range : – 40°C to 110°C 7

Marking : it is by default equivalent to the sales type (part number). If a special marking is required see attached option list chart.

Temperature range : – 40°C to 85°C 6

Temperature range : – 40°C to 110°C 7

Marking : it is by default equivalent to the sales type (part number). If a special marking is required see attached option list chart.

ST601X MICROCONTROLLER OPTION LIST

Customer .....
Address .....
Contact .....
Phone No .....
Reference .....

Device [ ] (d)
Package [ ] (p)
Temperature Range [ ] (t)

For marking one line with 11 characters maximum is possible

Special Marking [ ] (y/n) Line 1 "....." (M)

[d] 1 = ST6010, 2 = ST6011, 3 = ST6012, 4 = ST6013, 5=ST6014

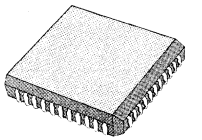
[p] B = Plastic Dual in Line, M = Plastic SO

(t) 6 = – 40 to 85°C
7 = – 40 to 110°C

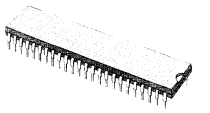
8 BIT HCMOS MCUs WITH A/D CONVERTER & LCD DRIVER

PRELIMINARY DATA

- 8-BIT ARCHITECTURE
- STATIC HCMOS OPERATION
- 3.0 TO 6.0 V SUPPLY OPERATING RANGE
- 3.25US TCYCLE (with 4 MHz clock)
- RUN, WAIT & STOP MODES
- USER ROM : 3876 BYTES
- RESERVED ROM : 220 BYTES
- DATA ROM : 64 BYTES
- DATA RAM : 64 BYTES
- 44-PIN PLASTIC PLCC PACKAGE (ST6040)
- 48-PIN PLASTIC DUAL IN LINE PACKAGE (ST6041)
- 15 PUSH-PULL BIDIRECTIONAL INPUTS/OUTPUTS WITH 5mA DRIVING CAPABILITY (ST6040)
- 16 PUSH-PULL BIDIRECTIONAL INPUTS/OUTPUTS WITH 5mA DRIVING CAPABILITY (ST6041)
- TWO 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER (Timer)
- DIGITAL SOFTWARE ACTIVATED WATCHDOG/TIMER (DSWD)
- 8-BIT A/D CONVERTER WITH 3 ANALOG INPUTS
- 18 LINES LCD DRIVER WITH 2:1 MULTIPLEXING (36 segments driving, ST6040)
- 20 LINES LCD DRIVER WITH 2:1 MULTIPLEXING (40 segments driving, ST6041)
- ONE EXTERNAL RISING EDGE SENSITIVE INTERRUPT INPUT (ST6040)
- ONE EXTERNAL FALLING EDGE SENSITIVE INTERRUPT INPUT (ST6041)
- ON-CHIP CLOCK OSCILLATOR
- POWER-ON RESET
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- WAIT, STOP AND BIT MANIPULATION INSTRUCTIONS
- TRUE LIFO 4 LEVEL STACK
- 9 POWERFUL ADDRESSING MODES
- THE ACCUMULATOR, THE X, Y, V & W REGISTERS, THE PORT AND PERIPHERALS DATA/CONTROL REGISTERS ARE ADDRESSED IN THE DATA SPACE AS RAM LOCATIONS
- THE DEVELOPMENT TOOL OF THE ST604X MICROCONTROLLERS CONSISTS OF THE EMS6-HW/B4X EMULATION AND DEVELOPMENT SYSTEM CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN MS-DOS PC
- ST60R4X IS THE ROMLESS VERSION



PLCC44



DIP-48

(Order Codes at the end of the datasheet)

Figure 1 : ST6040 Pin Configuration.

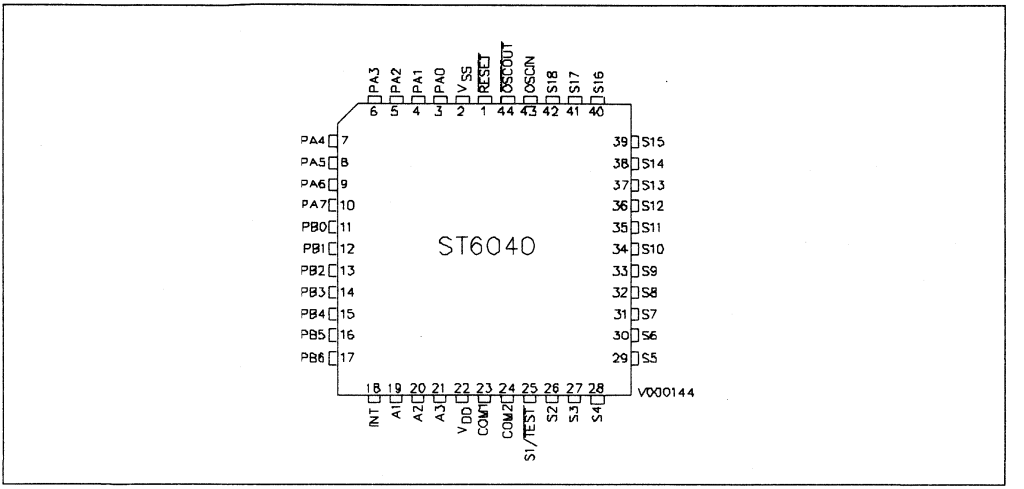
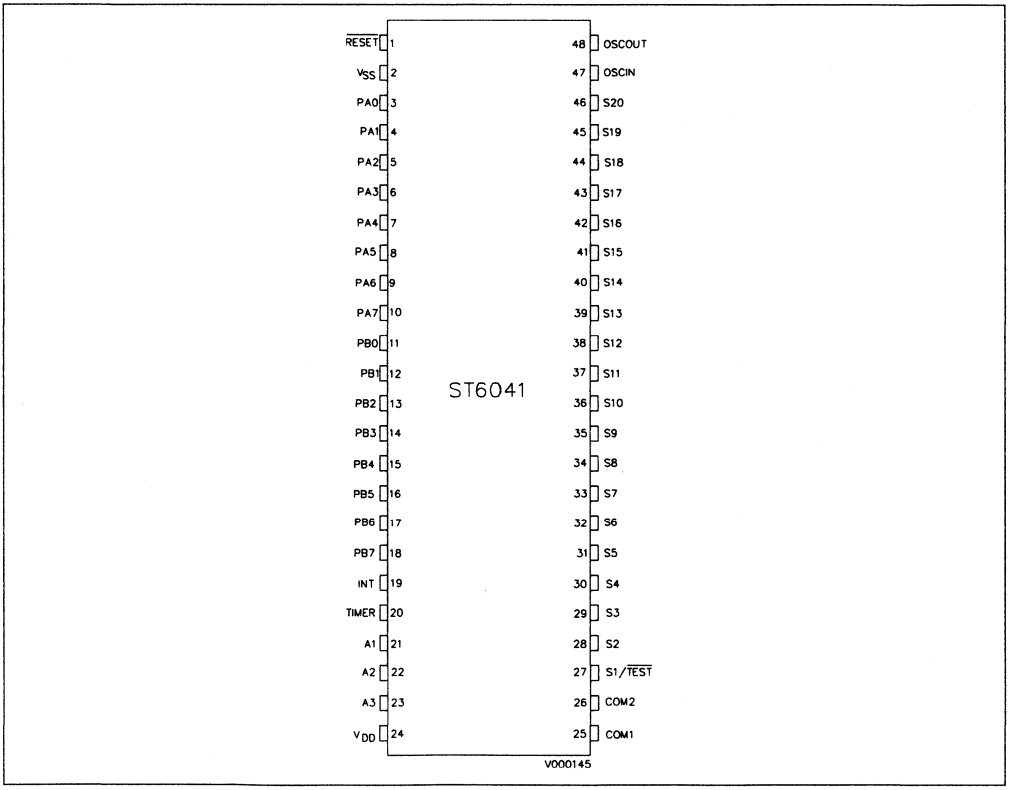


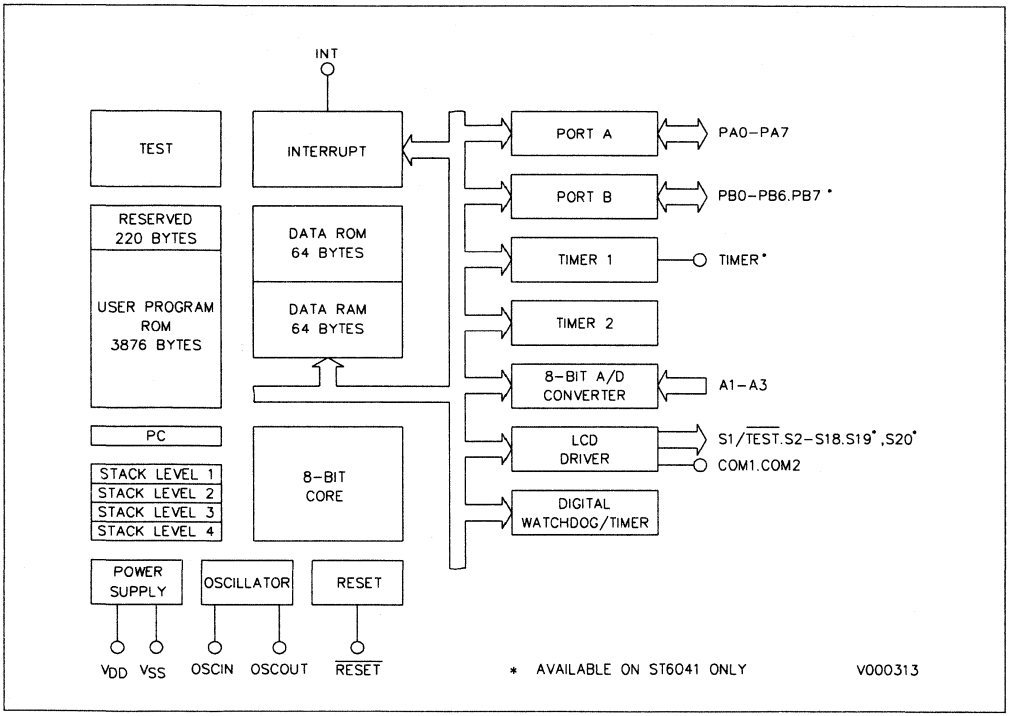
Figure 2 : ST6041 Pin Configuration.



GENERAL DESCRIPTION

The ST6040 and ST6041 microcontrollers are powerful members of the 8-bit HCMOS ST60XX family, a series of devices oriented to low-medium complexity applications. All ST60XX members are based on a building block approach : to a common core is associated a combination of on-chip peripherals (macrocells) available from a standard library to form around the core all the existing and future ST6 devices.These peripherals are designed with the same core technology giving full compatibility, short design and testing time. The macrocells of the ST6040/ST6041 are : two Timers each including an 8-bit counter with a 7-bit software programmable prescaler (Timer), the 8-bit A/D Converter with 3 analog inputs, the liquid crystal display driver (LCD) with 18x2 (ST6040) and 20x2 (ST6041) lines (36/40 segments), the software activated digital watchdog/timer (DSWD). Thanks to these peripherals the ST6040/ST6041 are well suited to consumer, automotive and industrial controls applications.

Figure 3 : ST6040 and ST6041 Block Diagram.



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN, OSCOUT. These pins are internally connected with the on-chip oscillator circuit. A crystal quartz or a ceramic resonator has to be connected between these two pins in order to allow a right operating of the MCU. The OSCIN pin is the input pin, the OSCOUT pin is the output pin.

$\overline{\text{RESET}}$. The active low RESET pin is used to restart the microcontroller at the beginning of its program.

INT. The INT pin provides the capability for asynchronous applying an external interrupt to the MCU.This pin is rising edge sensitive on ST6040 and falling edge sensitive on ST6041.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input or an output under software control of the data direction register. Port A has a push-pull output configuration with 5mA drive capability and schmitt trigger inputs.

PB0-PB6,PB7 (*). These 8 lines are organized as one I/O port (B). Each line may be configured as either an input or an output under software control of the data direction register. Port B has a push-pull output configuration with 5mA drive capability and schmitt trigger inputs. (*) PB7 is available only on ST6041.

TIMER (*). This is the Timer 1 I/O pin. In input mode it is connected to the prescaler and acts as external timer clock (DOUT=TOUT=0) or as control gate for the internal timer clock (DOUT=1,TOUT=0). In the output mode the timer pin outputs the data bit when a time out occurs. (*) This pin is available only on ST6041.

A1-A3. These pins are the analog inputs for the on-chip 8-bit A/D converter. The user can select by software which analog channel has to be converted.

COM1, COM2. These two pins are the LCD peripheral common outputs. They are the outputs of the on-chip backplane voltage generator which is used for multiplexing the 18/20 LCD lines allowing 36/40 segments driving.

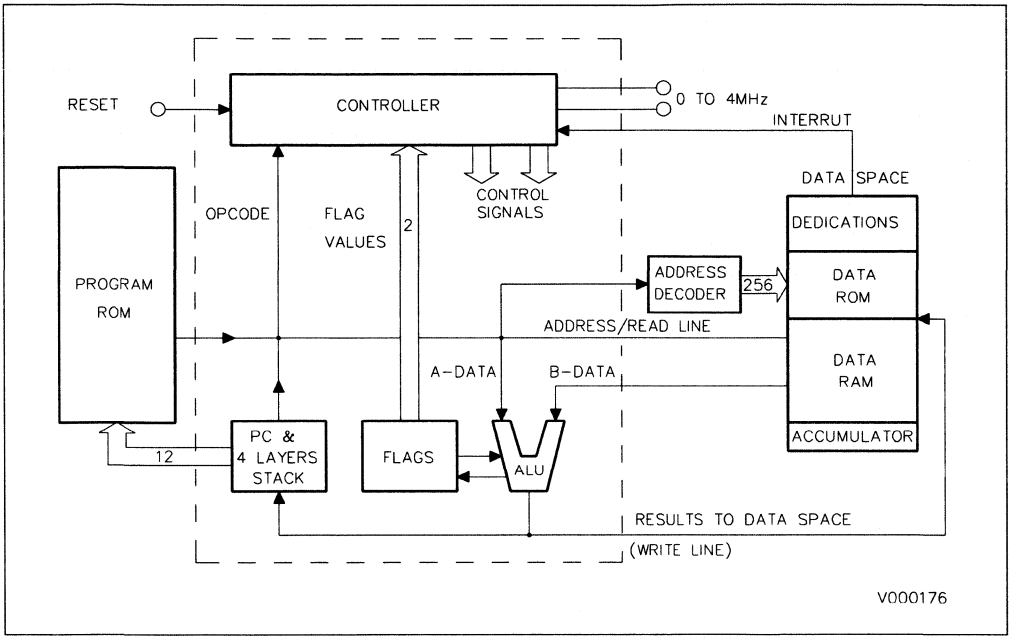
S1/**$\overline{\text{TEST}}$**. This pin is the LCD driver segment 1 output but also enables the factory test mode if tied low when Reset is active. The test mode is used to place the MCU into special operating mode.

S2-S18,S19(*),S20(*). These pins are the LCD driver segments outputs 2 to 20. (*) S19 and S20 are available only on ST6041.

ST60XX CORE

The Core of the ST60XX Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control buses. The in-core communications are arranged as shown in the following block diagram figure; the controller being externally linked to both the reset and the oscillator while the core is linked to the dedicated on-chip macrocells peripherals via the serial data bus and indirectly for interrupt purposes, through the control registers.

Figure 4 : ST60XX Core Block Diagram.



INPUT/OUTPUT PORT

The ST6040 and ST6041 microcontrollers have respectively 15 and 16 Input/Output lines that can be individually programmed either in the input mode or the output mode. The lines are organized in two ports (port A,B). The ports occupies four registers in the data space there being two registers, the DATA registers (DRA, DRB), used to read the logic level values of the lines programmed in the input mode or to write the logic value of the signal to be output on the lines configured in the output mode, and two DATA DIRECTION registers (DDRA, DDRB), that allow the selection of the direction of each pin (input or output). In input mode the data register remains unchanged as the logic value at port pins is read directly into the shift register of the port macrocell.

TIMERS

The ST6040 and ST6041 offer two on-chip Timer peripherals each consisting of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes. Timer 1 of ST6041 has the external TIMER pin available for the user. The content of the 8-bit counter can be read/written in the Timer/Counter register TCR that can be addressed in the data space as RAM location at the 13H (timer 1) and 16H (timer 2) addresses. The state of the 7-bit prescaler can be read in the PSC register at the 12H (timer 1) and 15H (timer 2) addresses. The control logic device can be managed thanks to the TSCR register (14H timer 1 and 17H timer2 addresses).

SOFTWARE ACTIVATED DIGITAL WATCHDOG/TIMER

The software activated digital watchdog/timer consists of a down counter that can be used to provide a controlled recovery from a software upset or as a simple 7-bit timer for general purpose counting. The watchdog/timer is using one data space register (DSWDR location 18H). The watchdog register is set to FEH after reset and the watchdog function is disabled. If the user is using the cell as a watchdog the watchdog time can be programmed using the 6 MSBits in the Watchdog/timer register; if the user selects the timer option there are 7 available counter bits. This is because when the cell is used as watchdog function bit 1 of the register is used for managing the watchdog. The check time can be set differently for different routines within the general program.

8-BIT A/D CONVERTER

The ST6040 and ST6041 A/D converter is an 8-bit analog to digital converter with 3 analog inputs offering 8-bit resolution with $\pm$ 1/2 bit of linearity and a conversion time of 150uS (clock frequency of 4MHz).

The ST6040 and ST6041 A/D peripheral converts by a process of successive approximations using a clock frequency from 100 to 500Khz. The clock is derived from the oscillator with a division factor of twelve.

LIQUID CRYSTAL DISPLAY DRIVER LCD

The Liquid Crystal Display Driver macrocell is based on an eight segment driver which can be multiplexed by the use of two backplanes. The ST6040 and ST6041 LCD allows two-lines multiplexed operation of 18 and 20 segments pair allowing direct driving of 36/40 segments.

DEVELOPMENT SUPPORT & EMULATION SYSTEM

The ST60XX development system offers powerful in-circuit emulator and easy-to-use sets (dedicated boards) of modular hardware and software tools to shorten the total system development time of the final application. The ST60XX emulator offers emulation power with plug-in flexibility in the selection of emulation hardware modules for the dedicated macrocells. The emulator can be interfaced with a standard RS232 serial link to industry standard MS-DOS personal computers. The ST60R4X romless version is also available to provide flexibility in prototypes or pre-production.

ABSOLUTE MAXIMUM RATINGS

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages. For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller than V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
I_O	Current Drain per Pin Excluding V_{DD} & V_{SS}	± 10	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50	mA
PD	Power Dissipation	30	mW
ESD	ESD Susceptibility	2000(1)	V
T_{stg}	Storage Temperature	– 65 to 150	°C

Notes : 1. MIL 883B Mode, 100pF through 1.5KΩ.
2. Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_A	Operating Temperature	6 Version 7 Version	– 40 – 40		85 110	°C °C
V_{DD}	Operating Supply Voltage		3		6	V
f_{OSC}	Oscillator Frequency	V_{DD} = 4.5 – 6.0V	0		4	MHz
f_{OSC}	Oscillator Frequency	V_{DD} = 3.5V	0		1	MHz
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V	0		0.5	MHz
AV_{DD} AV_{SS}	Analog Supply Voltage		V_{SS}		V_{DD}	V

Note : On ST6040/ST6041 AV_{DD} and AV_{SS} are internally connected to digital V_{SS} and V_{DD}.

THERMAL CHARACTERISTICS

$R_{th(J-A)}$	Thermal Resistance P-DIP PLCC	Max.	65 85	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, Tj, in Celsius can be obtained from :

$$Tj = TA + PD \times RthJA$$

where : TA = Ambient Temperature,

RthJA = Package thermal resistance (junction-to-ambient,

PD = Pint + Pport,

Pint = $I_{DD} \times V_{DD}$ (chip internal power),

Pport = Port power dissipation (determined by the user).

For most applications, Pport < Pint and the former can be neglected. Pport may become significant if the device is configured to drive darlington bases or sink LED loads. An approximate relationship between PD and TJ (if Pport is neglected) is :

$$PD = K (TJ + 273).$$

Solving previous equations gives:

$$K = PD \times (TA + 273) + RthJA \times PD^2$$

where K is constant pertaining to the particular part. K can be determined from the equation by measuring PD for a know TA. Using this value of K the values of PD and TJ can be obtained by solving first equations iteratively for any value of TA.

DC ELECTRICAL CHARACTERISTICS

$T_A = -40$ to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_P	Positive Threshold	All I/O Lines V_{DD} = 3.0V	1.8	2.0	2.2	V
		V_{DD} = 4.5V	2.8	3.2	3.8	
		V_{DD} = 5.5V	3.6	4.0	4.4	
V_N	Negative Threshold	All I/O Lines V_{DD} = 3.0V	1.1	1.3	1.5	V
		V_{DD} = 4.5V	1.6	2.0	2.4	
		V_{DD} = 5.5V	2.0	2.4	2.8	
V_H	Hysteresis Voltage	All I/O Lines V_{DD} = 3.0V	0.6	0.8	0.9	V
		V_{DD} = 4.5V	0.9	1.2	1.4	
		V_{DD} = 5.5V	1.1	1.6	1.8	
V_{IL}	Input Low Level Voltage	RESET PIN V_{DD} = 3.0V			0.90	V
		V_{DD} = 4.5V			1.35	
		V_{DD} = 5.5V			1.65	
V_{IL}	Input Low Level Voltage	INT PIN V_{DD} = 3.0V			0.90	V
		V_{DD} = 4.5V			1.35	
		V_{DD} = 5.5V			1.65	
V_{IH}	Input High Level Voltage	RESET PIN V_{DD} = 3.0V	2.10			V
		V_{DD} = 4.5V	3.15			
		V_{DD} = 5.5V	3.85			
V_{IH}	Input High Level Voltage	INT PIN V_{DD} = 3.0V	2.10			V
		V_{DD} = 4.5V	3.15			
		V_{DD} = 5.5V	3.85			
V_{OL}	Low Level Output Voltage	All I/O Lines $I_O < 1\mu A$				V
		V_{DD} = 3.0V			0.1	
		V_{DD} = 5.5V			0.1	
V_{OL}	Low Level Output Voltage	All I/O Lines $I_{OL} < 5mA$				V
		V_{DD} = 4.5V			0.8	
		V_{DD} = 5.5V			0.8	
V_{OH}	High Level Output Voltage	All I/O Lines $I_O < 1\mu A$				V
		V_{DD} = 3.0V	2.9			
		V_{DD} = 5.5V	5.4			
V_{OH}	High Level Output Voltage	All I/O Lines $I_{OH} = -5mA$				V
		V_{DD} = 4.5V	3.0			
		V_{DD} = 5.5V	4.0			

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{IL}, I_{IH}	Input Leakage Current	All Digital Inputs Vin = V_{DD} or V_{SS}				µA
		V_{DD} = 3.0V		0.1	1.0	
		V_{DD} = 5.5V		0.1	1.0	
I_{IL}, I_{IH}	Input Leakage Current	All A/D Conv. Inputs Vin = V_{DD} or V_{SS}				µA
		V_{DD} = 3.0V		0.1	1.0	
		V_{DD} = 5.5V		0.1	1.0	
V_{ON}	Trigger Level ON Voltage	RESET V_{DD} = 3.0V			1.0	V
		V_{DD} = 4.5V			1.5	
		V_{DD} = 5.5V			1.7	
V_{OFF}	Trigger Level ON Voltage	RESET V_{DD} = 3.0V	2.0			V
		V_{DD} = 4.5V	3.0			
		V_{DD} = 5.5V	3.8			
I_{DD}	Supply Current RUN Mode	ILoad = 0mA F_{osc} = 0.5MHz				
		V_{DD} = 3.0V			3.5	mA
		F_{osc} = 4MHz				
		V_{DD} = 5.5V			5.0	mA
I_{DD}	Supply Current WAIT Mode	ILoad = 0mA F_{osc} = 0.5MHz				
		V_{DD} = 3.0V			1.7	mA
		F_{osc} = 4MHz				
		V_{DD} = 5.5V			2.5	mA
I_{DD}	Supply Current STOP Mode	Note ILoad = 0mA				
		V_{DD} = 3.0V			20	µA
		V_{DD} = 5.5V			30	µA

AC ELECTRICAL CHARACTERISTICS

T_A = – 40 to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{OSC}	Oscillator Frequency	Crystal or External Clock				
		V_{DD} = 3.0V	DC		0.5	
		V_{DD} = 4.5V	DC		4	
		V_{DD} = 5.5V	DC		4	
t_{SU}	Oscillator Start-up Time	V_{DD} = 3.0V			15	mS
		V_{DD} = 4.5V			10	
		V_{DD} = 5.5V			10	
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Output Pins			15	pF

A/D ELECTRICAL CHARACTERISTICS

T_A = – 40 to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Res	Resolution		8	8	8	Bit
Lin	Non Linearity	Max Deviation from the Best Straight Line			± 1/2	LSB
Qe	Quantization Error	Uncertainly due to converter resolution.			± 1/2	LSB
ZO	Zero Offset Error	$V_I = AV_{SS}$			1	LSB
FSO	Full Scale Error	$V_I = AV_{DD}$			1	LSB
t_C	Conversion Time	f_{OSC} = 4MHz(1)		150		µs
V_{AN}	Conversion Range		AV_{SS}		AV_{DD}	V
ZIR	Zero Input Reading	Conversion result when $V_I = AV_{SS}$.	00			Hex
FSR	Full Scale Reading	Conversion result when $V_I = AV_{DD}$.			FF	Hex
AV_{SS} AV_{DD}	Analog Reference	(2)	V_{SS}		V_{DD}	V
AC_{IN}	Analog Input Capacitance				5	pF
ASI	Analog Source Impedance				30	KΩ
SSI	Analog Refer. Supply Imped.				2	KΩ

Notes : 1. With oscillator frequencies less than 1.2MHz, the A/D converter accuracy is decreased.
2. In ST6040/ST6041 Devices Analog V_{SS} and V_{DD} are internally connected to digital V_{SS} and V_{DD}.

TIMER CHARACTERISTICS

T_A = – 40 to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Res	Resolution		$\frac{1}{fo} \cdot 12$			s
f_{IN}	Input Frequency at TIMER Pin	V_{DD} = 3.0V V_{DD} = 4.5V		1/4 f_{OSC}		MHz

Note : Timer pin is available only on ST6041 timer 1.

LCD DRIVER CHARACTERISTICS

$T_A = -40$ to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
fBP	Backplane Frequency	Fosc = 4MHz V_{DD} = 4.5V	80	80	80	Hz
VOS	DC Offset Voltage	V_{DD} = 3.0V V_{DD} = 4.5V			50	Mv
V_{OL}	Low Level Output Voltage	V_{DD} = 4.5V		0.5		V
V_{OH}	High Level Output Voltage	V_{DD} = 4.5V		0.5		V

ORDERING INFORMATION

The following chapter deals with the procedure for transfer the Program/Data ROM codes to SGS-THOMSON.

Communication of the ROM codes. To communicate the contents of Program/Data ROM memories to SGS-THOMSON, the customer has to send two 2764 EPROM that must be programmed as follows:

0000H-007FH Reserved (Should be filled with FFH)
0080H-0F9FH User program
0FA0H-0FFBH Reserved (Should be filled with FFH)
0FFCH Interrupt vector LOW byte
0FFDH Interrupt vector HIGH byte
0FFEH Reset vector LOW byte
0FFFH Reset vector HIGH byte

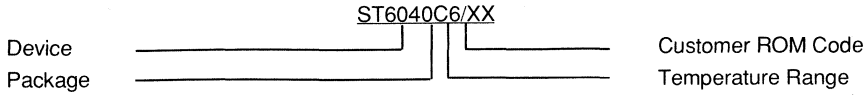
The Data ROM codes (64 Bytes) of the microcontroller must be placed in the EPROM from:

1140H-117FH

All unused bytes must be set to FFH. For shipment to SGS-THOMSON the EPROMs should be placed in a conductive IC carrier and packaged carefully.

Listing Generation & Verification. When SGS-THOMSON receives the EPROMs, they are compared and a computer listing is generated from them. This listing refers exactly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. SGS-THOMSON will also program one 2764 EPROM from the data file corresponding to the listing to help the customer in its verification. The signed listing constitutes a part of the contractual agreement for the creation of the customer mask. SGS-THOMSON sales organization will provide detailed information on contractual points.

ST6040 Part Number



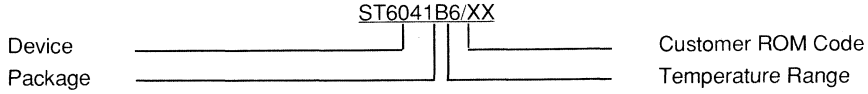
Device : ST6040

Package : C : 44 PLCC

Temperature range : – 40°C to 85°C 6
– 40°C to 110°C 7

Marking : it is by default equivalent to the sales type (part number). If a special marking is required see attached option list chart.

ST6041 Part Number



Device : ST6041

Package : B : 48 Plastic Dual-in-line

Temperature range : – 40°C to 85°C 6
– 40°C to 110°C 7

Marking : it is by default equivalent to the sales type (part number). If a special marking is required see attached option list.

ST604X MICROCONTROLLER OPTION LIST

Customer .....
Address .....
Contact .....
Phone No .....
Reference .....

Device [ ] (d)

Package [ ] (p)

Temperature Range [ ] (t)

For marking two lines with 10 characters maximum are possible

Special Marking [ ] (y/n) Line 1 "....." (M)
Line 2 "....." (M)

[d] 1 = ST6040, 2 = ST6041

[p] B=Plastic Dual in Line, C = PLCC

(t) 6 = – 40 to 85°C
7 = – 40 to 110°C

(M) Letters, digits, '.', '-', '/' and spaces only

Signature .....
Date .....

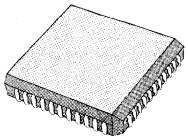
SGS-THOMSON MICROELECTRONICS

ST6050/51/52

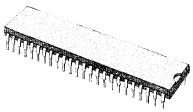
8 BIT HCMOS MICROCONTROLLERS

PRELIMINARY DATA

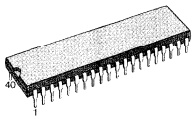
- 8-BIT ARCHITECTURE
- STATIC HCMOS OPERATION
- 3.0 TO 6.0V SUPPLY OPERATING RANGE
- 3.25US TCYCLE (with 4MHz clock)
- RUN, WAIT & STOP MODES
- USER ROM : 3876 BYTES
- RESERVED ROM : 220 BYTES
- DATA ROM : 64 BYTES
- DATA RAM : 64 BYTES
- 30 PUSH-PULL BIDIRECTIONAL INPUTS/OUTPUTS WITH 5mA DRIVING CAPABILITY (ST6050)
- 33 PUSH-PULL BIDIRECTIONAL INPUTS/OUTPUTS WITH 5mA DRIVING CAPABILITY (ST6051)
- 27 PUSH-PULL BIDIRECTIONAL INPUTS/OUTPUTS WITH 5mA DRIVING CAPABILITY (ST6052)
- TWO 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER (Timer)
- DIGITAL WATCHDOG/TIMER (HARDWARE OR SOFTWARE ACTIVATED)
- 8-BIT A/D CONVERTER WITH 3 (ST6050/52) & 4 (ST6051) ANALOG INPUTS
- ONE AC INPUT PREAMPLIFIER WITH FEEDBACK OUTPUT
- ONE EXTERNAL INTERRUPT INPUT (level or edge triggered)
- ON-CHIP CLOCK OSCILLATOR
- POWER-ON RESET
- 44 PIN PLCC PLASTIC PACKAGE (ST6050)
- 48 PIN DUAL-IN-LINE PLASTIC PACKAGE (ST6051)
- 40 PIN DUAL-IN-LINE PLASTIC PACKAGE (ST6052)
- SAME ST60XX INSTRUCTION SET
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- WAIT, STOP AND BIT MANIPULATION INSTRUCTIONS
- TRUE LIFO 4 LEVEL STACK
- 9 POWERFUL ADDRESSING MODES
- THE ACCUMULATOR, THE X, Y, V & W REGISTERS, THE PORT AND PERIPHERALS DATA/CONTROL REGISTERS ARE ADDRESSED IN THE DATA SPACE AS RAM LOCATIONS
- THE DEVELOPMENT TOOL OF THE ST605X MICRONTROLLERS FAMILY CONSISTS OF THE EMS6-HW/B5X1X EMULATION AND DEVELOPMENT PACKAGE CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN IBM PC
- ST60R5X IS THE ROMLESS VERSION



PLCC-44



DIP-48



DIP-40

(Order Codes at the end of the datasheet)

Figure 1 : ST6050 Pin Configuration.

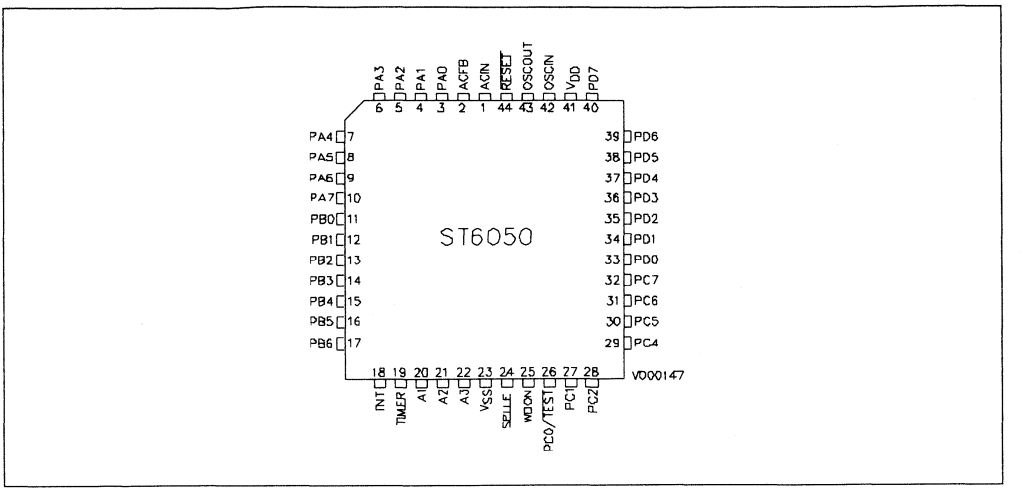


Figure 2 : ST6051 Pin Configuration.

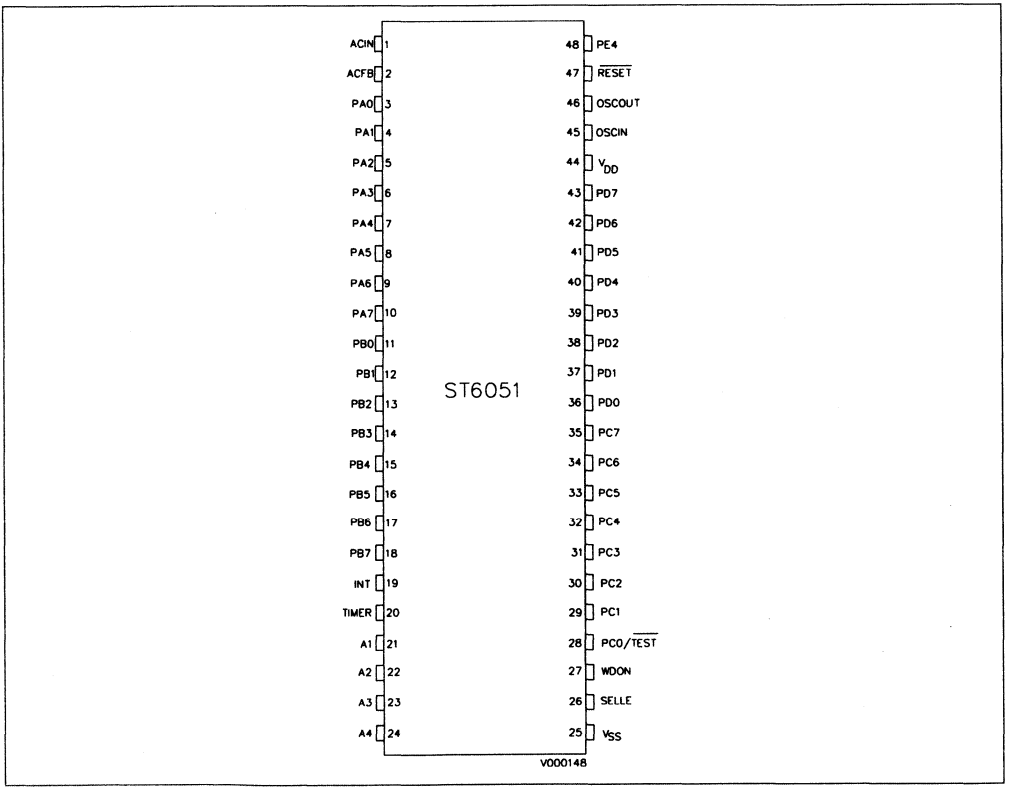
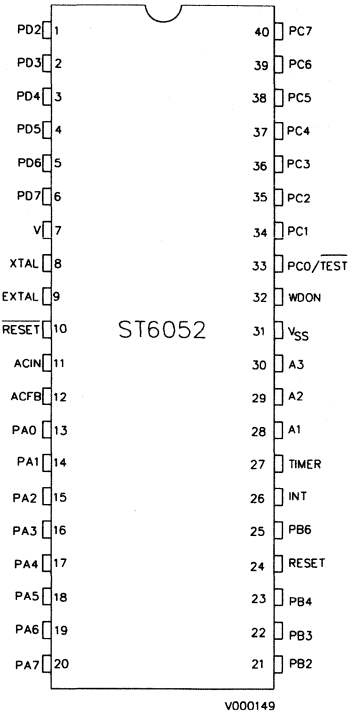


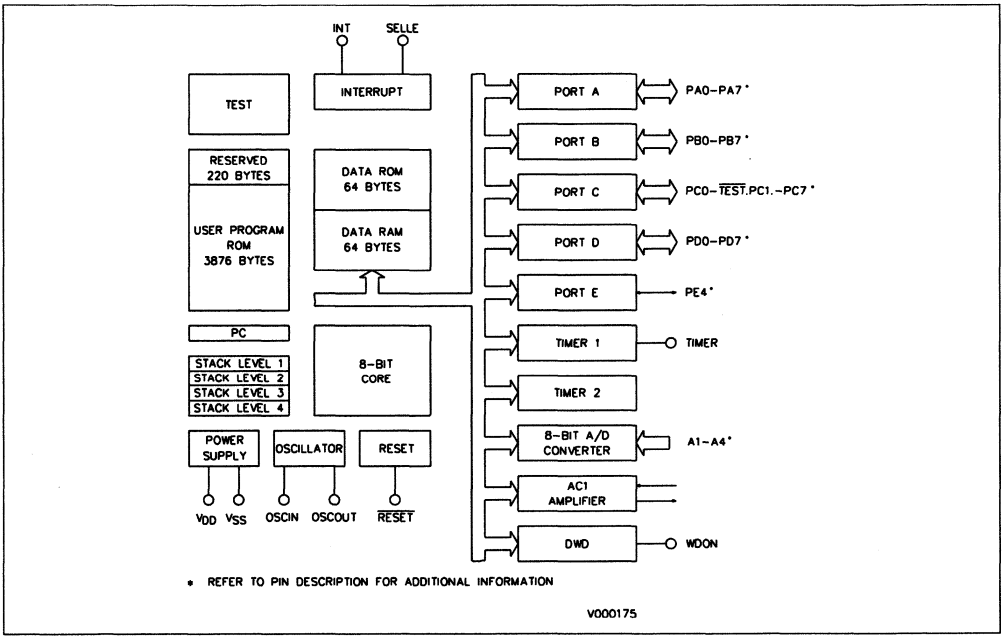
Figure 3 : ST6052 Pin Configuration.



GENERAL DESCRIPTION

The ST6050, ST6051 and ST6052 microcontrollers are powerful members of the 8-bit HCMOS ST60XX family, a series of devices oriented to low-medium complexity applications. All ST60XX members are based on a building block approach : to a common core is associated a combination of on-chip peripherals (macrocells) available from a standard library to form around the core all the existing and future ST6 devices. These peripherals are designed with the same core technology giving full compatibility, short design and testing time. The macrocells of the ST605X are : two Timers each including an 8-bit counter with a 7-bit software programmable prescaler (Timer), the digital watchdog/timer (DWD, hardware or software activated), the 8-bit A/D Converter with 3 (ST6050/52) or 4 (ST6052) analog inputs, one AC input operational amplifier with feedback output (AC1). Thanks to these peripherals the ST605X are well suited to consumer, automotive and industrial controls applications.

Figure 4 : ST605X Block Diagram.



PIN DESCRIPTION

VDD and VSS. Power is supplied to the MCU using these two pins. VDD is power and VSS is the ground connection.

OSCIN, OSCOUT. These pins are internally connected to the on-chip oscillator circuit. A crystal quartz or a ceramic resonator has to be connected between these two pins in order to allow a right operating of the MCU. A signal can be also provided to the OSCIN pin as external clock. The OSCIN pin is the input pin, the OSCOUT pin is the output pin.

$\overline{\text{RESET}}$. The active low RESET pin is used to restart the microcontroller to the beginning of its program. Refer to RESET description for additional information.

INT. The INT pin provides the capability for asynchronous applying an external interrupt to the MCU. This pin can be low level or rising edge sensitive, the sensitivity is programmed through the SELLE pin. (On ST6052 the interrupt sensitivity is fixed as rising edge).

SELLE. This pin selects between low level (SELLE=0) and rising edge (SELLE=1) interrupt pin sensitivity.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input or an output under software control of the data direction register. Port A has a push-pull output configuration with 5mA drive capability and schmitt trigger inputs.

PB0(*), PB1(*),PB2-PB7(*). These 8 lines are organized as one I/O port (B). Each line may be configured as either an input or an output under software control of the data direction register. Port B has a push-pull output configuration with 5mA drive capability and schmitt trigger inputs. (*) PB7 is not available on ST6050/52. PB0 and PB1 are not available on ST6052.

PC0/$\overline{\text{TEST}}$,PC1-PC2, PC3(*)-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured as either an input or an output under software control of the data direction register. Port C has a push-pull output configuration with 5mA drive capability and schmitt trigger inputs. PC0 also enables the factory test mode if tied low when Reset is active. The Test mode is used to place the MCU into a special operating mode.(*) PC3 is not available on ST6050

PD0(*), PD1(*), PD2-PD7. These 8 lines are organized as one I/O port (D). Each line may be configured as either an input or an output under software control of the data direction register. Port D has a push-pull output configuration with 5mA drive capability and schmitt trigger inputs. PD0 and PD1 are not available on ST6052.

PE4(*),PE5. These 2 lines are organized as one I/O port (E). This port has only two valid bits. PE4 is connected to a pin and can be used as any other I/O line. PE4 may be configured as either an input or an output under software control of the data direction register. PE4 has a push-pull output configuration with 5mA drive capability and schmitt trigger input. PE5 does not have the output buffer and is connected to the digital output of the sensing device AC1. This allows the user to read the AC comparator output digital signal by reading the data register of the I/O port, bit 5. The data direction register bit related to PE5 must be cleared to zero (input mode). PE5 is not connected to a pin. PE4 is not available on ST6050/52.

TIMER. This is the Timer 1 I/O pin. In input mode it is connected to the prescaler and acts as external timer clock (DOUT=TOUT=0) or as control gate for the internal timer clock (DOUT=1,TOUT=0). In the output mode the timer pin outputs the data bit when a time out occurs.

A1-A3, A4(*). These 4 pins are the analog inputs for the on-chip 8-bit A/D converter. The user can select by software which analog channel has to be converted. A4 is not available on ST6050/52.

WDON. This pin selects the watchdog enable option (HW or SW). A low level selects the hardware activation (watchdog always active), an high level selects the software activation (the watchdog can be enabled by software, deactivated by reset).

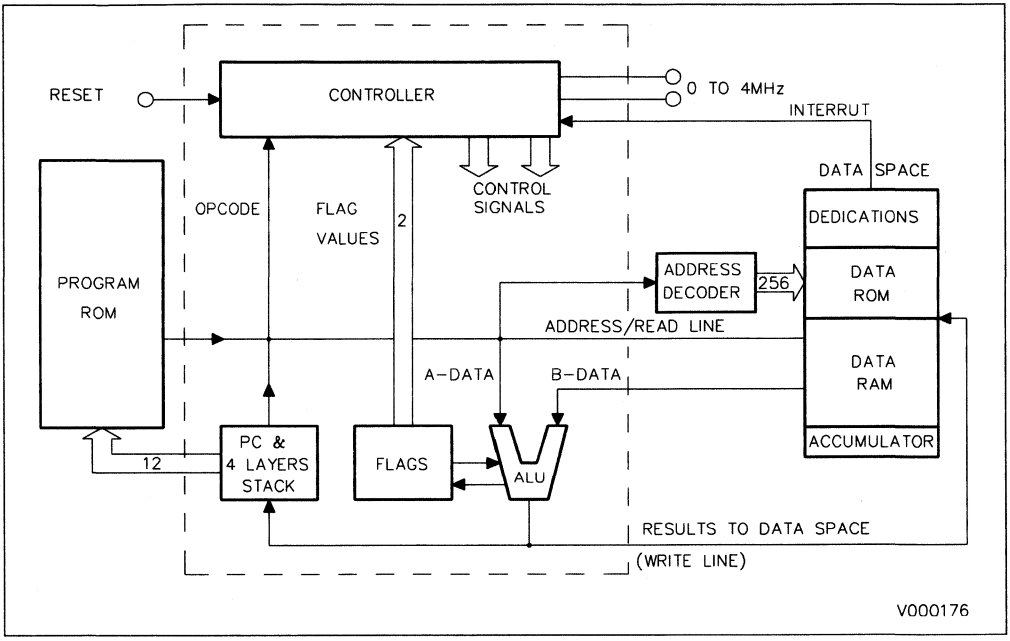
ACIN. This pin is the analog input signal of the operational preamplifier AC1.

ACFB. This pin is the output of the on-chip operational preamplifier; this output pin allows the user to fix the amplifier gain by external resistors.

ST60XX CORE

The Core of the ST60XX Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control buses. The in-core communications are arranged as shown in the following block diagram figure; the controller being externally linked to both the reset and the oscillator while the core is linked to the dedicated on-chip macrocells peripherals via the serial data bus and indirectly for interrupt purposes, through the control registers.

Figure 5 : ST60XX Core Block Diagram.



INPUT/OUTPUT PORT

The ST6050, ST6051 and ST6052 microcontrollers have respectively 30, 33 and 27 Input/Output lines that can be individually programmed either in the input mode or the output mode. The lines are organized in five ports (port A-E). The ports occupies ten registers in the data space there being five registers, the DATA registers (DRA-E), used to read the logic level values of the lines programmed in the input mode or to write the logic value of the signal to be output on the lines configured in the output mode, and five DATA DIRECTION registers (DDRA-E), that allow the selection of the direction of each pin (input or output). In input mode the data register remains unchanged as the logic value at port pins is read directly into the shift register of the port macrocell.

TIMERS

The ST605X offer two on-chip Timer peripherals each consisting of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes. Timer 1 has the external TIMER pin available for the user. The content of the 8-bit counter can be read/written in the Timer/Counter register TCR that can be addressed in the data space as RAM location at the 13H (timer 1) and 16H (timer 2) addresses. The state of the 7-bit prescaler can be read in the PSC register at the 12H (timer 1) and 15H (timer 2) addresses. The control logic device can be managed thanks to the TSCR register (14H timer 1 and 17H timer2 addresses).

DIGITAL WATCHDOG/TIMER

The ST605X watchdog/timer offers both of the watchdog options software activated watchdog/timer and the hardware activated watchdog function. The user can select one of the two options simply by applying an appropriate logic level to the WDON pin. A low level will select the hardware option which means the watchdog is always enabled, while a high logic level will select the software option so that the watchdog is software activated. The hardware activated digital watchdog function consists of a down counter that is automatically initialized after reset so that this function does not need to be activated by the user program. As the watchdog function is always activated this down counter can't be used as a timer. The software activated digital watchdog/timer consists of a down counter that can be used to provide a controlled recovery from a software upset or as a simple 7-bit timer for general purpose counting. The watchdog/timer is using one data space register (DWR location 18H).

8-BIT A/D CONVERTER

The ST605X A/D converter is an 8-bit analog to digital converter with 3/4 analog inputs offering 8-bit resolution with $\pm$ 1/2 bit of linearity and a conversion time of 150µS (clock frequency of 4MHz).

The ST605X A/D peripheral converts by a process of successive approximations using a clock frequency from 100 to 500kHz. The clock is derived from the oscillator with a division factor of twelve.

AC INPUT PIN WITH OPERATIONAL PREAMPLIFIER

The ST605X AC1 input is a sensing device for analog voltage signals that can be processed by the core. This macrocell consists of an operational amplifier and a schmitt trigger to generate logic pulses. The AC1 can be switched off by using the STOP instruction. The operation point of the operational amplifier is internally set to $1/2V_{DD}$. The amplified signal is compared with an internal reference of $0.29V_{DD}$ with an hysteresis of $\pm 0.02V_{DD}$. If the amplified input signal is greater than the internal reference, the digital output is low and vice-versa. The output of the amplifier is connected to a pin (ACFB); through this pin the user can fix the gain of the amplifier by external resistors and can also set the threshold level at which the comparator switches.

DEVELOPMENT SUPPORT & EMULATION SYSTEM

The ST60XX development system offers powerful in-circuit emulator and easy-to-use sets (dedicated boards) of modular hardware and software tools to shorten the total system development time of the final application. The ST60XX emulator offers emulation power with plug-in flexibility in the selection of emulation hardware modules for the dedicated macrocells. The emulator can be interfaced with a standard RS232 serial link to industry standard MS-DOS personal computers. The ST60R5X romless version is also available to provide flexibility in prototypes or pre-production.

ABSOLUTE MAXIMUM RATINGS

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages. For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller than V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
I_O	Current Drain per Pin Excluding V_{DD} & V_{SS}	± 10	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50	mA
PD	Power Dissipation	30	mW
ESD	ESD Susceptibility	2000(1)	V
T_{stg}	Storage Temperature	– 65 to 150	°C

Notes : 1. MIL 883B Mode, 100pF through 1.5KΩ.
2. Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_A	Operating Temperature	6 Version 7 Version	– 40 – 40		85 110	°C °C
V_{DD}	Operating Supply Voltage		3		6	V
f_{OSC}	Oscillator Frequency	V_{DD} = 4.5 – 6.0V	0		4	MHz
f_{OSC}	Oscillator Frequency	V_{DD} = 3.5V	0		1	MHz
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V	0		0.5	MHz
AV_{DD} AV_{SS}	Analog Supply Voltage		V_{SS}		V_{DD}	V

Note : On ST605X AV_{DD} and AV_{SS} are internally connected to digital V_{SS} and V_{DD}.

THERMAL CHARACTERISTICS

$R_{th(J-A)}$	Thermal Resistance P-DIP 40	Max.	68	°C/W
	P-DIP 48		65	
	PLCC		85	

POWER CONSIDERATIONS

The average chip-junction temperature, Tj, in Celsius can be obtained from :

$$Tj = TA + PD \times RthJA$$

Where :TA = Ambient Temperature,

RthJA = Package thermal resistance (junction-to-ambient,

PD = Pint + Pport,

Pint = $I_{DD} \times V_{DD}$ (chip internal power),

Pport = Port power dissipation (determined by the user).

For most applications, Pport << Pint and the former can be neglected. Pport may become significant if the device is configured to drive darlington bases or sink LED loads. An approximate relationship between PD and TJ (if Pport is neglected) is :

$$PD = K (TJ + 273).$$

Solving previous equations gives:

$$K = PD \times (TA + 273) + RthJA \times PD^2$$

where K is constant pertaining to the particular part. K can be determined from the equation by measuring PD for a know TA. Using this value of K the values of PD and TJ can be obtained by solving first equations iteratively for any value of TA.

DC ELECTRICAL CHARACTERISTICS

$T_A = -40$ to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_P	Positive Threshold	All I/O Lines V_{DD} = 3.0V	1.8	2.0	2.2	V
		V_{DD} = 4.5V	2.8	3.2	3.8	
		V_{DD} = 5.5V	3.6	4.0	4.4	
V_N	Negative Threshold	All I/O Lines V_{DD} = 3.0V	1.1	1.3	1.5	V
		V_{DD} = 4.5V	1.6	2.0	2.4	
		V_{DD} = 5.5V	2.0	2.4	2.8	
V_H	Hysteresis Voltage	All I/O Lines V_{DD} = 3.0V	0.6	0.8	0.9	V
		V_{DD} = 4.5V	0.9	1.2	1.4	
		V_{DD} = 5.5V	1.1	1.6	1.8	
V_{IL}	Input Low Level Voltage	RESET PIN V_{DD} = 3.0V			0.90	V
		V_{DD} = 4.5V			1.35	
		V_{DD} = 5.5V			1.65	
V_{IL}	Input Low Level Voltage	INT PIN V_{DD} = 3.0V			0.90	V
		V_{DD} = 4.5V			1.35	
		V_{DD} = 5.5V			1.65	
V_{IH}	Input High Level Voltage	RESET PIN V_{DD} = 3.0V	2.10			V
		V_{DD} = 4.5V	3.15			
		V_{DD} = 5.5V	3.85			
V_{IH}	Input High Level Voltage	INT PIN V_{DD} = 3.0V	2.10			V
		V_{DD} = 4.5V	3.15			
		V_{DD} = 5.5V	3.85			
V_{OL}	Low Level Output Voltage	All I/O Lines $I_O < 1\mu A$				V
		V_{DD} = 3.0V			0.1	
		V_{DD} = 5.5V			0.1	
V_{OL}	Low Level Output Voltage	All I/O Lines $I_{OL} < 5mA$				V
		V_{DD} = 4.5V			0.8	
		V_{DD} = 5.5V			0.8	
V_{OH}	High Level Output Voltage	All I/O Lines $I_O < 1\mu A$				V
		V_{DD} = 3.0V	2.9			
		V_{DD} = 5.5V	5.4			
V_{OH}	High Level Output Voltage	All I/O Lines $I_{OH} = -5mA$				V
		V_{DD} = 4.5V	3.0			
		V_{DD} = 5.5V	4.0			

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{IL}, I_{IH}	Input Leakage Current	All Digital Inputs Vin = V_{DD} or V_{SS} V_{DD} = 3.0V V_{DD} = 5.5V		 0.1 0.1	 1.0 1.0	µA
I_{IL}, I_{IH}	Input Leakage Current	All A/D Conv. Inputs Vin = V_{DD} or V_{SS} V_{DD} = 3.0V V_{DD} = 5.5V		 0.1 0.1	 1.0 1.0	µA
V_{ON}	Trigger Level ON Voltage	RESET V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V			1.0 1.5 1.7	V
V_{OFF}	Trigger Level ON Voltage	RESET V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	2.0 3.0 3.8			V
I_{DD}	Supply Current RUN Mode	ILoad = 0mA F_{osc} = 0.5MHz V_{DD} = 3.0V F_{osc} = 4MHz V_{DD} = 5.5V			 3.5 5.0	 mA mA
I_{DD}	Supply Current WAIT Mode	ILoad = 0mA F_{osc} = 0.5MHz V_{DD} = 3.0V F_{osc} = 4MHz V_{DD} = 5.5V			 1.7 2.5	 mA mA
I_{DD}	Supply Current STOP Mode	Note ILoad = 0mA V_{DD} = 3.0V V_{DD} = 5.5V			 20 30	 µA µA

Note : STOP mode is available only when watchdog/timer is not enabled.

AC ELECTRICAL CHARACTERISTICS

T_A = – 40 to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{OSC}	Oscillator Frequency	Crystal or External Clock V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	 DC DC DC		 0.5 4 4	
t_{SU}	Oscillator Start-up Time	V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V			15 10 10	mS
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Output Pins			15	pF

A/D ELECTRICAL CHARACTERISTICS

$T_A = -40$ to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Res	Resolution		8	8	8	Bit
Lin	Non Linearity	Max Deviation from the Best Straight Line			± 1/2	LSB
Qe	Quantization Error	Uncertainly due to converter resolution.			± 1/2	LSB
ZO	Zero Offset Error	$V_I = AV_{SS}$			1	LSB
FSO	Full Scale Error	$V_I = AV_{DD}$			1	LSB
t_C	Conversion Time	f_{OSC} = 4MHz(1)		150		µs
V_{AN}	Conversion Range		AV_{SS}		AV_{DD}	V
ZIR	Zero Input Reading	Conversion result when $V_I = AV_{SS}$.	00			Hex
FSR	Full Scale Reading	Conversion result when $V_I = AV_{DD}$.			FF	Hex
AV_{SS} AV_{DD}	Analog Reference	(2)	V_{SS}		V_{DD}	V
AC_{IN}	Analog Input Capacitance				5	pF
ASI	Analog Source Impedance				30	KΩ
SSI	Analog Refer. Supply Imped.				2	KΩ

Notes : 1. With oscillator frequencies less than 1.2MHz, the A/D converter accuracy is decreased.
2. In ST605X Devices Analog V_{SS} and V_{DD} are internally connected to digital V_{SS} and V_{DD}.

TIMER CHARACTERISTICS

$T_A = -40$ to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Res	Resolution		$\frac{1}{fo} \cdot 12$			s
f_{IN}	Input Frequency at TIMER Pin	V_{DD} = 3.0V V_{DD} = 4.5V		1/4 f_{OSC}		MHz

Note : Timer pin is available only on timer 1.

LCD DRIVER CHARACTERISTICS

$T_A = -40$ to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
fBP	Backplane Frequency	Fosc = 4MHz V_{DD} = 4.5V	80	80	80	Hz
VOS	DC Offset Voltage	V_{DD} = 3.0V V_{DD} = 4.5V			50	Mv
V_{OL}	Low Level Output Voltage	V_{DD} = 4.5V		0.5		V
V_{OH}	High Level Output Voltage	V_{DD} = 4.5V		0.5		V

ORDERING INFORMATION

The following chapter deals with the procedure for transfer the Program/Data ROM codes to SGS-THOMSON.

Communication of the ROM codes. To communicate the contents of Program/Data ROM memories to SGS-THOMSON, the customer has to send two 2764 EPROM that must be programmed as follows :

0000H-007FH	Reserved (Should be filled with FFH)
0080H-0F9FH	User program
0FA0H-0FFBH	Reserved (Should be filled with FFH)
0FFCH	Interrupt vector LOW byte
0FFDH	Interrupt vector HIGH byte
0FFEH	Reset vector LOW byte
0FFFH	Reset vector HIGH byte

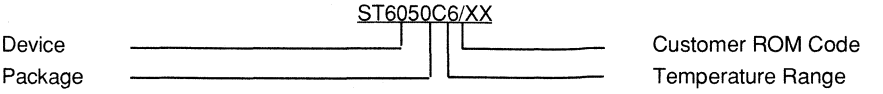
The Data ROM codes (64 Bytes) of the microcontroller must be placed in the EPROM from :

1140H-117FH

All unused bytes must be set to FFH. For shipment to SGS-THOMSON the EPROMs should be placed in a conductive IC carrier and packaged carefully.

Listing Generation & Verification. When SGS-THOMSON receives the EPROMs, they are compared and a computer listing is generated from them. This listing refers exactly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. SGS-THOMSON will also program one 2764 EPROM from the data file corresponding to the listing to help the customer in its verification. The signed listing constitutes a part of the contractual agreement for the creation of the customer mask. SGS-THOMSON sales organization will provide detailed information on contractual points.

ST6050 Part Number



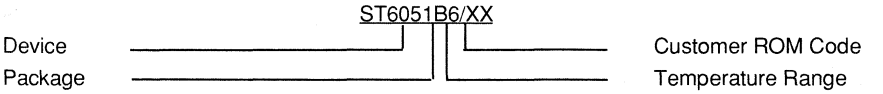
Device : ST6050

Package : C : 44 PLCC

Temperature range : – 40°C to 85°C 6
– 40°C to 110°C 7

Marking : it is by default equivalent to the sales type (part number). If a special marking is required see attached option list chart.

ST6051 Part Number



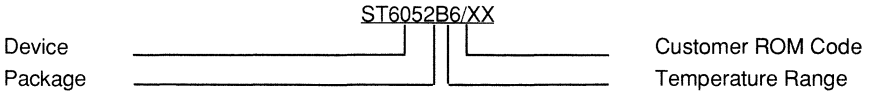
Device : ST6051

Package : B : 48 Plastic Dual-in-line

Temperature range : – 40°C to 85°C 6
– 40°C to 110°C 7

Marking : it is by default equivalent to the sales type (part number). If a special marking is required see attached option list chart.

ST6052 Part Number



Device : ST6052

Package : B : 40 Plastic Dual-in-line

Temperature range : – 40°C to 85°C 6
– 40°C to 110°C 7

Marking : it is by default equivalent to the sales type (part number). If a special marking is required see attached option list chart.

ST605X MICROCONTROLLER OPTION LIST

Customer .....
Address .....
Contact .....
Phone No .....
Reference .....

Device [ ] (d)
Package [ ] (p)
Temperature Range [ ] (t)
For marking two lines with 10 characters maximum are possible
Special Marking [ ] (y/n) Line 1 "....." (M)
Line 2 "....." (M)

[d] 1=ST6050, 2=ST6051, 3=ST6052

[p] B=Plastic Dual in Line, C=PLCC

(t) 6 = – 40 to 85°C
7 = – 40 to 110°C

(M) Letters, digits, '.', '-', '/' and spaces only

Signature .....
Date .....

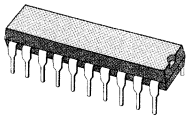
SGS-THOMSON MICROELECTRONICS

ST6210/E10
ST6215/E15

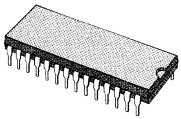
8 BIT HCMOS MICROCONTROLLERS WITH A/D CONVERTER

PRELIMINARY DATA

- 8-BIT ARCHITECTURE
- HCMOS LOW POWER CONSUMPTION
- SINGLE POWER SUPPLY – 3.0V TO 6.0V (ROM VERSION)
- 1.625µS TCYCLE (with 8MHz clock)
- RUN, WAIT & STOP MODES
- 5 DIFFERENT INTERRUPT VECTORS
- LOOK-UP TABLE CAPABILITY IN ROM
- USER ROM : 1828 BYTES (2K EPROM in ST62E10/15)
- RESERVED ROM : 220 BYTES
- DATA ROM/EPROM : USER SELECTABLE (physically in program ROM/EPROM)
- DATA RAM : 64 BYTES
- 12/20 FULLY SOFTWARE PROGRAMMABLE INPUTS/OUTPUTS AS :
  INPUTS WITH OR WITHOUT INTERNAL PULL-UP RESISTORS
  INTERRUPT GENERATING INPUTS WITH PULL-UP RESISTORS
  OPEN-DRAIN OR PUSH-PULL OUTPUTS
  ANALOG INPUTS
- 4 I/O PINS CAN SINK 10MA FOR DIRECT LED DRIVING
- 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER (Timer)
- DIGITAL WATCHDOG/TIMER (DWD)
- 8-BIT A/D CONVERTER WITH UP TO 8 (ST6210) AND 16 (ST6215) (ROM Version)
- ANALOG INPUTS
- ONE EXTERNAL NOT MASKABLE INTERRUPT INPUT
- ON-CHIP CLOCK OSCILLATOR
- POWER-ON RESET
- PDIP-20,SO-20 (ST6210), CDIP-20-W (ST62E10) PACKAGES
- PDIP-28,SO-28 (ST6215), CDIP-28-W (ST62E15) PACKAGES
- SAME ST62XX INSTRUCTION SET
- EASY TO PROGRAM
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- WAIT, STOP AND BIT MANIPULATION INSTRUCTIONS
- TRUE LIFO 6 LEVEL STACK
- 9 POWERFUL ADDRESSING MODES
- THE ACCUMULATOR, THE X, Y, V & W REGISTERS, THE PORT AND PERIPHERALS DATA/CONTROL REGISTERS ARE ADDRESSED IN THE DATA SPACE AS RAM LOCATIONS
- THE DEVELOPMENT TOOL OF THE ST621X MICROCONTROLLER FAMILY CONSISTS OF THE EMST62-HW/E1X EMULATION AND DEVELOPMENT PACKAGE CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN IBM PC
- ST62E10 AND ST62E15 EPROM VERSION ARE AVAILABLE FOR LOW-VOLUME PRODUCTION AND EMULATION PURPOSES



DIP-20



DIP-28

(Order Codes at the end of the datasheet)

GENERAL DESCRIPTION

The ST6210/ST6215 microcontrollers are members of the 8-bit HCMOS ST62XX family, a series of devices oriented to low-medium complexity applications. All ST60XX members are based on a building block approach: to a common core is associated a combination of on-chip peripherals (macrocells) available from a standard library to form around the core all the existing and future ST6 devices.These peripherals are designed with the same core technology giving full compatibility, short design and testing time. The macrocells of the ST6210/E10 and ST6215/E15 are: the Timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler (Timer), the 8-bit A/D Converter with up to 8 (ST6210/E10) and up to 16 (ST6215/E15) analog inputs (A/D inputs are alternate functions of I/O pins), the digital watchdog/timer (DWD). Thanks to these peripherals the ST6210/E10 & ST6215/E15 are well suited for automotive, industrial & consumer applications. The ST62E10 and ST62E15 EPROM versions are available for prototypes and low-volume production.

Figure 1 : ST6210/ST62E10 Pin Configuration.

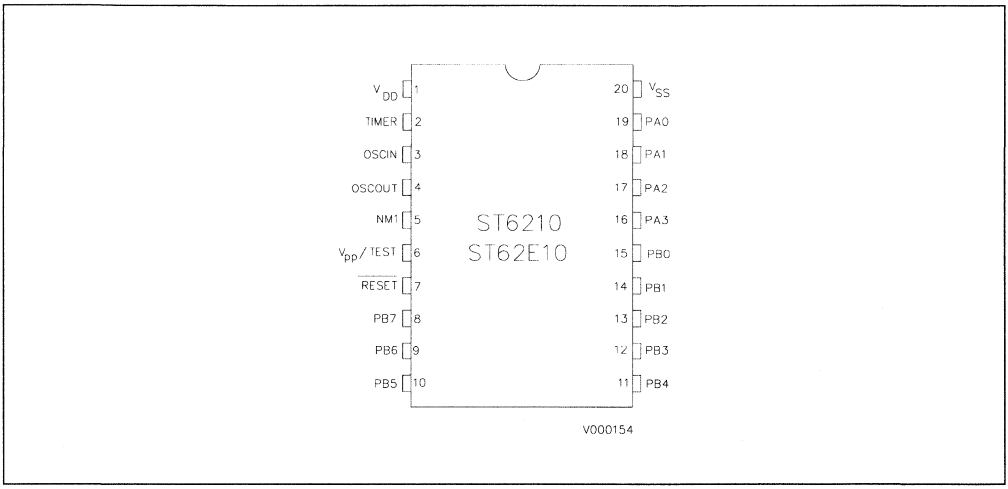
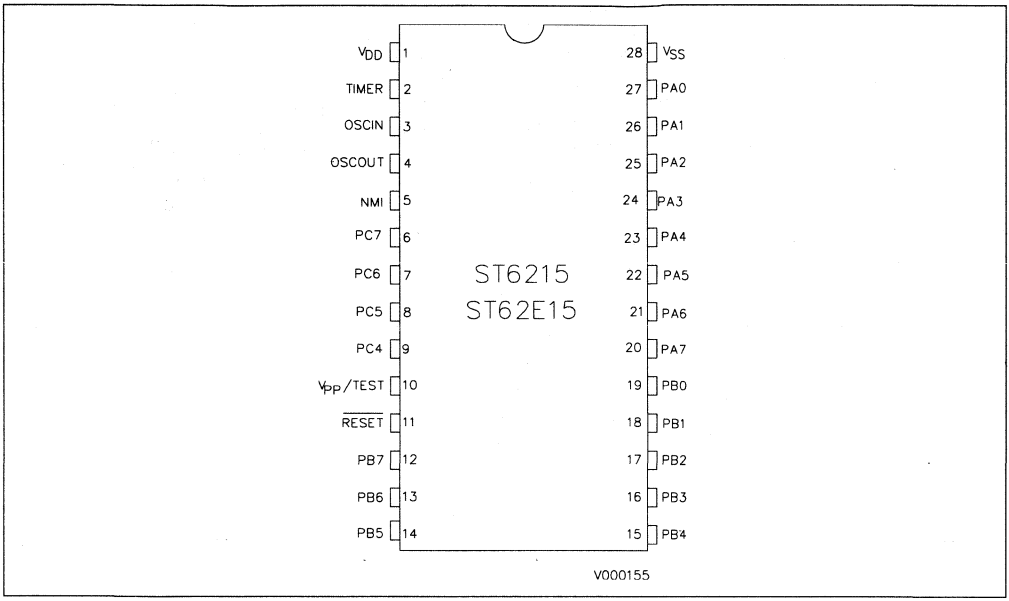


Figure 2 : ST6215/E15 Pin Configuration.



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. VDD is power and VSS is the ground connection.

OSCIN and OSCOUT. These pins are internally connected with the on-chip oscillator circuit. A crystal quartz, a resistor/capacitor network or a ceramic resonator can be connected between these two pins in order to allow a right operating of the MCU. The OSCIN pin is the input pin, the OSCOUT pin is the output pin.

$\overline{\text{RESET}}$. The active low RESET pin is used to restart the microcontroller to the beginning of its program.

TEST/VPP. The TEST pin is used to place the MCU into special operating mode. If TEST is held at V_{SS} the MCU enters the normal operating mode. If TEST is held at a high logic level the test operating mode is automatically selected (the user should connect this pin to V_{SS} for normal operation). If this pin is connected to a +12.5V level during the reset phase the EPROM programming mode is entered (EPROM versions only).

NMI. The NMI pin provides the capability for asynchronous applying an external not maskable interrupt to the MCU. The NMI is falling edge sensitive.

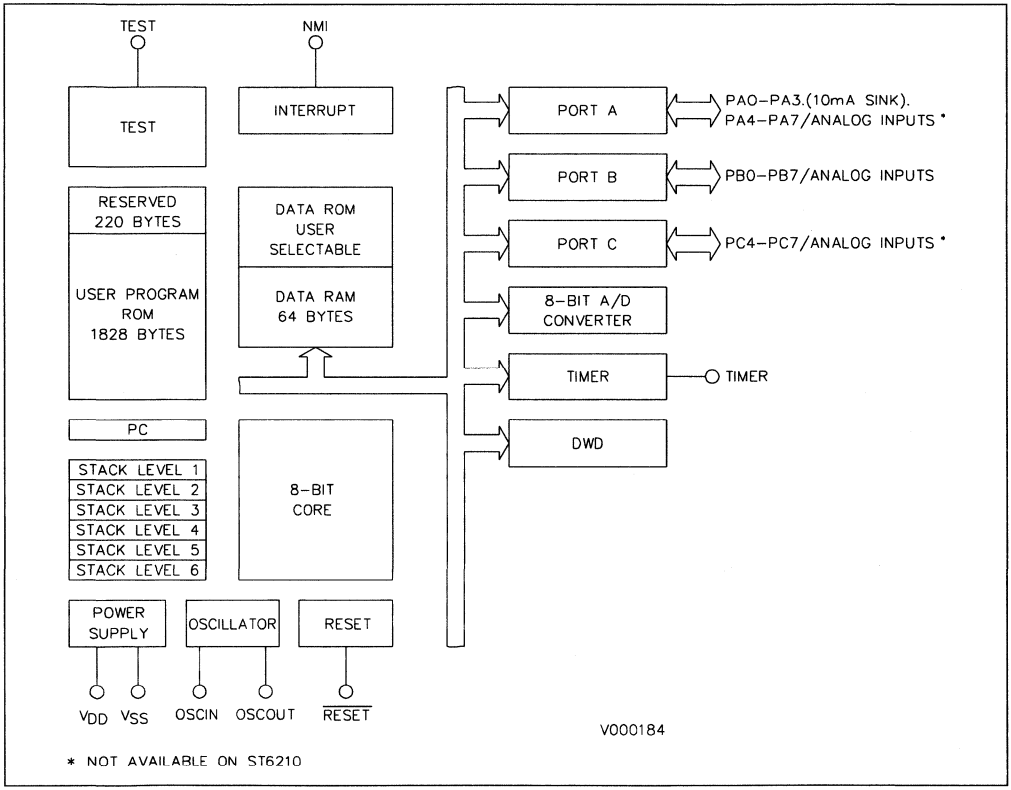
TIMER. This in the timer I/O pin. In input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time out occurs.

PA0-PA3,PA4-PA7(*). These 8 lines are organized as one I/O port (A). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs. PA0-PA3 can also sink 10mA for direct led driving while PA4-PA7 can be programmed as analog inputs for the A/D converter. (*) PA4-PA7 are not available on ST6210/E10.

PB0-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs and as analog inputs for the A/D converter.

PC4-PC7(*). These 4 lines are organized as one I/O port (C). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs and as analog inputs for the A/D converter.(*) PC4-PC7 are not available on ST6210/E10.

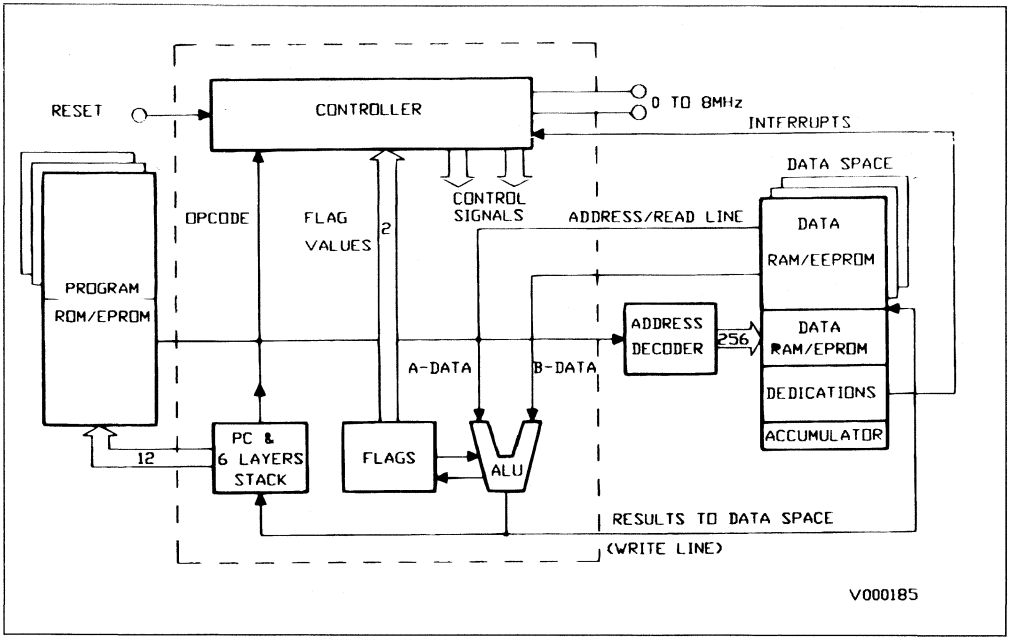
Figure 3 : ST6210/ST6215 Block Diagram.



ST62XX CORE

The ultra small and fast Micro-core of the ST6210/E10 and ST6215/E15 microcontrollers is designed to provide the economy of small die size through advanced HCMOS technologies. The ST62XX core can directly address 4 Kbyte of program memory with extension capability by 2 Kbyte bank addition. The directly addressable data space is 256 bytes sized with extension capability by 64 byte bank addition. The data ROM which is addressed in the data space is physically located in the program area. The core includes an 8-bit accumulator, two 8-bit index registers and a 12-bit program counter. Three pairs of flags monitors the processor operations while a six levels LIFO hardware stack is available for subroutine & interrupt return address storage. One NMI and four normal interrupt vectors are available. STOP and WAIT modes are included to reduce overall power consumption.

Figure 4 : ST62XX Core Block Diagram.



I/O PORTS

The ST6210/E10, ST6215/E15 I/O ports are fully software programmable to be configured as: inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs, analog inputs and in addition four I/O pins can sink 10mA for direct led driving.

TIMER

The Timer peripheral consists of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes: event counter, input gated and output modes. The content of the 8-bit counter can be read/written in the Timer/Counter register. The state of the 7-bit prescaler can be read in the prescaler register . A maskable interrupt is associated with the end-of-count.

DIGITAL WATCHDOG/TIMER

The digital watchdog/timer consists of a down counter that can be used to provide a controlled recovery from a software upset or as a simple 7-bit timer for general purpose counting. The check time can be set differently for different routines within the general program. After a reset the watchdog/timer is in off-state. The watchdog should be activated inside the Reset restart routine. Once the watchdog is enabled it can not be cleared by software without generating a Reset. The reset is prevented if the register is reloaded with the desired value before the watchdog register time-out. If the watchdog is active the STOP instruction is deactivated and a WAIT instruction is automatically executed instead of the STOP.

8-BIT A/D CONVERTER

The ST6210/E10, ST6215/E15 A/D converter is an 8-bit analog to digital converter offering 8-bit resolution with $\pm$ 1/2 bit of linearity and a conversion time of 70uS. ST6210/E10 has up to 8 analog inputs while in the ST6215/E15 the number of input pin can be extendeded up to 16 (alternate functions of I/O ports). The ST621X A/D peripheral converts by a process of successive approximations. The clock is derived from the oscillator.

DEVELOPMENT SUPPORT & EMULATION SYSTEM

The ST62XX development system offers powerful in-circuit emulator and easy-to-use sets (dedicated boards) of modular hardware and software tools to shorten the total system development time of the final application. The ST62XX emulator offers emulation power with plug-in flexibility in the selection of emulation hardware modules for the dedicated macrocells. The emulator can be interfaced with a standard RS232 serial link to industry standard MS-DOS personal computers. The ST62E10 and ST62E15 EPROM versions are also available to provide flexibility and cost effectiveness in prototypes or preproduction.

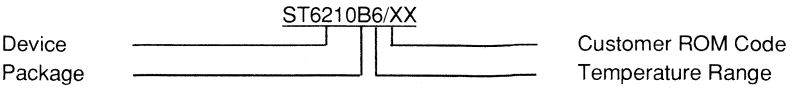
ORDERING INFORMATION

The following chapter deals with the procedure for transfer the Program/Data ROM codes to SGS-THOMSON.

Communication of the ROM codes. To communicate the contents of Program/Data ROM memories to SGS-THOMSON, the customer has to send two 2764 EPROM with exactly the same addresses as for the ROM version.
All unused bytes must be set to FFH. For shipment to SGS-THOMSON the EPROMs should be placed in a conductive IC carrier and packaged carefully.

Listing Generation & Verification. When SGS-THOMSON receives the EPROMs, they are compared and a computer listing is generated from them. This listing refers exactly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. SGS-THOMSON will also program one 2764 EPROM from the data file corresponding to the listing to help the customer in its verification. The signed listing constitutes a part of the contractual agreement for the creation of the customer mask. SGS-THOMSON sales organization will provide detailed information on contractual points.

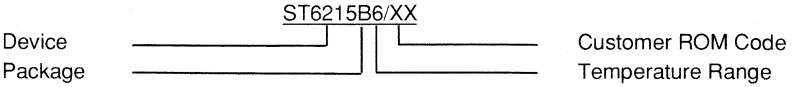
ST6210 Part Number



Device : ST6210
Package : B Plastic Dual-in-line Package
Package : M Plastic SO Package
Temperature range : – 40°C to 85°C 6
– 40°C to 110°C 7

Marking : it is by default equivalent to the sales type (part number). If a special marking is required see attached option list chart.

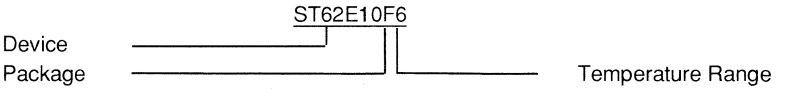
ST6215 Part Number



Device : ST6215
Package : B Plastic Dual-in-line Package
Package : M Plastic SO Package
Temperature range : – 40°C to 85°C 6
– 40°C to 110°C 7

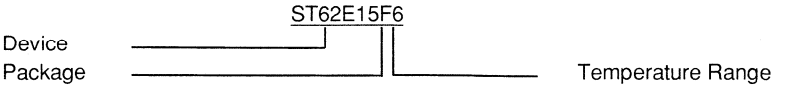
Marking : it is by default equivalent to the sales type (part number). If a special marking is required see attached option list chart.

ST62E10 Part Number



Device : ST62E10
Package : F Window Frit-Seal Package (DIL)
Temperature range : – 40°C to 85°C 6
– 40°C to 110°C 7

ST62E15 Part Number



Device : ST62E15
Package : F Window Frit-Seal Package (DIL)
Temperature range : – 40°C to 85°C 6
– 40°C to 110°C 7

ST621X MICROCONTROLLER OPTION LIST

Customer .....
Address .....
Contact .....
Phone No .....
Reference .....

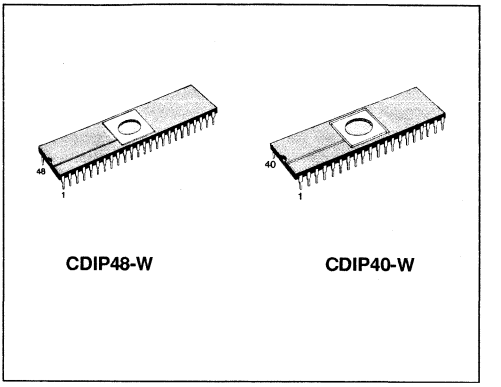
Device [ ] (d)
Package [ ] (p)
Temperature Range [ ] (t)
For marking one line with 11 characters maximum is possible
Special Marking [ ] (y/n) Line 1 "....." (M)
[d] 1 = ST6210, 2 = ST6215
[p] B = Plastic Dual in Line, M = Plastic SO
(t) 6 = – 40 to 85°C
7 = – 40 to 110°C
(M) Letters, digits, '.', '-', '/' and spaces only

Signature .....
Date .....

ST9 8K EPROM HCMOS MICROCONTROLLER

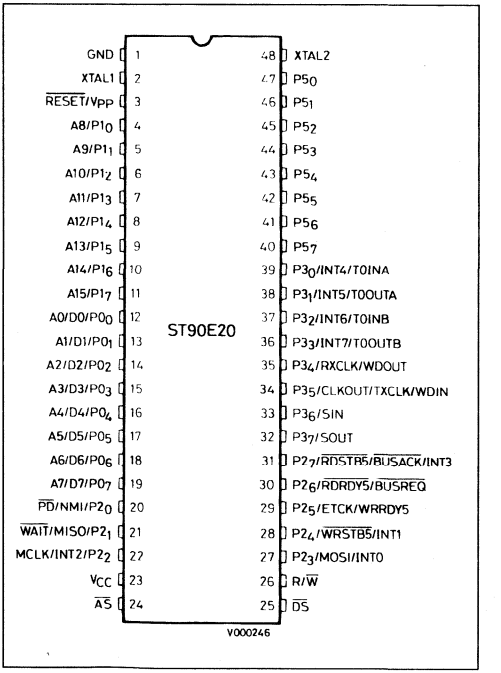
ADVANCE DATA

- COMPLETE MICROCONTROLLER, 8K BYTES OF EPROM, 256 BYTES OF REGISTER FILE WITH 224 GENERAL PURPOSE REGISTERS AVAILABLE AS RAM, ACCUMULATOR OR INDEX POINTERS. THE ON-CHIP EPROM CAN BE PROGRAMMED BY USING THE ST90E2X PROGRAMMING BOARD DEVELOPED AND DELIVERED BY SGS-THOMSON. FULLY COMPATIBLE WITH THE STANDARD ROM VERSION
- 8/16-BIT CORE WITH FULL FEATURE DMA CONTROLLER AND POWERFUL INTERRUPT HANDLER AND MSPI OR SBUS/I^2CBUS SERIAL INTERFACE
- UP TO 8 EXTERNAL INTERRUPTS PLUS 1 NOT MASKABLE INTERRUPT
- 16-BIT WATCHDOG TIMER FOR SYSTEM INTEGRITY
- ONE 16-BIT TIMER, WITH AN 8-BIT PRESCALER AND 14 OPERATING MODES, ALLOWING EASY USE FOR COMPLEX PWM FUNCTIONS AND MANY OTHER TIMING SYSTEM FUNCTIONS
- 2 ON-CHIP DMA CHANNELS ASSOCIATED TO THE TIMER
- FULL FUNCTION SERIAL COMMUNICATION INTERFACE (SCI) WITH 110 TO 19200 BAUD RATE GENERATOR, ASYNCHRONOUS AND BYTE SYNCHRONOUS CAPABILITY (fully programmable format) AND ADDRESS/WAKE-UP BIT OPTION
- FIVE 8-BIT I/O PORTS WITH PROGRAMMABLE INPUT THRESHOLDS AND OUTPUT CHARACTERISTICS. ALTERNATE FUNCTIONS ALLOW FULL USE OF ALL LINES
- FULL FEATURES SOFTWARE DEVELOPMENT TOOLS, INCLUDING ASSEMBLER, LINKER, C-COMPILER, ARCHIVER, SOFTWARE AND HARDWARE EMULATORS
- PACKAGES AVAILABLE :
  - ST90E20 48-PIN DUAL IN LINE CERAMIC MULTILAYER WITH LENS
  - ST90E21 40-PIN DUAL IN LINE CERAMIC MULTILAYER WITH LENS
  - ST90E23 44-LEAD CERAMIC LEADED CHIP CARRIER WITH LENS



CDIP48-W **CDIP40-W**

Figure 1 : ST90E20 Pin Configuration.



GENERAL DESCRIPTION

The ST90E20, ST90E21 and ST90E23 are EPROM members of the ST9 family of microcontroller, completely developed and produced by SGS-THOMSON using the HCMOS 1.5µ n-well process.

They are fully compatible with their ROM version ST9020/21/23 and can be configured as : stand alone microcontroller with 8K bytes of on-chip EPROM : traditional microcontroller that manage up to 120K bytes of external memory, or parallel processing elements in a system with other processors and peripheral controllers.

The 8K x 8 on-chip EPROM can be programmed off line using the ST90E2X programming board delivered by SGS-THOMSON (Order Code ST90E2XEPR).

ARCHITECTURE

The ST90E20/21/23 architecture is of prime importance due to the modular philosophy of the system.

The nucleus of the ST90E20/21/23 is an advanced Core including the CPU, the Register File, a 16-bit Timer/Watchdog with 8-bit prescaler, a Master Serial Peripheral Interface and SBUS/I^{2}CBUS interface, and two 8-bit I/O Ports. The Core has its own internal busses in addition to those used as link between magacells.

Microcontroller applications demands powerful I/O capabilities. The ST90E20/21/23 fulfill this with up to 40 I/O lines dedicated to Input/Output. These lines are grouped into up to 5 ports of eight lines each and are configured under software control to provide timing, status signals, address/data bus for interfacing external memory, timer inputs and outputs, external interrupts and serial or parallel I/O with or without handshake.

Because the multiplexed address/data bus is merged with the I/O oriented ports, the ST90E20/21/22 can assume many different memory and I/O configurations. These configurations range from a self-contained Microcontroller to a Microprocessor that can address 120K bytes of external memory.

Three basic address spaces are available to support this wide range of configurations : Program Memory (internal and external), Data Memory (external) and Register File.

One 16-bit Timer with an 8-bit prescaler and 14 operating modes allow easy use for complex PWM functions and many other timing system functions by the usage of two associated DMA channels.

To complete the device a full duplex Serial Communication Interface is available with 110 to 19200 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.

Figure 2 : ST90E21 Pin Configuration.

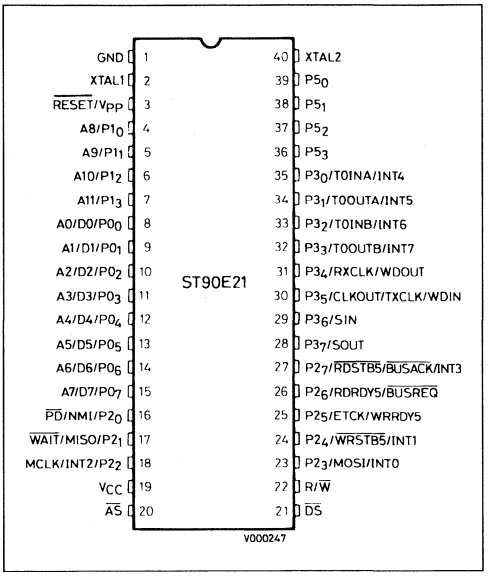
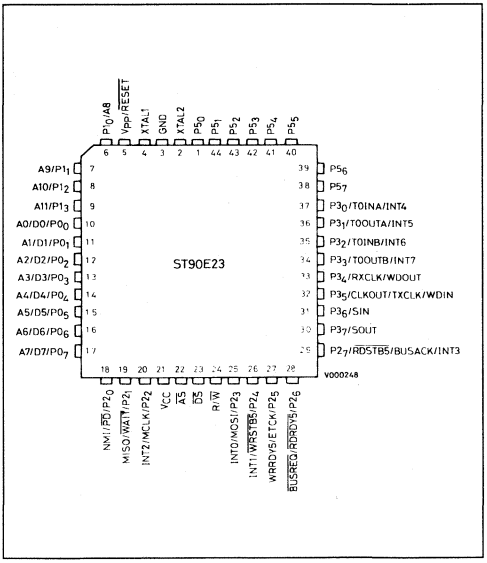
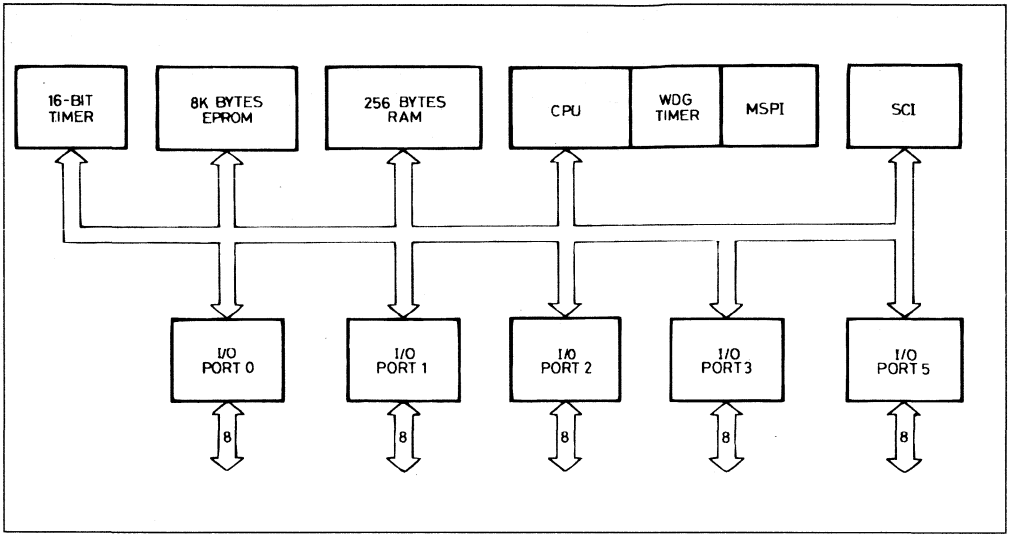


Figure 3 : ST90E23 Pin Configuration.



ARCHITECTURE (continued)

Figure 4 : ST90E20 Block Diagram.



PIN DESCRIPTION

$P0_0$-$P0_7$. I/O Port Lines (input/output, TTL or CMOS compatible). 8 Lines bit programmable that can be configured under program control for I/O or multiplexed address (A0-A7) and data (D0-D7) lines used to interface with Program/Data memory.

$P1_0$-$P1_7$. I/O Port Lines (input/outputs, TTL or CMOS compatible). 8 Lines bit programmable that can be configured under program control for I/O or external memory expansion (A8-A15).

$P2_0$-$P2_7$. I/O Port Lines (input/outputs, TTL or CMOS compatible) 8 Lines bit programmable that can be configured under program control for I/O or, in alternate function, as control lines for some of external interrupts, the Master Serial Peripheral Interface and SBUS/I_2CBUS interface, the handshake protocol or the Timer-DMA control lines of Ports 5, the external Bus control lines, the WAIT and Program/Data signals and the Timer 0 external clock input.

$P3_0$-$P3_7$. I/O Port Lines (input/outputs, TTL or CMOS compatible) 8 Lines bit programable that can be configured under program control for I/O or, in alternate function, as input and output lines of the multifunction 16-bit Timer 0 and as Serial Communication Interface protocol with its control lines.

$P5_0$-$P5_7$. I/O Port Lines (input/outputs, TTL or CMOS compatible) 8 Lines bit programmable that can be configured under program control for I/O or, in alternate function, to manage the parallel handshake protocol or the Timer-DMA function.

$\overline{AS}$. Address Strobe (output, active low, 3-State). Address strobe is pulsed low once at the beginning of each machine cycle. The rising edge of AS indicates that address, Read/Write (R/W), and Data Memory (DM) signals are valid when output for external program or data memory transfers. Under program control, AS can be placed in a high-impedance state along with Ports 0 and 1, Data Strobe (DS), and R/W.

$\overline{DS}$. Data Strobe (output, active low, 3-State). Data strobe provides the timing for data movement to or from Port 0 for each external memory transfer. During a write cycle, data out is valid at the leading edge of DS. During a read cycle, data in must be valid prior to the trailing edge of DS.

It can be placed in a high impendance state along with Port 0, Port 1, AS and R/W.

R/$\overline{W}$. Read/Write (output, 3-State). Read/Write determines the direction of data transfer for external memory transactions. R/W is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high-impedance state, with Port 0, Port 1, AS and DS.

$\overline{\text{RESET}}$/V_{PP}. Reset or V_{PP} (input). The ST9 is initialized by Reset signals, active low. With the deactivation of RESET, program execution begins from the Program Memory location, pointed by the vector contained in program memory locations 00H and 01H. If held low, RESET acts a register file protection during power-down and power-up sequences. In Eprom-Mode this pin functions as V_{PP} and is pulsed to 12.5V ± 300mV to perform on-chip EPROM programming.

XTAL1, XTAL2. Crystal 1, Crystal 2 (oscillator input and output). These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. XTAL1-Input of the oscillator inverter and internal clock generator ; XTAL2-Output of the oscillator inverter.

V_{DD}. Main Power Supply Voltage (5V).

V_{SS}. Digital Circuit Ground.

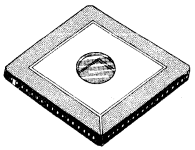
SGS-THOMSON MICROELECTRONICS

ST90E30
ST90E31-ST90E32

ST9 8K EPROM HCMOS MICROCONTROLLER

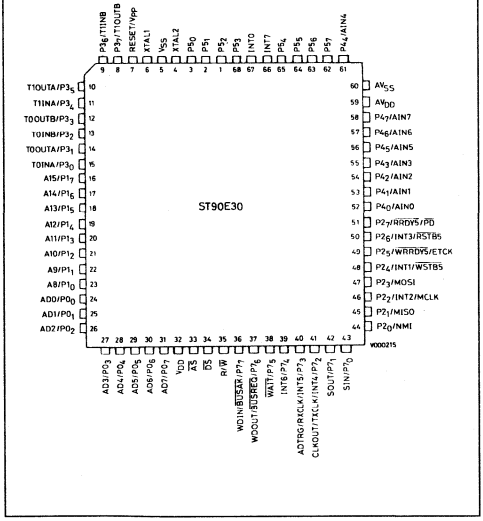
ADVANCE DATA

- COMPLETE MICROCONTROLLER, 8K BYTES OF EPROM, 256 BYTES OF REGISTER FILE WITH 224 GENERAL PURPOSE REGISTERS AVAILABLE AS RAM, ACCUMULATOR OR INDEX POINTERS. THE ON-CHIP EPROM CAN BE PROGRAMMED BY USING THE ST9 PROGRAMMING BOARD DEVELOPED AND DELIVERED BY SGS-THOMSON MICROELECTRONICS. FULLY COMPATIBLE WITH THE STANDARD ROM VERSION
- 8/16-BIT CORE WITH FULL FEATURE DMA CONTROLLER AND POWERFUL INTERRUPT HANDLER AND MSPI OR I^2CBUS SERIAL INTERFACE
- 16-BIT WATCHDOG TIMER FOR SYSTEM INTEGRITY
- TWO 16-BIT TIMERS, EACH WITH AN 8-BIT PRESCALER AND 14 OPERATING MODES, ALLOWING EASY USE FOR COMPLEX PWM FUNCTIONS AND MANY OTHER TIMING SYSTEM FUNCTIONS
- 8-CHANNEL ANALOG TO DIGITAL CONVERTER, WITH INTEGRAL SAMPLE AND HOLD, FAST 16µs CONVERTION TIME AND 8-BIT ± 1/2 LSB RESOLUTION
- FULL FUNCTION SERIAL I/O INTERFACE WITH 110 TO 19200 BAUD RATE GENERATOR, ASYNCHRONOUS AND BYTE SYNCHRONOUS CAPABILITY (fully programmable format) AND ADDRESS/WAKE-UP BIT OPTION
- SIX 8-BIT I/O PORTS WITH PROGRAMMABLE INPUT THRESHOLDS AND OUTPUT CHARACTERISTICS. ALTERNATE FUNCTIONS ALLOW FULL USE OF ALL LINES
- FULL FEATURES SOFTWARE DEVELOPMENT TOOLS, INCLUDING ASSEMBLER, LINKER, C-COMPILER, ARCHIVER, SOFTWARE AND HARDWARE EMULATORS
- AVAILABLE IN 48 DUAL-IN-LINE (ST90E31), 64 DUAL-IN-LINE-SHRINK (ST90E32) AND 68 LEADED CHIP CARRIER (ST90E30) CERAMIC PACKAGES



LLCC68-W

Figure 1 : ST90E30 Pin Configuration.



GENERAL DESCRIPTION

The ST90E30, ST90E31 and ST90E32 are EPROM members of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON using the HCMOS 1.5µ n-well process.

They are fully compatible with their ROM version ST9030 and can be configured as : stand alone microcontrollers with 8K bytes os on-chip EPROM : traditional microcontrollers that manage up to 120K bytes of external memory, or parallel processing elements in a system with other processors and peripheral controllers.

The 8K x 8 on-chip EPROM can be programmed off line using the ST9 programming board delivered by SGS-THOMSON.

ARCHITECTURE

The ST90E30 architecture is of prime importance due to the modular philosophy of the system.

The nucleus of teh ST90E30 is an advanced Core including the CPU, the Register File, a 16-bit Timer/Watchdog with 8-bit prescaler, a Master Serial Peripheral and I^2CBUS interface, and two 8-bit I/O Ports. The Core has its own internal busses in addition to those used as link between magacells. Microcontroller applications demands powerful I/O capabilities. The ST90E30 fulfills this with up to 56 I/O lines dedicated to Input/Output. These lines are grouped into up to 7 ports of eight lines each and are configured under software control to provide timing, status signals, address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Because the multiplexd address/data bus is merged with the I/O oriented ports, the ST90E30 can assume many different memory and I/O configurations. These configurations range from as self-contained microcontroller to a Microprocessor that can address 120K bytes of external memory.

Three basic address spaces are available to support this wide range of configurations : Program Memory (internal and external), Data Memory (external) and Register File.

Two 16-bit Timers, each with an 8-bit prescaler and 14 operating modes allow easy use for complex PWM functions and many other timing system functions.

In addition there is an 8 channel Analogue to Digital Converter with integral sample and hold, fast 15µ conversion time and 8-bit ± 1/2 LSB resolution.

To complete the device a full duplex Serial I/O interface is available with 110 to 19200 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.

Figure 2 : ST90E31 Pin Configuration.

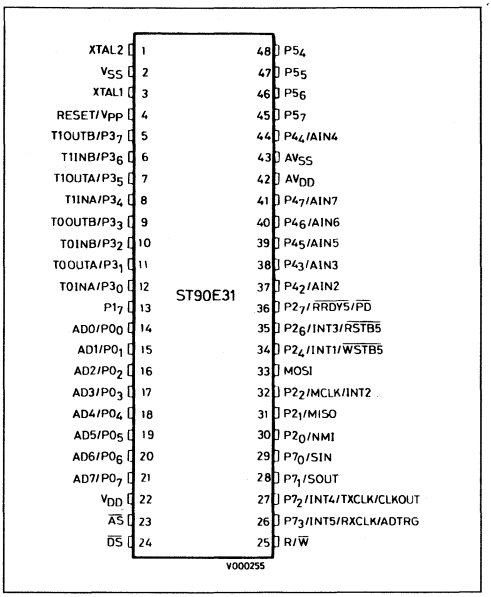
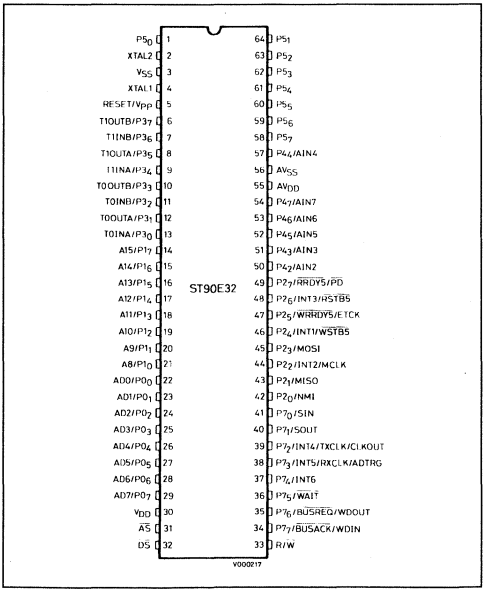
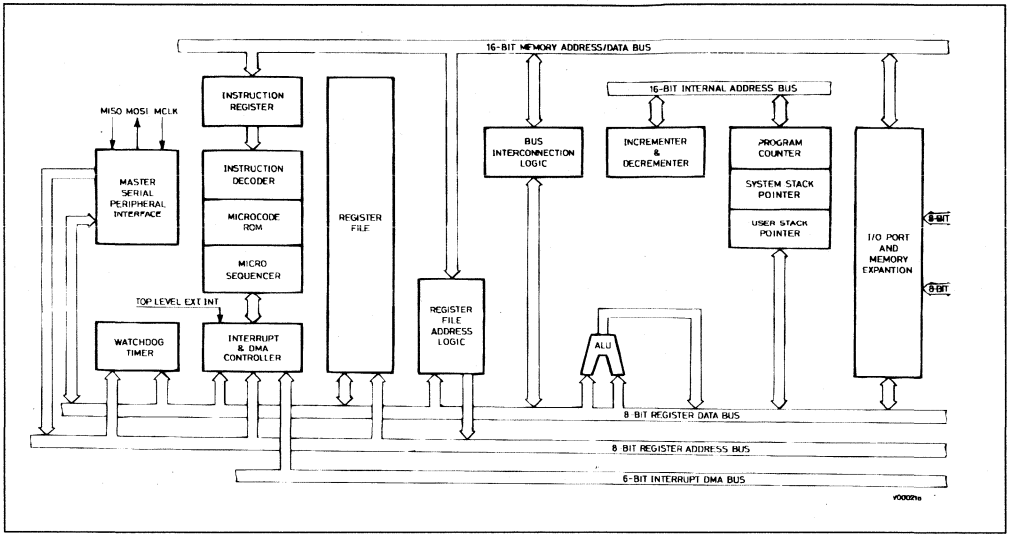


Figure 3 : ST90E32 Pin Configuration.



ARCHITECTURE (continued)

Figure 4 : ST9 Core Block Diagram.



PIN DESCRIPTION

$P0_0$-$P0_7$. I/O Port Lines (input/output, TTL or CMOS compatible). 8 lines bit programmable that can be configured under program control for I/O or multiplexed address (A0-A7) and data (D0-D7) lines used to interface with Program/Data memory.

$P1_0$-$P1_7$. I/O Port Lines (input/outputs, TTL or CMOS compatible). 8 lines bit programmable that can be configured under program control for I/O or external memory expansion (A8-A15).

$P2_0$-$P2_7$. I/O Port Lines (input/outputs, TTL or CMOS compatible) 8 lines bit programmable that can be configured under program control for I/O or, in alternate function, as control lines for external interrupts, the Master Serial Peripheral and I^2CBUS interface and the handshake control lines of Ports 5.

$P3_0$-$P3_7$. I/O Port Lines (input/outputs, TTL or CMOS compatible) 8 lines bit programmable that can be configured under program control for I/O or, in alternate function, as input and output lines of the 2 x 16-bit Timers (timer 0 and timer 1).

$P4_0$-$P4_7$. I/O Port Lines (input/outputs, TTL or CMOS compatible) 8 lines bit programmable that can be configured under program control for I/O or, in alternate function, as analog inputs of the Analog to Digital Converter.

$P5_0$-$P5_7$. I/O Port Lines (input/outputs, TTL or CMOS compatible) 8 Lines bit programmable that can be configured under program control for I/O or, in alternate function, to manage the parallel handshake protocol or the Timer-DMA function.

$P7_6$-$P7_7$. I/O Port Lines (input/output, TTL or CMOS compatible). 8 Lines bit programmable that can be configured under program control for I/O or, in alternate function, as control lines for the Serial Communication Controller, the Timer/Watchdog input/output lines, the External bus control lines, the Wait signal and some of the external Interrupts.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

INTO. External Interrupt Input of channel 0.

INT7. External Interrupt Input of channel 7.

$\overline{AS}$. Address Strobe (output, active low, 3-State). Address strobe is pulsed low once at the beginning of each machine cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/W), and Data Memory (DM) signals are valid when output for external program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Ports 0 and 1, Data Strobe ($\overline{DS}$), and R/$\overline{W}$.

$\overline{DS}$. Data Strobe (output, active low, 3-State). Data strobe provides the timing for data movement to or from Port 0 for each external memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a write cycle, data in must be valid prior to the trailing ede of $\overline{DS}$. It can be placed in a high impendance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. Read/Write (output, 3-State). Read/Write determines the direction of data transfer for external memory transactions. R/W is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high-impedance state, with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. Reset (input, active low). The ST9 is initialized by Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program Memory location pointed by the vector contained in program memory locations 00H and 01H. If held low, $\overline{RESET}$ acts a register file protection during power-down and power-up sequences.

XTAL1, XTAL2. Crystal 1, Crystal 2 (oscillator input and output). These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. XTAL1-Input of the oscillator inverter and internal clock generator ; XTAL2-Output of the oscillator inverter.

V_{DD}. Main Power Supply Voltage (5V).

V_{SS}. Digital Circuit Ground.

SGS-THOMSON MICROELECTRONICS

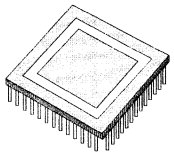
ST18940/41

DIGITAL SIGNAL PROCESSOR

ADVANCE DATA

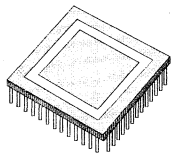
MAIN FEATURES

- 100ns MACHINE CYCLE TIME (1.2 CMOS Technology)
- PARALLEL HARVARD ARCHITECTURE
- TRIPLE DATA BUSES STRUCTURE
- 3 DATA MODES . SINGLE PRECISION
  . DOUBLE PRECISION
  . COMPLEX
- 32-BIT INSTRUCTION
- MULTIPLIER 16 x 16 —> 32, SIGNED AND UNSIGNED
- 32-BIT BARREL SHIFTER, 32-BIT ALU
- PROVISION FOR FLOATING POINT
- FOUR 32-BIT ACCUMULATORS, FOUR LEVEL 32-BIT FIFO
- IMMEDIATE AND COMPUTED BRANCH
- 8-LEVEL STACK
- 9 EXTERNAL AND 3 INTERNAL INTERRUPTS
- AUTOMATIC LOOP, UP TO 256 TIMES 32 INSTRUCTIONS
- 2 INDEPENDENT PARALLEL BUSES ; LOCAL AND SYSTEM
- FULL SPEED ACCESS TO EXTERNAL 64K x 16-BIT MEMORY ON THE LOCAL BUS
- HARDWARE AND/OR SOFTWARE WAIT STATES MODE TO ACCESS SLOWER EXTERNAL MEMORIES/PERIPHERALS, DMA CHANNEL
- 2 x 16 BYTES FIFO ON THE SYSTEM BUS
- SERIAL CHANNEL FOR DIRECT INTERFACE WITH CODEC, ISDN IC's...
- GENERAL PURPOSE PARALLEL PORT
- ON CHIP DATA RAM 2 x 256 x 16-bit
- FOUR INDEPENDENT ADDRESS CALCULATION UNITS
- ADDRESSING MODES : IMMEDIATE, DIRECT, INDIRECT WITH POST MODIFICATION, CIRCULAR, BIT REVERSED
- 2 VERSIONS : - ST18940 (PLCC/PGA 84) CLOSED VERSION WITH 3K x 32-BIT ON-CHIP PROGRAM ROM AND 512 x 16-BIT COEFFICIENT ROM
  - ST18941 (PGA 144) OPEN VERSION WITH 64K x 32-BIT OFF-CHIP PROGRAM ROM AND 128 x 16 BIT ON-CHIP COEFFICIENT RAM
- POWER DOWN MODE
- TYPICAL CONSUMPTION 0.5W



ST18941 - PIN GRID ARRAY - 144-pin

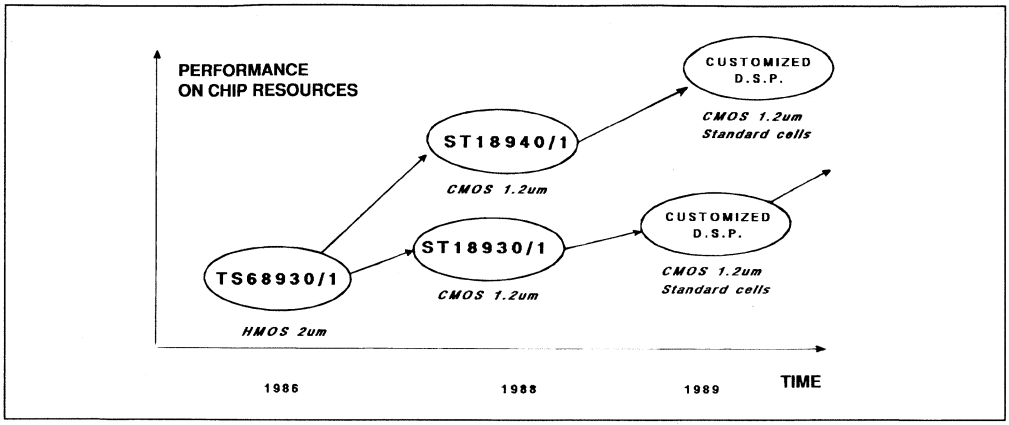
ST18940 - PLASTIC LEADED CHIP CARRIER - 84-pin



ST18940 - PIN GRID ARRAY - 84-pin

- WITH VERY HIGH SPEED COMPUTATION POWER, THE ST18 DIGITAL SIGNAL PROCESSOR FAMILY CAN BE USED IN AUTOMOTIVE ENVIRONMENT IN APPLICATIONS SUCH AS :
  - ENGINE CONTROL
  - VIBRATION ANALYSIS
  - ANTISKID BRAKES
  - ADAPTIVE RIDE CONTROL
  - GLOBAL POSITIONING
  - NAVIGATION
  - VOICE COMMANDS
  - AUDIO PROCESSING

Figure 1 : ST18 Family Highlights.



DEVELOPMENT SYSTEM

The ST18940-41 is supported by a complete set of hardware and software tools for system development. The software package includes an assembler/linker, a simulator, and a "C" compiler and optimizer which run under several VAX and PC operating systems. Hardware tools include a standalone emulator, an EPROM emulation module, a multiprocessor development station and an evaluation module (PC compatible).

DESCRIPTION

The ST18940/41 Digital Signal Processor is a member of SGS-THOMSON Microelectronics ST18 family.

The ST18 family comprises 3 products covering a wide spectrum of DSP applications. Complete development tools (hardware and software) are available as aids to efficient system designs.

The first processor in the ST18 family is the TS68930/31 (NMOS) with a 160ns machine cycle time. The second member of the family, the ST18930/31, is a CMOS version of the TS68930 with a faster instruction cycle time (80ns) and the inclusion of additional hardware and software features (The ST18930 is pin compatible with the TS68930).

The ST18940/41, which is described in this datasheet, is the third member in the family. It is upward compatible with the other members of the family, but provides enhanced arithmetic capabilities, addressing modes and additional I/O functions.

It is an advanced HCMOS single chip general purpose DSP designed for fast arithmetic intensive applications in the areas of telecommunications, modems, speech processing, graphic/image processing spectrum analysis, audio processing, digital filtering, high speed control, instrumentation, numeric processing...

The ST18940 structure is based on a triple 16-bit data bus, a 16 x 16 multiplier, a 32-bit ALU. The powerful parallel and serial Input/Output interfaces and the DMA channel contribute to the flexibility of the system interface with external environment.

Two versions are available :

- the ST18940 includes 3K x 32-bit program ROM and 512 x 16-bit coefficient ROM.
- the ST18941 microprocessor version can address up to 64K of program memory on a dedicated bus, thus providing true real-time emulation of the ST18940 ROM version. In addition to the two internal RAMs (X and Y), a 128 x 16-bit coefficient RAM is included for coefficient memory emulation.

Figure 2 : ST18940/41 Logic Functions.

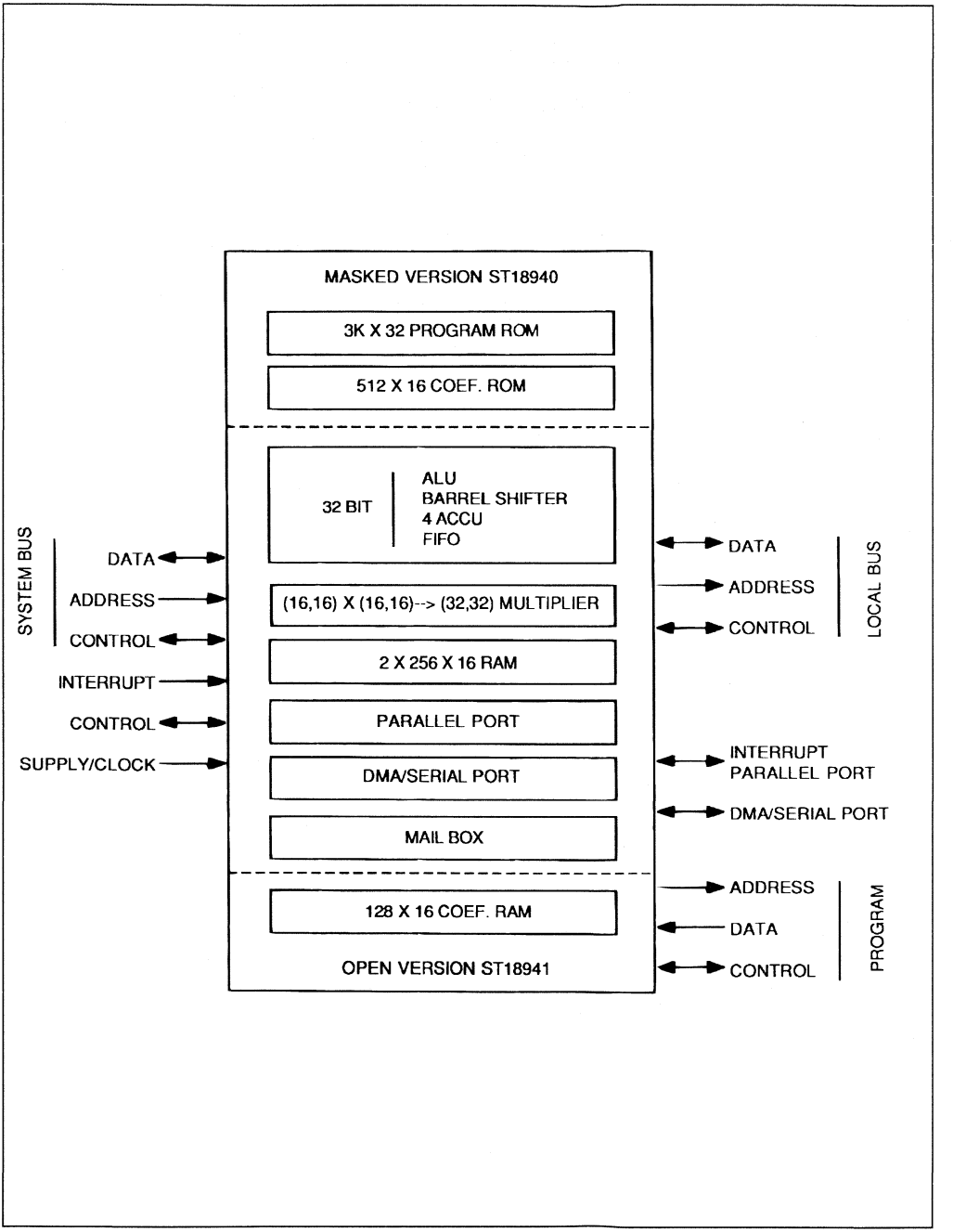
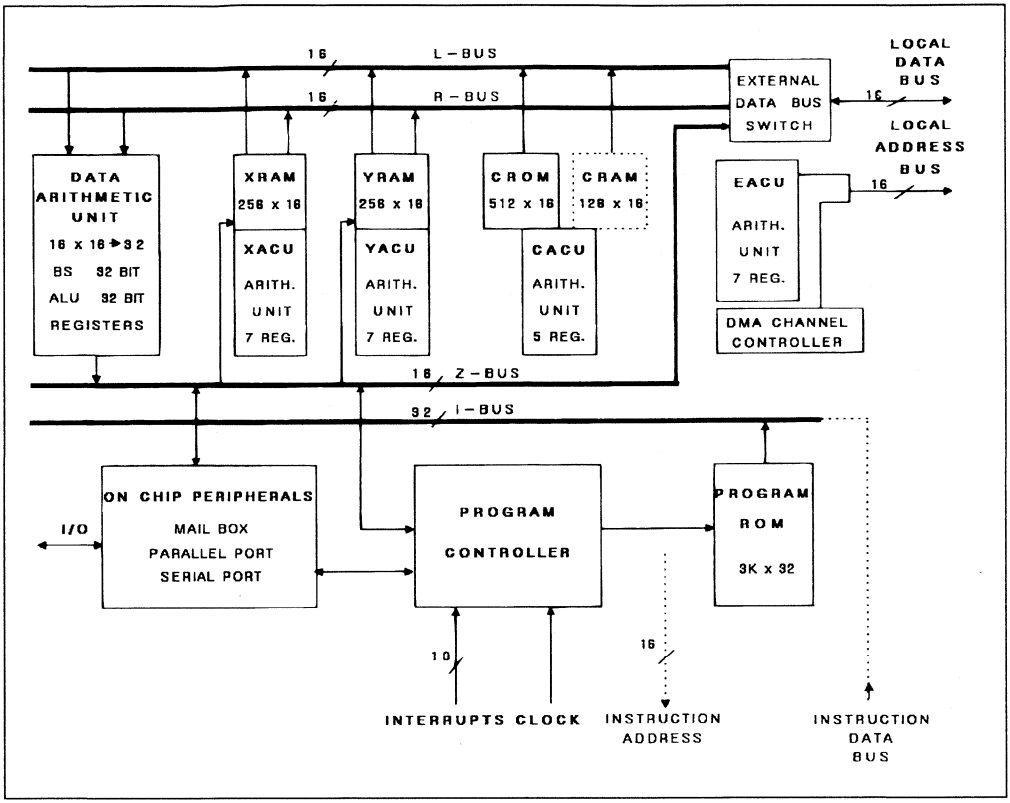


Figure 3 : ST18940/41 Block Diagram.



FUNCTIONAL DESCRIPTION

One of the key features of the ST1840/41 is that all hardware resources have been designed to support the following three data types :

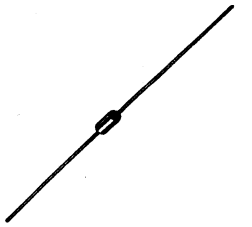
- simple precision : 16-bit data
- double precision : 32-bit data
- complex : 16-bit real and 16-bit imaginary

Any one of the above three arithmetic modes can be dynamically selected by means of a single program instruction. Once the mode has been selected, all resources (such as ALU, memories, registers, multiplier) are automatically configured for the appropriate operations. The same assembler instructions are used in all three modes. In double-precision and complex modes the data are stored in two contiguous memory locations, with an automatic adjustment of the address calculation unit. Two's complement representation is used throughout. In real mode, all instructions except branch are executed in one cycle time. In complex and double precision modes, all instructions are executed in two cycle times.

BZW04-5V8, B → 376, B
BZW04P5V8, B → 376, B

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 400 W / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 5.8 V → 376 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX B FOR BIDIRECTIONAL TYPES



F 126
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

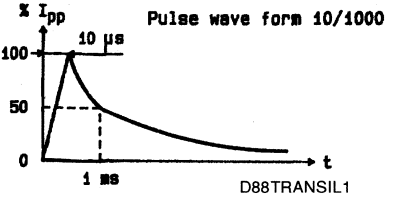
ABSOLUTE MAXIMUM RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	400	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 50 °C	1.7	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	50	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 55 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	60	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P BZW04P5V8	P BZW04P5V8B	1000	5.8	6.45	6.8	7.48	10	10.5	38	13.4	174	5.7	3500
BZW04-5V8	BZW04-5V8B	1000	5.8	6.45	6.8	7.14	10	10.5	38	13.4	174	5.7	3500
BZW04P6V4	P BZW04P6V4B	500	6.4	7.13	7.5	8.25	10	11.3	35.4	14.5	160	6.1	3100
BZW04-6V4	BZW04-6V4B	500	6.4	7.13	7.5	7.88	10	11.3	35.4	14.5	160	6.1	3100
BZW04P7V0	P BZW04P7V0B	200	7.02	7.79	8.2	9.02	10	12.1	33	15.5	148	6.5	2700
BZW04-7V0	BZW04-7V0B	200	7.02	7.79	8.2	8.61	10	12.1	33	15.5	148	6.5	2700
BZW04P7V8	BZW04P7V8B	50	7.78	8.65	9.1	10.0	1	13.4	30	17.1	134	6.8	2300
BZW04-7V8	BZW04-7V8B	50	7.78	8.65	9.1	9.55	1	13.4	30	17.1	134	6.8	2300
BZW04P8V5	BZW04P8V5B	10	8.55	9.50	10	11.0	1	14.5	27.6	18.6	258	7.3	2000
BZW04-8V5	BZW04-8V5B	10	8.55	9.50	10	10.50	1	14.5	27.6	18.6	258	7.3	2000
P BZW04P9V4	P BZW04P9V4B	5	9.4	10.5	11	12.1	1	15.6	25.7	20.3	236	7.5	1750
BZW04-9V4	BZW04-9V4B	5	9.4	10.5	11	11.6	1	15.6	25.7	20.3	236	7.5	1750
BZW04P10	BZW04P10B	5	10.2	11.4	12	13.2	1	16.7	24	21.7	221	7.8	1550
BZW04-10	BZW04-10B	5	10.2	11.4	12	12.6	1	16.7	24	21.7	221	7.8	1550
P BZW04P11	P BZW04P11B	5	11.1	12.4	13	14.3	1	18.2	22	23.6	203	8.1	1450
BZW04-11	BZW04-11B	5	11.1	12.4	13	13.7	1	18.2	22	23.6	203	8.1	1450
P BZW04P13	P BZW04P13B	5	12.8	14.3	15	16.5	1	21.2	19	27.2	176	8.4	1200
BZW04-13	BZW04-13B	5	12.8	14.3	15	15.8	1	21.2	19	27.2	176	8.4	1200
P BZW04P14	P BZW04P14B	5	13.6	15.2	16	17.6	1	22.5	17.8	28.9	166	8.6	1100
BZW04-14	BZW04-14B	5	13.6	15.2	16	16.8	1	22.5	17.8	28.9	166	8.6	1100
P BZW04P15	P BZW04P15B	5	15.3	17.1	18	19.8	1	25.2	16	32.5	148	8.8	975
BZW04-15	BZW04-15B	5	15.3	17.1	18	18.9	1	25.2	16	32.5	148	8.8	975
BZW04P17	BZW04P17B	5	17.1	19	20	22	1	27.7	14.5	36.1	133	9.0	850
BZW04-17	BZW04-17B	5	17.1	19	20	21	1	27.7	14.5	36.1	133	9.0	850
BZW04P19	BZW04P19B	5	18.8	20.9	22	24.2	1	30.6	13	39.3	122	9.2	800
BZW04-19	BZW04-19B	5	18.8	20.9	22	23.1	1	30.6	13	39.3	122	9.2	800
BZW04P20	P BZW04P20B	5	20.5	22.8	24	26.4	1	33.2	12	42.8	112	9.4	725
BZW04-20	BZW04-20B	5	20.5	22.8	24	25.2	1	33.2	12	42.8	112	9.4	725
P BZW04P23	BZW04P23B	5	23.1	25.7	27	29.7	1	37.5	10.7	48.3	99	9.6	625
BZW04-23	BZW04-23B	5	23.1	25.7	27	28.4	1	37.5	10.7	48.3	99	9.6	625
P BZW04P26	P BZW04P26B	5	25.6	28.5	30	33	1	41.5	9.6	53.5	90	9.7	575
BZW04-26	BZW04-26B	5	25.6	28.5	30	31.5	1	41.5	9.6	53.5	90	9.7	575
BZW04P28	P BZW04P28B	5	28.2	31.4	33	36.3	1	45.7	8.8	59	81.5	9.8	510
BZW04-28	BZW04-28B	5	28.2	31.4	33	34.7	1	45.7	8.8	59	81.5	9.8	510
P BZW04P31	P BZW04P31B	5	30.8	34.2	36	39.6	1	49.9	8	64.3	74.5	9.9	480
BZW04-31	BZW04-31B	5	30.8	34.2	36	37.8	1	49.9	8	64.3	74.5	9.9	480
P BZW04P33	BZW04P33B	5	33.3	37.1	39	42.9	1	53.9	7.4	69.7	69	10.0	450

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

Types			I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirectional		Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
BZW04-33		BZW04-33B	5	33.3	37.1	39	41	1	53.9	7.4	69.7	69	10.0	450
BZW04P37	P	BZW04P37B	5	36.8	40.9	43	47.3	1	59.3	6.7	76.8	62.5	10.1	400
BZW04-37		BZW04-37B	5	36.8	40.9	43	45.2	1	59.3	6.7	76.8	62.5	10.1	400
BZW04P40		BZW04P40B	5	40.2	44.7	47	51.7	1	64.8	6.2	84	57	10.1	370
BZW04-40		BZW04-40B	5	40.2	44.7	47	49.4	1	64.8	6.2	84	57	10.1	370
BZW04P44		BZW04P44B	5	43.6	48.5	51	56.1	1	70.1	5.7	91	52.5	10.2	350
BZW04-44		BZW04-44B	5	43.6	48.5	51	53.6	1	70.1	5.7	91	52.5	10.2	350
BZW04P48		BZW04P48B	5	47.8	53.2	56	61.6	1	77	5.2	100	48	10.3	320
BZW04-48		BZW04-48B	5	47.8	53.2	56	58.8	1	77	5.2	100	48	10.3	320
BZW04P53		BZW04P53B	5	53	58.9	62	68.2	1	85	4.7	111	43	10.4	290
BZW04-53		BZW04-53B	5	53	58.9	62	65.1	1	85	4.7	111	43	10.4	290
BZW04P58		BZW04P58B	5	58.1	64.6	68	74.8	1	92	4.3	121	39.5	10.4	270
BZW04-58		BZW04-58B	5	58.1	64.6	68	71.4	1	92	4.3	121	39.5	10.4	270
BZW04P64		BZW04P64B	5	64.1	71.3	75	82.5	1	103	3.9	134	36	10.5	250
BZW04-64		BZW04-64B	5	64.1	71.3	75	78.8	1	103	3.9	134	36	10.5	250
BZW04P70	P	BZW04P70B	5	70.1	77.9	82	90.2	1	113	3.5	146	33	10.5	230
BZW04-70		BZW04-70B	5	70.1	77.9	82	86.1	1	113	3.5	146	33	10.5	230
BZW04P78		BZW04P78B	5	77.8	86.5	91	100	1	125	3.2	162	29.5	10.6	210
BZW04-78		BZW04-78B	5	77.8	86.5	91	95.5	1	125	3.2	162	29.5	10.6	210
P BZW04P85		BZW04P85B	5	85.5	95	100	110	1	137	2.9	178	27	10.6	200
BZW04-85		BZW04-85B	5	85.5	95	100	105	1	137	2.9	178	27	10.6	200
BZW04P94		BZW04P94B	5	94	105	110	121	1	152	2.6	195	24.5	10.7	185
BZW04-94		BZW04-94B	5	94	105	110	116	1	152	2.6	195	24.5	10.7	185
BZW04P102		BZW04P102B	5	102	114	120	132	1	165	2.4	212	22.5	10.7	170
BZW04-102		BZW04-102B	5	102	114	120	126	1	165	2.4	212	22.5	10.7	170
P BZW04P111		BZW04P111B	5	111	124	130	143	1	179	2.2	230	20.8	10.7	165
BZW04-111		BZW04-111B	5	111	124	130	137	1	179	2.2	230	20.8	10.7	165
P BZW04P128	P	BZW04P128B	5	128	143	150	165	1	207	2.0	265	18.1	10.8	145
BZW04-128		BZW04-128B	5	128	143	150	158	1	207	2.0	265	18.1	10.8	145
P BZW04P136	P	BZW04P136B	5	136	152	160	176	1	219	1.8	282	17	10.8	140
BZW04-136		BZW04-136B	5	136	152	160	168	1	219	1.8	282	17	10.8	140
P BZW04P145		BZW04P145B	5	145	161	170	187	1	234	1.7	301	16	10.8	135
BZW04-145		BZW04-145B	5	145	161	170	179	1	234	1.7	301	16	10.8	135
BZW04P154		BZW04P154B	5	154	171	180	198	1	246	1.6	317	15.1	10.8	125
BZW04-154		BZW04-154B	5	154	171	180	189	1	246	1.6	317	15.1	10.8	125
BZW04P171		BZW04P171B	5	171	190	200	220	1	274	1.5	353	13.6	10.8	120
BZW04-171		BZW04-171B	5	171	190	200	210	1	274	1.5	353	13.6	10.8	120
BZW04P188	P	BZW04P188B	5	188	209	220	242	1	301	1.4	388	12.4	10.8	110
BZW04-188		BZW04-188B	5	188	209	220	231	1	301	1.4	388	12.4	10.8	110
P BZW04P213		BZW04P213B	5	213	237	250	275	1	344	1.5	442	12	11	100
BZW04-213		BZW04-213B	5	213	237	250	263	1	344	1.5	442	12	11	100
P BZW04P239		BZW04P239B	5	239	266	280	308	1	384	1.5	494	12	11	95
BZW04-239		BZW04-239B	5	239	266	280	294	1	384	1.5	494	12	11	95
BZW04P256		BZW04P256B	5	256	285	300	330	1	414	1.2	529	10	11	90
BZW04-256		BZW04-256B	5	256	285	300	315	1	414	1.2	529	10	11	90
BZW04P273		BZW04P273B	5	273	304	320	352	1	438	1.2	564	10	11	85
BZW04-273		BZW04-273B	5	273	304	320	336	1	438	1.2	564	10	11	85
P BZW04P299		BZW04P299B	5	299	332	350	385	1	482	0.9	618	9	11	80
BZW04-299		BZW04-299B	5	299	332	350	368	1	482	0.9	618	9	11	80
BZW04P342		BZW04P342B	5	342	380	400	440	1	548	0.9	706	8	11	75
BZW04-342		BZW04-342B	5	342	380	400	420	1	548	0.9	706	8	11	75
BZW04P376		BZW04P376B	5	376	418	440	484	1	603	0.8	776	8	11	70
BZW04-376		BZW04-376B	5	376	418	440	462	1	603	0.8	776	8	11	70

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

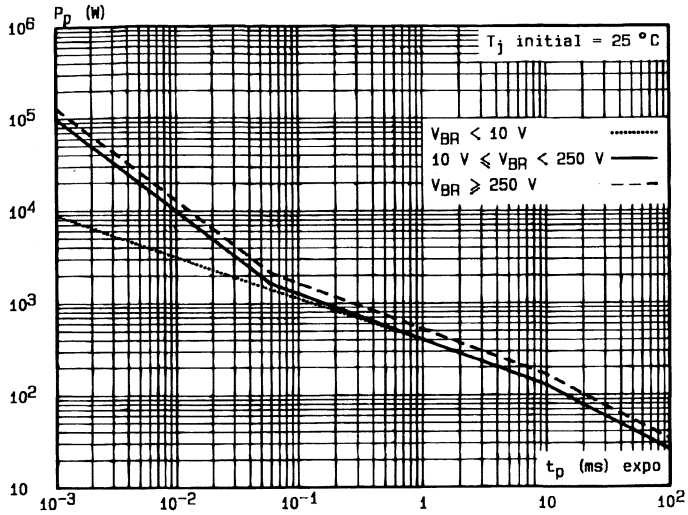


Fig.1 - Peak pulse power versus exponential pulse duration.

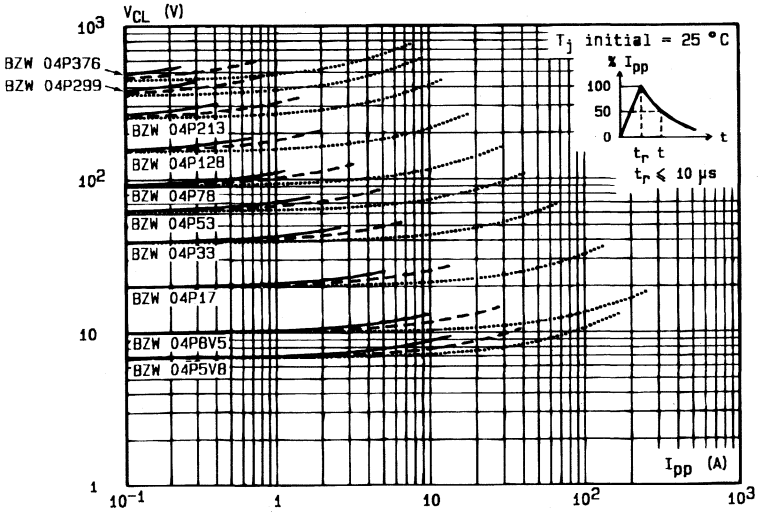


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

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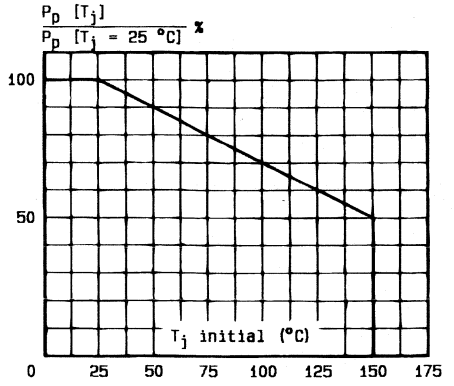


Fig.3 - Allowable power dissipation versus junction temperature.

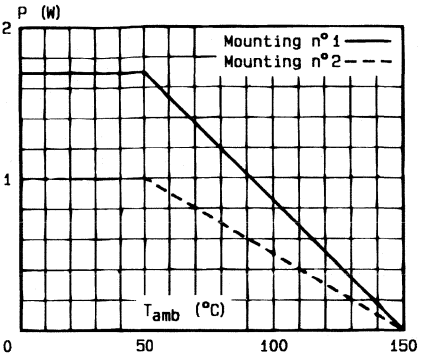


Fig.4 - Power dissipation versus ambient temperature.

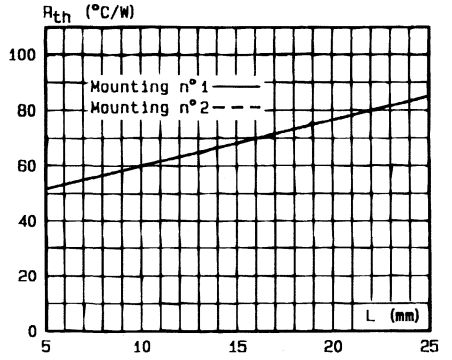
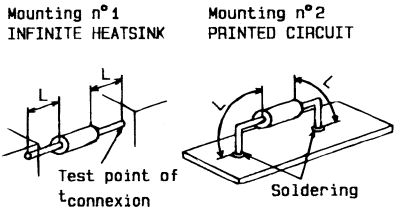


Fig.5 - Thermal resistance versus lead length.



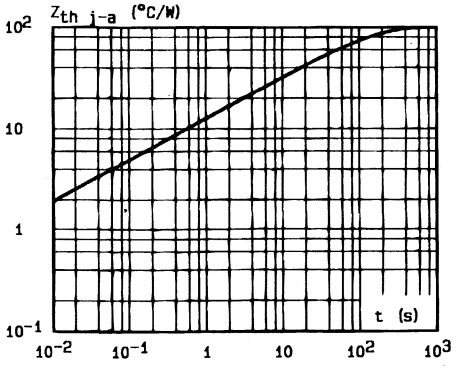


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

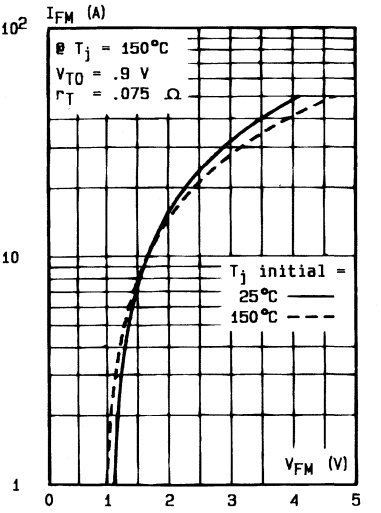


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

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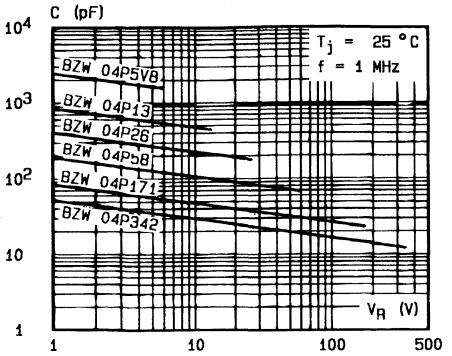

Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

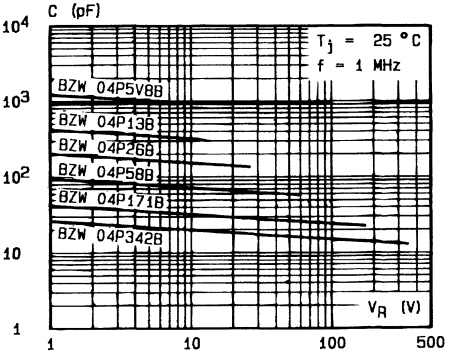

Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

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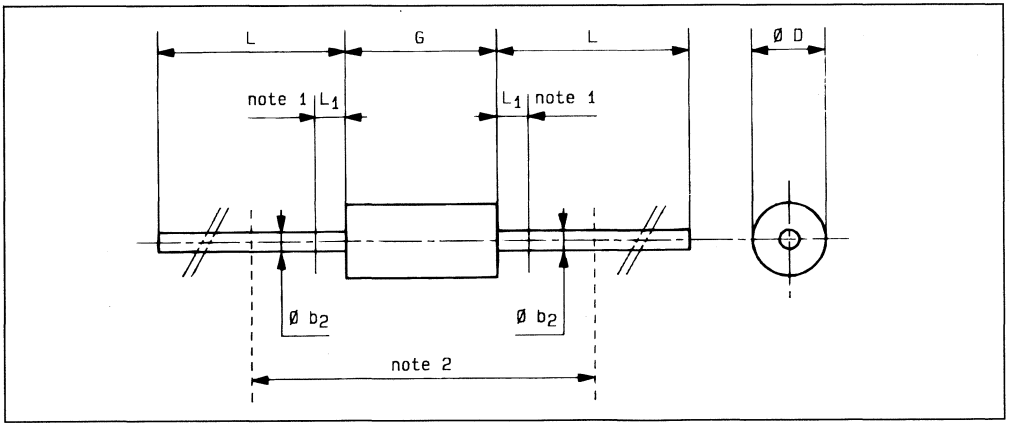
PACKAGE MECHANICAL DATA

F 126 Plastic



Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	0.76	0.86	0.029	0.034	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.59" (15 mm).
Ø D	2.95	3.05	0.116	0.120	
G	6.05	6.35	0.238	0.250	
L	26	–	1.024	–	
L_1	–	1.27	–	0.050	

Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 0.4 g.

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 600 W / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 5.8 V → 376 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES

CB-417
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

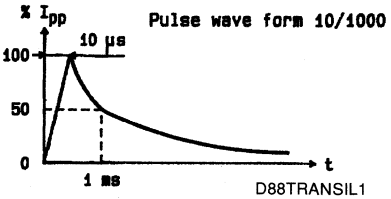
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	600	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 75 °C	5	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	100	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 55 to 175 175	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



D88TRANSIL1

ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.
V_{FM}	Forward Voltage Drop for Unidirectional Types (I_{FM} = 50 A)		3.5 V max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P P6KE6V8P	P P6KE6V8CP	1000§	5.8	6.45	6.8	7.48	10	10.5	57	13.4	261	5.7	4000
P6KE6V8A	P6KE6V8CA	1000§	5.8	6.45	6.8	7.14	10	10.5	57	13.4	261	5.7	4000
P P6KE7V5P	P P6KE7V5CP	500§	6.4	7.13	7.5	8.25	10	11.3	53	14.5	241	6.1	3700
P6KE7V5A	P6KE7V5CA	500§	6.4	7.13	7.5	7.88	10	11.3	53	14.5	241	6.1	3700
P P6KE8V2P	P6KE8V2CP	200§	7.02	7.79	8.2	9.02	10	12.1	50	15.5	226	6.5	3400
P6KE8V2A	P6KE8V2CA	200§	7.02	7.79	8.2	8.61	10	12.1	50	15.5	226	6.5	3400
P6KE9V1P	P6KE9V1CP	50§	7.78	8.65	9.1	10	1	13.4	45	17.1	205	6.8	3100
P6KE9V1A	P6KE9V1CA	50§	7.78	8.65	9.1	9.55	1	13.4	45	17.1	205	6.8	3100
P6KE10P	P6KE10CP	10§	8.55	9.5	10	11	1	14.5	41	18.6	387	7.3	2800
P6KE10A	P6KE10CA	10§	8.55	9.5	10	10.5	1	14.5	41	18.6	387	7.3	2800
P6KE11P	P6KE11CP	5§	9.4	10.5	11	12.1	1	15.6	38	20.3	355	7.5	2500
P6KE11A	P6KE11CA	5§	9.4	10.5	11	11.6	1	15.6	38	20.3	355	7.5	2500
P P6KE12P	P P6KE12CP	5	10.2	11.4	12	13.2	1	16.7	36	21.7	332	7.8	2300
P6KE12A	P6KE12CA	5	10.2	11.4	12	12.6	1	16.7	36	21.7	332	7.8	2300
P P6KE13P	P P6KE13CP	5	11.1	12.4	13	14.3	1	18.2	33	23.6	305	8.1	2150
P6KE13A	P6KE13CA	5	11.1	12.4	13	13.7	1	18.2	33	23.6	305	8.1	2150
P P6KE15P	P P6KE15CP	5	12.8	14.3	15	16.5	1	21.2	28	27.2	265	8.4	1900
P6KE15A	P6KE15CA	5	12.8	14.3	15	15.8	1	21.2	28	27.2	265	8.4	1900
P6KE16P	P6KE16CP	5	13.6	15.2	16	17.6	1	22.5	27	28.9	249	8.6	1800
P6KE16A	P6KE16CA	5	13.6	15.2	16	16.8	1	22.5	27	28.9	249	8.6	1800
P P6KE18P	P P6KE18CP	5	15.3	17.1	18	19.8	1	25.2	24	32.5	222	8.8	1600
P6KE18A	P6KE18CA	5	15.3	17.1	18	18.9	1	25.2	24	32.5	222	8.8	1600
P P6KE20P	P6KE20CP	5	17.1	19	20	22	1	27.7	22	36.1	199	9.0	1500
P6KE20A	P6KE20CA	5	17.1	19	20	21	1	27.7	22	36.1	199	9.0	1500
P6KE22P	P P6KE22CP	5	18.8	20.9	22	24.2	1	30.6	20	39.3	183	9.2	1350
P6KE22A	P6KE22CA	5	18.8	20.9	22	23.1	1	30.6	20	39.3	183	9.2	1350
P6KE24P	P6KE24CP	5	20.5	22.8	24	26.4	1	33.2	18	42.8	168	9.4	1250
P6KE24A	P6KE24CA	5	20.5	22.8	24	25.2	1	33.2	18	42.8	168	9.4	1250
P P6KE27P	P6KE27CP	5	23.1	25.7	27	29.7	1	37.5	16	48.3	149	9.6	1150
P6KE27A	P6KE27CA	5	23.1	25.7	27	28.4	1	37.5	16	48.3	149	9.6	1150
P P6KE30P	P6KE30CP	5	25.6	28.5	30	33	1	41.5	14.5	53.5	134	9.7	1075
P6KE30A	P6KE30CA	5	25.6	28.5	30	31.5	1	41.5	14.5	53.5	134	9.7	1075
P P6KE33P	P P6KE33CP	5	28.2	31.4	33	36.3	1	45.7	13.1	59	122	9.8	1000
P6KE33A	P6KE33CA	5	28.2	31.4	33	34.7	1	45.7	13.1	59	122	9.8	1000
P P6KE36P	P6KE36CP	5	30.8	34.2	36	39.6	1	49.9	12	64.3	112	9.9	950
P6KE36A	P6KE36CA	5	30.8	34.2	36	37.8	1	49.9	12	64.3	112	9.9	950

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types P6KE6V8CP → 11CA, IRM must be double that specified for unidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		V_{CL} @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ. V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P P6KE39P	P P6KE39CP	5	33.3	37.1	39	42.9	1	53.9	11.1	69.7	103	10.0	900
P6KE39A	P6KE39CA	5	33.3	37.1	39	41	1	53.9	11.1	69.7	103	10.0	900
P6KE43P	P6KE43CP	5	36.8	40.9	43	47.3	1	59.3	10.1	76.8	94	10.1	850
P6KE43A	P6KE43CA	5	36.8	40.9	43	45.2	1	59.3	10.1	76.8	94	10.1	850
P6KE47P	P P6KE47CP	5	40.2	44.7	47	51.7	1	64.8	9.3	84	86	10.1	800
P6KE47A	P6KE47CA	5	40.2	44.7	47	49.4	1	64.8	9.3	84	86	10.1	800
P P6KE51P	P6KE51CP	5	43.6	48.5	51	56.1	1	70.1	8.6	91	79	10.2	750
P6KE51A	P6KE51CA	5	43.6	48.5	51	53.6	1	70.1	8.6	91	79	10.2	750
P P6KE56P	P6KE56CP	5	47.8	53.2	56	61.6	1	77	7.8	100	72	10.3	700
P6KE56A	P6KE56CA	5	47.8	53.2	56	58.8	1	77	7.8	100	72	10.3	700
P6KE62P	P6KE62CP	5	53	58.9	62	68.2	1	85	7.1	111	65	10.4	650
P6KE62A	P6KE62CA	5	53	58.9	62	65.1	1	85	7.1	111	65	10.4	650
P P6KE68P	P6KE68CP	5	58.1	64.6	68	74.8	1	92	6.5	121	59.5	10.4	625
P6KE68A	P6KE68CA	5	58.1	64.6	68	71.4	1	92	6.5	121	59.5	10.4	625
P6KE75P	P6KE75CP	5	64.1	71.3	75	82.5	1	103	5.8	134	53.5	10.5	575
P6KE75A	P6KE75CA	5	64.1	71.3	75	78.8	1	103	5.8	134	53.5	10.5	575
P P6KE82P	P6KE82CP	5	70.1	77.9	82	90.2	1	113	5.3	146	49	10.5	550
P6KE82A	P6KE82CA	5	70.1	77.9	82	86.1	1	113	5.3	146	49	10.5	550
P6KE91P	P6KE91CP	5	77.8	86.5	91	100	1	125	4.8	162	44.5	10.6	525
P6KE91A	P6KE91CA	5	77.8	86.5	91	95.5	1	125	4.8	162	44.5	10.6	525
P6KE100P	P6KE100CP	5	85.5	95	100	110	1	137	4.4	178	40.5	10.6	500
P6KE100A	P6KE100CA	5	85.5	95	100	105	1	137	4.4	178	40.5	10.6	500
P6KE110P	P6KE110CP	5	94	105	110	121	1	152	3.9	195	37	10.7	470
P6KE110A	P6KE110CA	5	94	105	110	116	1	152	3.9	195	37	10.7	470
P6KE120P	P6KE120CP	5	102	114	120	132	1	165	3.6	212	34	10.7	450
P6KE120A	P6KE120CA	5	102	114	120	126	1	165	3.6	212	34	10.7	450
P P6KE130P	P6KE130CP	5	111	124	130	143	1	179	3.4	230	31.5	10.7	420
P6KE130A	P6KE130CA	5	111	124	130	137	1	179	3.4	230	31.5	10.7	420
P6KE150P	P6KE150CP	5	128	143	150	165	1	207	2.9	265	27.2	10.8	400
P6KE150A	P6KE150CA	5	128	143	150	158	1	207	2.9	265	27.2	10.8	400
P6KE160P	P P6KE160CP	5	136	152	160	176	1	219	2.7	282	25.5	10.8	380
P6KE160A	P6KE160CA	5	136	152	160	168	1	219	2.7	282	25.5	10.8	380
P6KE170P	P6KE170CP	5	145	161	170	187	1	234	2.6	301	24	10.8	370
P6KE170A	P6KE170CA	5	145	161	170	179	1	234	2.6	301	24	10.8	370
P P6KE180P	P6KE180CP	5	154	171	180	198	1	246	2.4	317	22.7	10.8	360
P6KE180A	P6KE180CA	5	154	171	180	189	1	246	2.4	317	22.7	10.8	360
P P6KE200P	P6KE200CP	5	171	190	200	220	1	274	2.2	353	20.4	10.8	350
P6KE200A	P6KE200CA	5	171	190	200	210	1	274	2.2	353	20.4	10.8	350
P6KE220P	P6KE220CP	5	188	209	220	242	1	301	2	388	18.6	10.8	330
P6KE220A	P6KE220CA	5	188	209	220	231	1	301	2	388	18.6	10.8	330
P P6KE250P	P6KE250CP	5	213	237	250	275	1	344	2	442	19	11	310
P6KE250A	P6KE250CA	5	213	237	250	263	1	344	2	442	19	11	310
P6KE280P	P6KE280CP	5	239	266	280	308	1	384	2	494	18	11	300
P6KE280A	P6KE280CA	5	239	266	280	294	1	384	2	494	18	11	300
P6KE300P	P6KE300CP	5	256	285	300	330	1	414	1.6	529	14	11	290
P6KE300A	P6KE300CA	5	256	285	300	315	1	414	1.6	529	14	11	290
P6KE320P	P6KE320CP	5	273	304	320	352	1	438	1.6	564	14	11	280
P6KE320A	P6KE320CA	5	273	304	320	336	1	438	1.6	564	14	11	280
P6KE350P	P6KE350CP	5	299	332	350	385	1	482	1.6	618	14	11	270
P6KE350A	P6KE350CA	5	299	332	350	368	1	482	1.6	618	14	11	270
P P6KE400P	P P6KE400CP	5	342	380	400	440	1	548	1.3	706	11	11	360
P6KE400A	P6KE400CA	5	342	380	400	420	1	548	1.3	706	11	11	360
P P6KE440P	P6KE440CP	5	376	418	440	484	1	603	1.3	776	11	11	350
P6KE440A	P6KE440CA	5	376	418	440	462	1	603	1.3	776	11	11	350

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

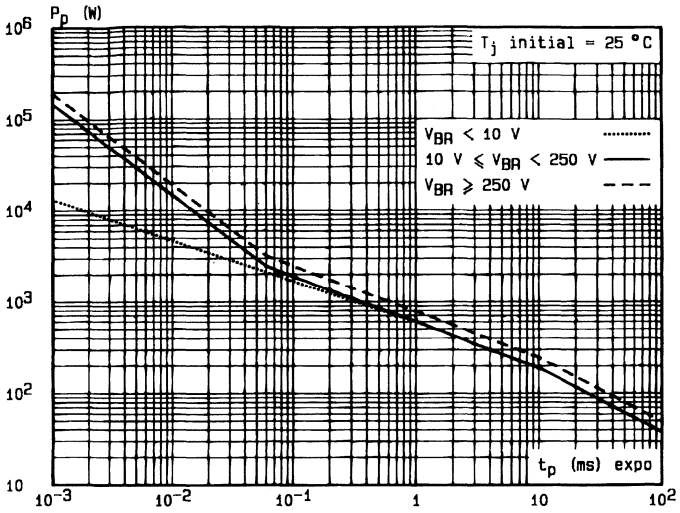


Fig.1 - Peak pulse power versus exponential pulse duration.

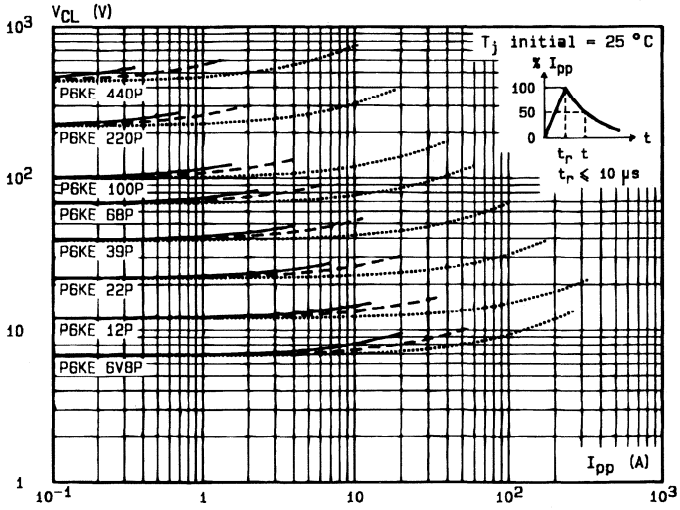


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D88P6KEP4

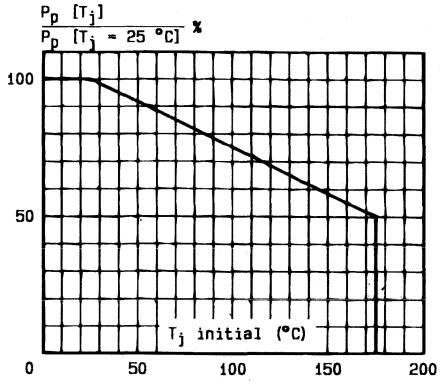


Fig.3 - Allowable power dissipation versus junction temperature.

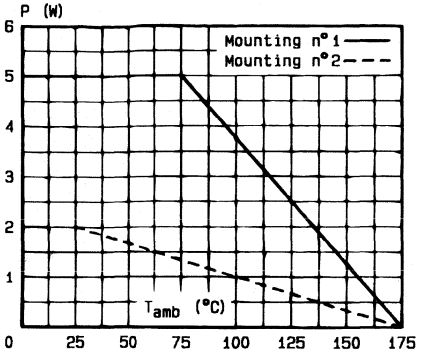


Fig.4 - Power dissipation versus ambient temperature.

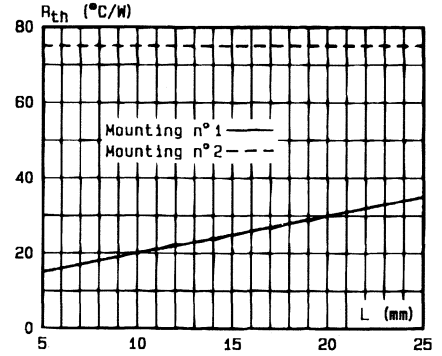
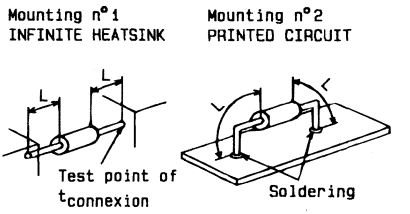


Fig.5 - Thermal resistance versus lead length.



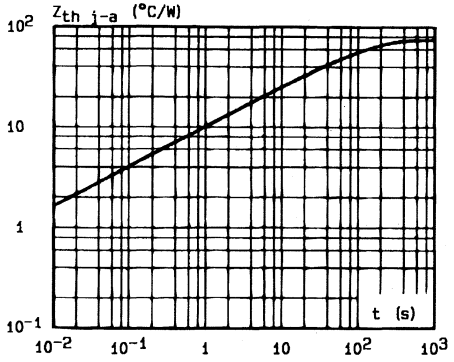


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

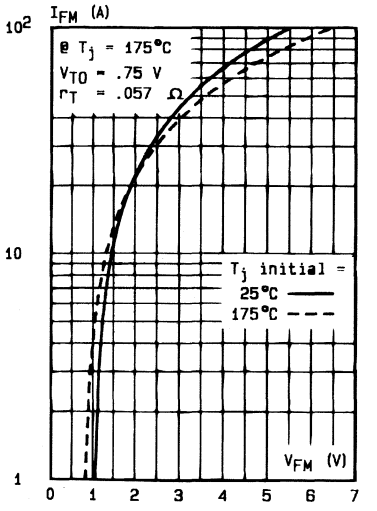


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88P6KEP5

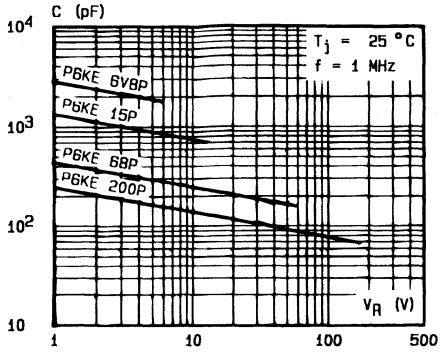


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

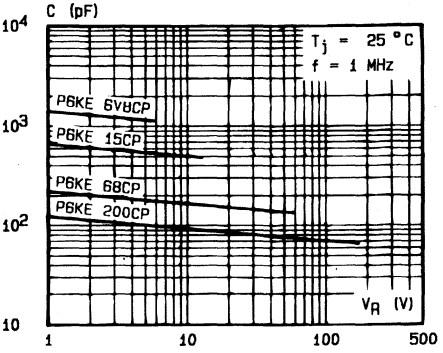
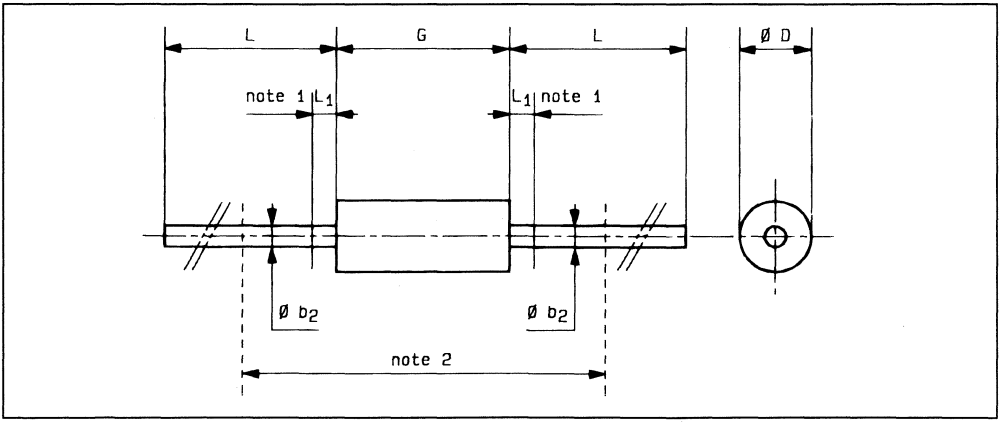


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88P6KEP6

PACKAGE MECHANICAL DATA

CB-417 Plastic



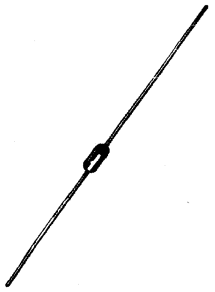
Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	–	1.092	–	0.043	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.59" (15 mm).
Ø D	–	3.683	–	0.145	
G	–	8.89	–	0.350	
L	25.4	–	1.000	–	
L_1	–	1.25	–	0.049	

Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 0.6 g.

SGS-THOMSON MICROELECTRONICS

PL360D

UNIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSOR



F126
(Plastic)

DESCRIPTION

Transient voltage suppressor diode especially designed for transistor protection in electronic ignition circuit.
Connected accross collector and base it avoids any transistor damage when spark plug is fouled or disconnected.

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_{tot}	DC Power Dissipation	T_{amb} = 50 °C	1.7	W
I_{ZM}	Continuous Reverse Current	T_{amb} = 50 °C	3.5	mA
P_{RSM}	Non Repetitive Surge Peak Power Dissipation	T_J Initial = 25 °C t = 1 ms	300	W
T_{oper}	Operating Temperature		– 55 to 150	°C
T_{stg} T_j	Storage and Junction Temperature Range		– 55 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 3 s at 5 mm from Case		300	°C

THERMAL RESISTANCE

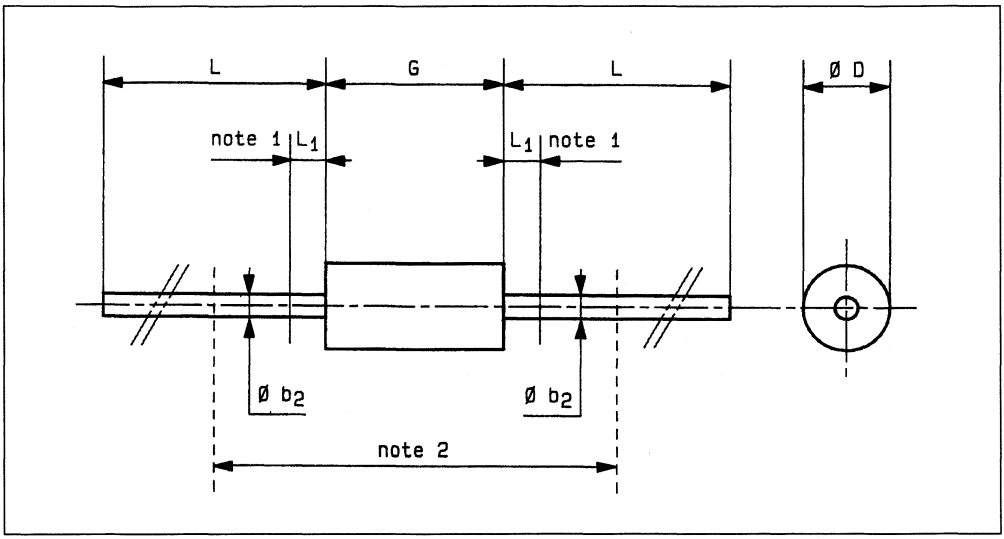
Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	60	°C/W

ELECTRICAL CHARACTERISTICS

Type	V_{BR} @ T_j = 25 °C min.	max.	V_{BR} @ T_j = 120 °C min.	max.	I_R	α_T typ.	I_{RM}/V_{RM} max.	V_{RM}	I_{ZM}
	(V)		(V)		(mA)	(10^{-4}/°C)	(µA)	(V)	(mA)
PL 360 D	330	370	358	416	2	11	0.35	270	3.5

PACKAGE MECHANICAL

F 126 Plastic



Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	0.76	0.86	0.029	0.034	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.59" (15 mm).
Ø D	2.95	3.05	0.116	0.120	
G	6.05	6.35	0.238	0.250	
L	26	–	1.024	–	
L_1	–	1.27	–	0.050	

Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode.
Weight : 0.4 g.

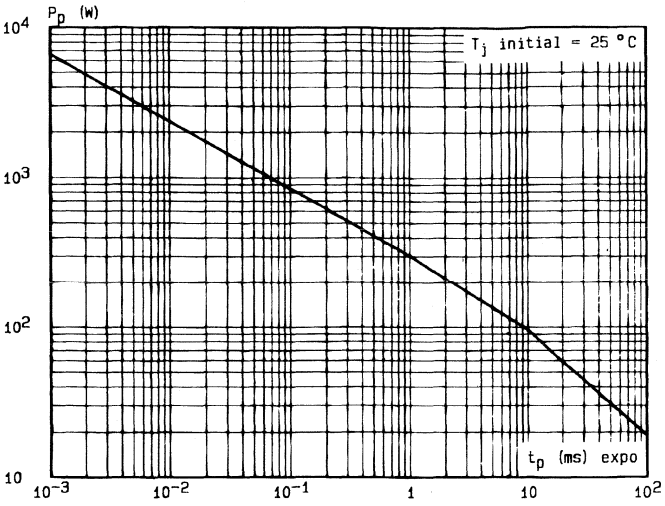


Fig.1 - Peak pulse power versus exponential pulse duration.

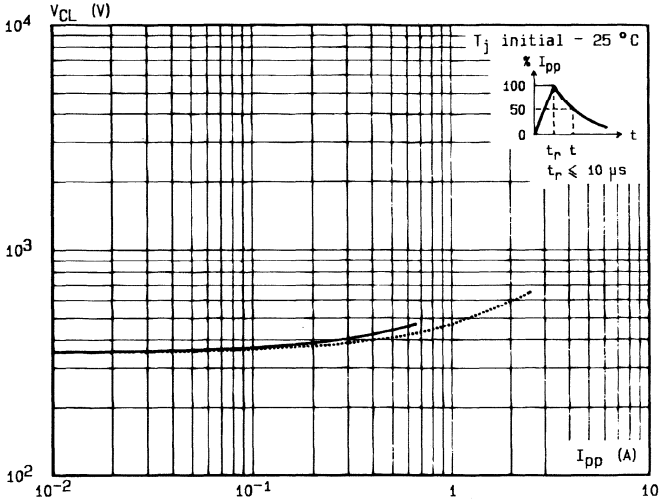


Fig.2 - Clamping voltage versus peak pulse current
exponential waveform t = 20 µs ·····
t = 1 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

DB9PL360DP3

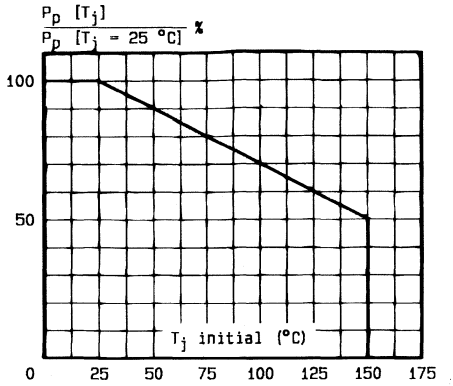


Fig.3 - Allowable power dissipation versus junction temperature.

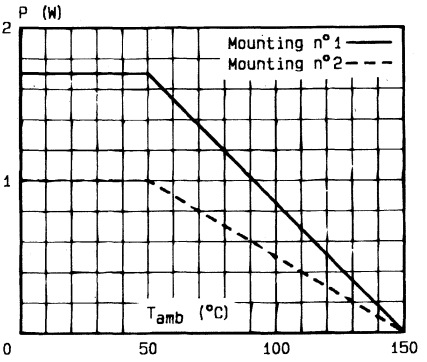


Fig.4 - Power dissipation versus ambient temperature.

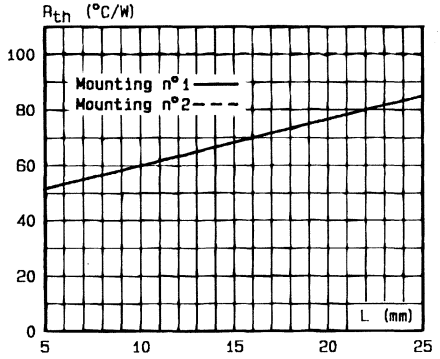
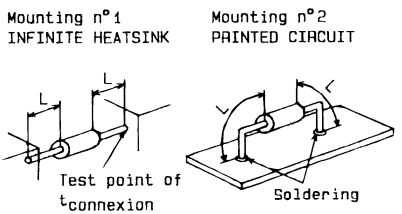


Fig.5 - Thermal resistance versus lead length.



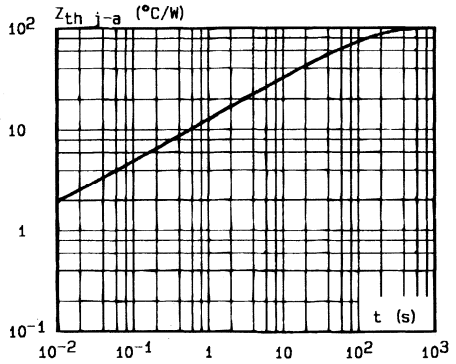


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

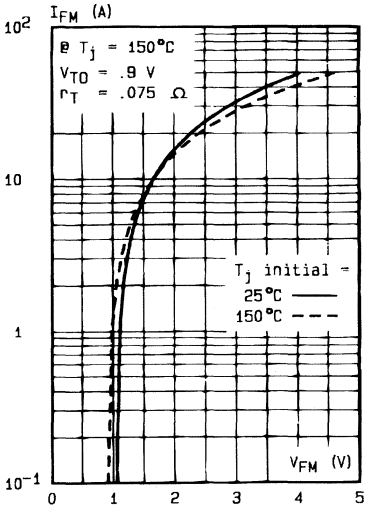


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

DB9PL360DP4

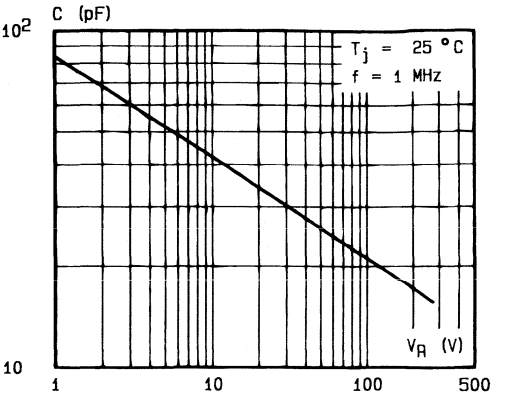


Fig.8 - Capacitance versus reverse aplied voltage (typical values).

D89PL360DP5

SGS-THOMSON MICROELECTRONICS

1.5KE6V8P,A → 440P,A
1.5KE6V8CP,CA → 440CP,CA

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 1.5 kW / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 5.8 V → 376 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES

CB-429
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

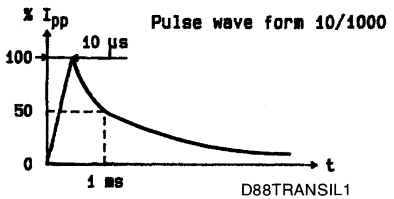
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	1.5	kW
P	Power Dissipation on Infinite Heatsink	T_{amb} = 75 °C	5	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	250	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 175 175	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ. V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P 1.5KE6V8P	P 1.5KE6V8CP	1000§	5.8	6.45	6.8	7.48	10	10.5	143	13.4	746	5.7	9500
1.5KE6V8A	1.5KE6V8CA	1000§	5.8	6.45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
P 1.5KE7V5P	1.5KE7V5CP	500§	6.4	7.13	7.5	8.25	10	11.3	132	14.5	690	6.1	8500
1.5KE7V5A	1.5KE7V5CA	500§	6.4	7.13	7.5	7.88	10	11.3	132	14.5	690	6.1	8500
1.5KE8V2P	1.5KE8V2CP	200§	7.02	7.79	8.2	9.02	10	12.1	124	15.5	645	6.5	8000
1.5KE8V2A	1.5KE8V2CA	200§	7.02	7.79	8.2	8.61	10	12.1	124	15.5	645	6.5	8000
1.5KE9V1P	1.5KE9V1CP	50§	7.78	8.65	9.1	10	1	13.4	112	17.1	585	6.8	7500
1.5KE9V1A	1.5KE9V1CA	50§	7.78	8.65	9.1	9.55	1	13.4	112	17.1	585	6.8	7500
P 1.5KE10P	1.5KE10CP	10§	8.55	9.5	10	11	1	14.5	103	18.6	968	7.3	7000
1.5KE10A	1.5KE10CA	10§	8.55	9.5	10	10.5	1	14.5	103	18.6	968	7.3	7000
1.5KE11P	1.5KE11CP	5§	9.4	10.5	11	12.1	1	15.6	96	20.3	887	7.5	6400
1.5KE11A	1.5KE11CA	5§	9.4	10.5	11	11.6	1	15.6	96	20.3	887	7.5	6400
P 1.5KE12P	P 1.5KE12CP	5	10.2	11.4	12	13.2	1	16.7	90	21.7	829	7.8	6000
1.5KE12A	1.5KE12CA	5	10.2	11.4	12	12.6	1	16.7	90	21.7	829	7.8	6000
P 1.5KE13P	1.5KE13CP	5	11.1	12.4	13	14.3	1	18.2	82	23.6	763	8.1	5500
1.5KE13A	1.5KE13CA	5	11.1	12.4	13	13.7	1	18.2	82	23.6	763	8.1	5500
1.5KE15P	1.5KE15CP	5	12.8	14.3	15	16.5	1	21.2	71	27.2	662	8.4	5000
1.5KE15A	1.5KE15CA	5	12.8	14.3	15	15.8	1	21.2	71	27.2	662	8.4	5000
P 1.5KE16P	1.5KE16CP	5	13.6	15.2	16	17.6	1	22.5	67	28.9	623	8.6	4700
1.5KE16A	1.5KE16CA	5	13.6	15.2	16	16.8	1	22.5	67	28.9	623	8.6	4700
P 1.5KE18P	P 1.5KE18CP	5	15.3	17.1	18	19.8	1	25.2	59.5	32.5	554	8.8	4300
1.5KE18A	1.5KE18CA	5	15.3	17.1	18	18.9	1	25.2	59.5	32.5	554	8.8	4300
P 1.5KE20P	P 1.5KE20CP	5	17.1	19	20	22	1	27.7	54	36.1	498	9.0	4000
1.5KE20A	1.5KE20CA	5	17.1	19	20	21	1	27.7	54	36.1	498	9.0	4000
P 1.5KE22P	1.5KE22CP	5	18.8	20.9	22	24.2	1	30.6	49	39.3	458	9.2	3700
1.5KE22A	1.5KE22CA	5	18.8	20.9	22	23.1	1	30.6	49	39.3	458	9.2	3700
1.5KE24P	1.5KE24CP	5	20.5	22.8	24	26.4	1	33.2	45	42.8	421	9.4	3500
1.5KE24A	1.5KE24CA	5	20.5	22.8	24	25.2	1	33.2	45	42.8	421	9.4	3500
P 1.5KE27P	1.5KE27CP	5	23.1	25.7	27	29.7	1	37.5	40	48.3	373	9.6	3200
1.5KE27A	1.5KE27CA	5	23.1	25.7	27	28.4	1	37.5	40	48.3	373	9.6	3200
P 1.5KE30P	P 1.5KE30CP	5	25.6	28.5	30	33	1	41.5	36	53.5	336	9.7	2900
1.5KE30A	1.5KE30CA	5	25.6	28.5	30	31.5	1	41.5	36	53.5	336	9.7	2900
P 1.5KE33P	P 1.5KE33CP	5	28.2	31.4	33	36.3	1	45.7	33	59	305	9.8	2700
1.5KE33A	1.5KE33CA	5	28.2	31.4	33	34.7	1	45.7	33	59	305	9.8	2700
P 1.5KE36P	P 1.5KE36CP	5	30.8	34.2	36	39.6	1	49.9	30	64.3	280	9.9	2500
1.5KE36A	1.5KE36CA	5	30.8	34.2	36	37.8	1	49.9	30	64.3	280	9.9	2500
P 1.5KE39P	P 1.5KE39CP	5	33.3	37.1	39	42.9	1	53.9	28	69.7	258	10.0	2400

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.

** Divide these values by 2 for bidirectional types.

§ For bidirectional types 1.5KE6V8CP → 11CA, I_{RM} must be double that specified for unidirectional types.

For bidirectional types, electrical characteristics apply in both directions.

P : Preferred device.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
1.5KE39A	1.5KE39CA	5	33.3	37.1	39	41	1	53.9	28	69.7	258	10.0	2400
P 1.5KE43P	1.5KE43CP	5	36.8	40.9	43	47.3	1	59.3	25.3	76.8	234	10.1	2200
1.5KE43A	1.5KE43CA	5	36.8	40.9	43	45.2	1	59.3	25.3	76.8	234	10.1	2200
P 1.5KE47P	P 1.5KE47CP	5	40.2	44.7	47	51.7	1	64.8	23.2	84	214	10.1	2050
1.5KE47A	1.5KE47CA	5	40.2	44.7	47	49.4	1	64.8	23.2	84	214	10.1	2050
P 1.5KE51P	1.5KE51CP	5	43.6	48.5	51	56.1	1	70.1	21.4	91	198	10.2	1950
1.5KE51A	1.5KE51CA	5	43.6	48.5	51	53.6	1	70.1	21.4	91	198	10.2	1950
1.5KE56P	1.5KE56CP	5	47.8	53.2	56	61.6	1	77	19.5	100	180	10.3	1800
1.5KE56A	1.5KE56CA	5	47.8	53.2	56	58.8	1	77	19.5	100	180	10.3	1800
1.5KE62P	1.5KE62CP	5	53	58.9	62	68.2	1	85	17.7	111	162	10.4	1700
1.5KE62A	1.5KE62CA	5	53	58.9	62	65.1	1	85	17.7	111	162	10.4	1700
P 1.5KE68P	P 1.5KE68CP	5	58.1	64.6	68	74.8	1	92	16.3	121	148	10.4	1550
1.5KE68A	1.5KE68CA	5	58.1	64.6	68	71.4	1	92	16.3	121	148	10.4	1550
1.5KE75P	1.5KE75CP	5	64.1	71.3	75	82.5	1	103	14.6	134	134	10.5	1450
1.5KE75A	1.5KE75CA	5	64.1	71.3	75	78.8	1	103	14.6	134	134	10.5	1450
P 1.5KE82P	P 1.5KE82CP	5	70.1	77.9	82	90.2	1	113	13.3	146	123	10.5	1350
1.5KE82A	1.5KE82CA	5	70.1	77.9	82	86.1	1	113	13.3	146	123	10.5	1350
1.5KE91P	1.5KE91CP	5	77.8	86.5	91	100	1	125	12	162	111	10.6	1250
1.5KE91A	1.5KE91CA	5	77.8	86.5	91	95.5	1	125	12	162	111	10.6	1250
1.5KE100P	1.5KE100CP	5	85.5	95	100	110	1	137	11	178	101	10.6	1150
1.5KE100A	1.5KE100CA	5	85.5	95	100	105	1	137	11	178	101	10.6	1150
1.5KE110P	P 1.5KE110CP	5	94	105	110	121	1	152	9.9	195	92	10.7	1050
1.5KE110A	1.5KE110CA	5	94	105	110	116	1	152	9.9	195	92	10.7	1050
1.5KE120P	1.5KE120CP	5	102	114	120	132	1	165	9.1	212	85	10.7	1000
1.5KE120A	1.5KE120CA	5	102	114	120	126	1	165	9.1	212	85	10.7	1000
1.5KE130P	P 1.5KE130CP	5	111	124	130	143	1	179	8.4	230	78	10.7	950
1.5KE130A	1.5KE130CA	5	111	124	130	137	1	179	8.4	230	78	10.7	950
1.5KE150P	1.5KE150CP	5	128	143	150	165	1	207	7.2	265	68	10.8	850
1.5KE150A	1.5KE150CA	5	128	143	150	158	1	207	7.2	265	68	10.8	850
1.5KE160P	1.5KE160CP	5	136	152	160	176	1	219	6.8	282	64	10.8	800
1.5KE160A	1.5KE160CA	5	136	152	160	168	1	219	6.8	282	64	10.8	800
P 1.5KE170P	1.5KE170CP	5	145	161	170	187	1	234	6.4	301	60	10.8	750
1.5KE170A	1.5KE170CA	5	145	161	170	179	1	234	6.4	301	60	10.8	750
P 1.5KE180P	P 1.5KE180CP	5	154	171	180	198	1	246	6.1	317	57	10.8	725
1.5KE180A	1.5KE180CA	5	154	171	180	189	1	246	6.1	317	57	10.8	725
P 1.5KE200P	P 1.5KE200CP	5	171	190	200	220	1	274	5.5	353	51	10.8	675
1.5KE200A	1.5KE200CA	5	171	190	200	210	1	274	5.5	353	51	10.8	675
1.5KE220P	P 1.5KE220CP	5	188	209	220	242	1	328	4.6	388	46.5	10.8	625
1.5KE220A	1.5KE220CA	5	188	209	220	231	1	328	4.6	388	46.5	10.8	625
P 1.5KE250P	P 1.5KE250CP	5	213	237	250	275	1	344	5.0	442	47	11	560
1.5KE250A	1.5KE250CA	5	213	237	250	263	1	344	5.0	442	47	11	560
1.5KE280P	1.5KE280CP	5	239	266	280	308	1	384	5.0	494	47	11	520
1.5KE280A	1.5KE280CA	5	239	266	280	294	1	384	5.0	494	47	11	520
P 1.5KE300P	P 1.5KE300CP	5	256	285	300	330	1	414	5.0	529	47	11	500
1.5KE300A	1.5KE300CA	5	256	285	300	315	1	414	5.0	529	47	11	500
1.5KE320P	1.5KE320CP	5	273	304	320	352	1	438	4.5	564	42	11	460
1.5KE320A	1.5KE320CA	5	273	304	320	336	1	438	4.5	564	42	11	460
P 1.5KE350P	P 1.5KE350CP	5	299	332	350	385	1	482	4.0	618	37	11	430
1.5KE350A	1.5KE350CA	5	299	332	350	368	1	482	4.0	618	37	11	430
P 1.5KE400P	P 1.5KE400CP	5	342	380	400	440	1	548	4.0	706	37	11	390
1.5KE400A	1.5KE400CA	5	342	380	400	420	1	548	4.0	706	37	11	390
P 1.5KE440P	P 1.5KE440CP	5	376	418	440	484	1	603	3.5	776	33	11	360
1.5KE440A	1.5KE440CA	5	376	418	440	462	1	603	3.5	776	33	11	360

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

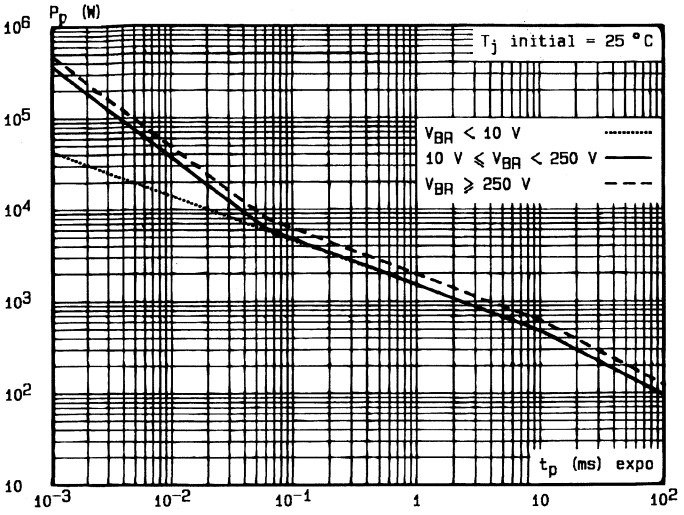


Fig.1 - Peak pulse power versus exponential pulse duration.

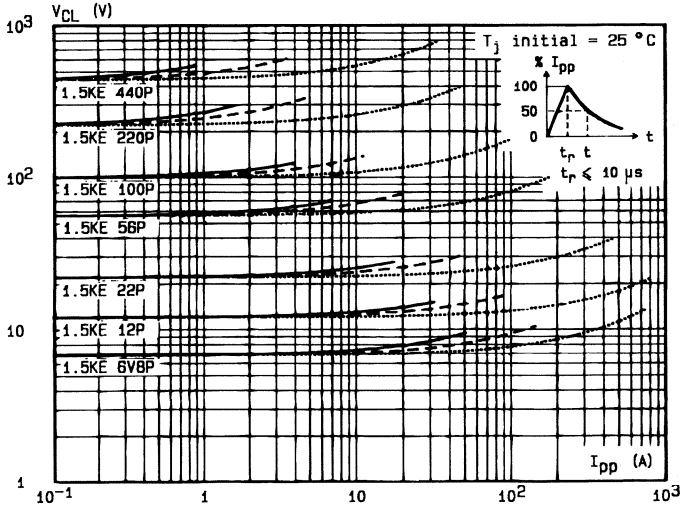


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D881.5KEP4

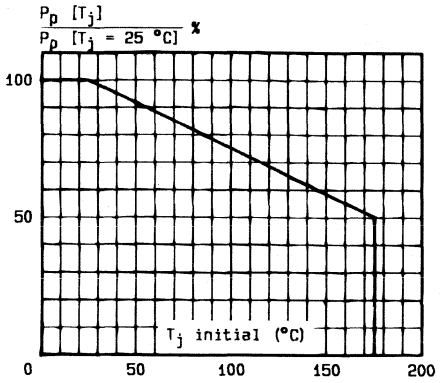


Fig.3 - Allowable power dissipation versus junction temperature.

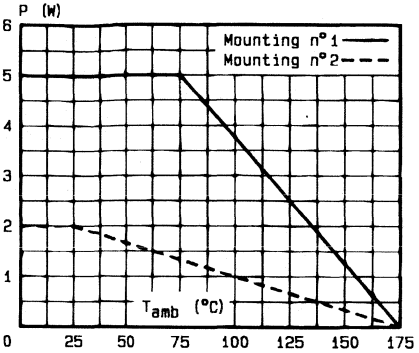


Fig.4 - Power dissipation versus ambient temperature.

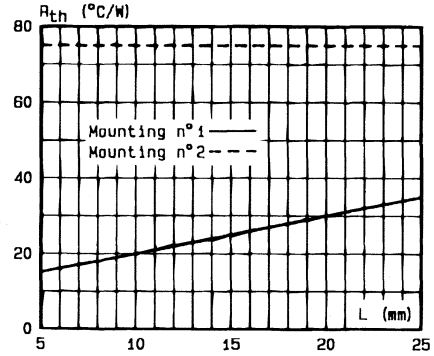
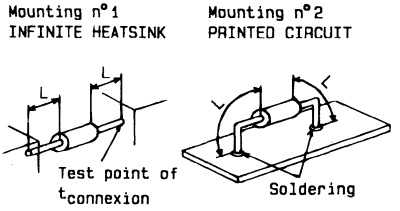


Fig.5 - Thermal resistance versus lead length.



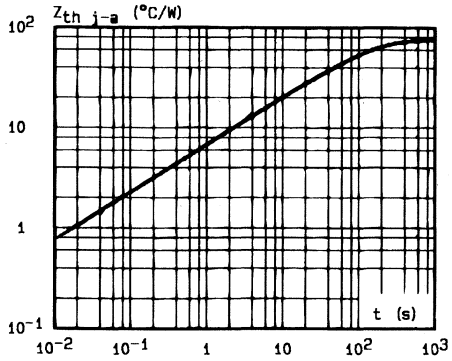


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

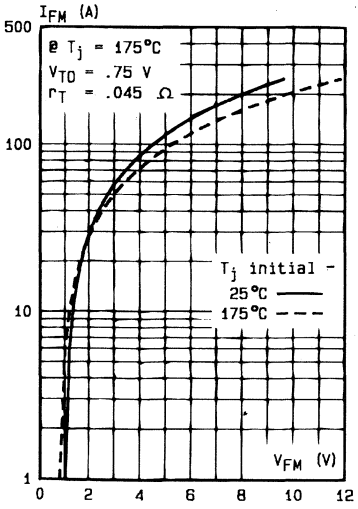


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D881.5KEP5

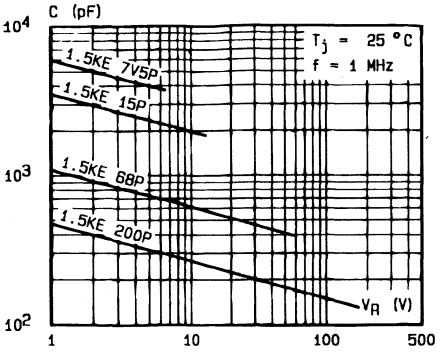


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

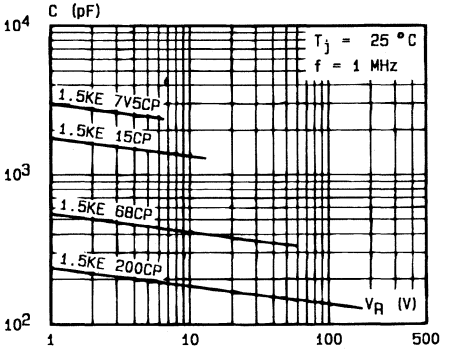
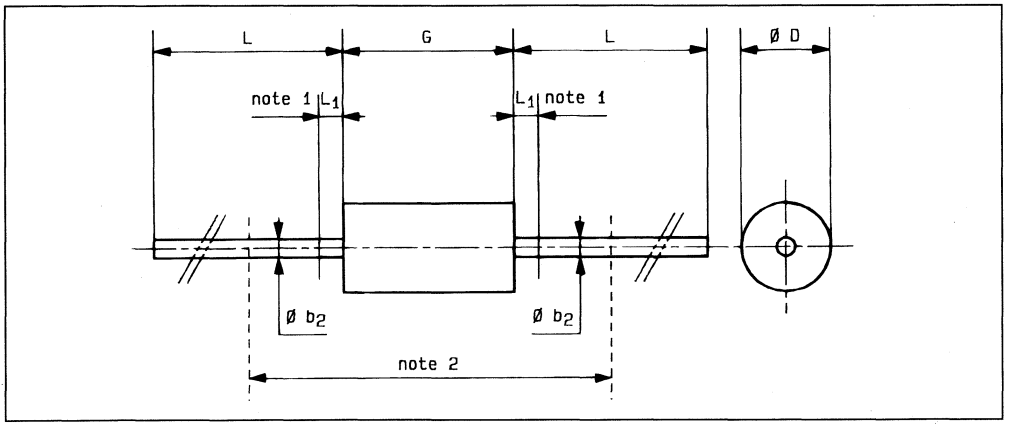


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D881.5KEP6

PACKAGE MECHANICAL DATA

CB-429 Plastic



Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	–	1.06	–	0.042	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.70" (18 mm).
Ø D	–	5.1	–	0.20	
G	–	9.8	–	0.386	
L	26	–	1.024	–	
L_1	–	1.27	–	0.050	

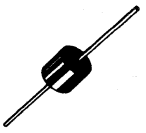
Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 0.9 g.

SGS-THOMSON MICROELECTRONICS

BZW50-10,B → 180, B

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 5 kW / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 10 V → 180 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX B FOR BIDIRECTIONAL TYPES



AG
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

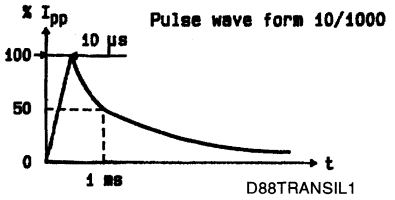
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	5	kW
P	Power Dissipation on Infinite Heatsink	T_{amb} = 75 °C	5	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	500	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	15	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



D88TRANSIL1

ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ. V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
BZW50-10	BZW50-10B	5	10	11.1	12.4	13.6	1	18.8	266	23.4	2564	7.8	24000
BZW50-12	BZW50-12B	5	12	13.3	14.8	16.3	1	22	227	28	2143	8.4	18500
BZW50-15	BZW50-15B	5	15	16.6	18.5	20.4	1	26.9	186	35	1714	8.8	13500
BZW50-18	BZW50-18B	5	18	20	22.2	24.4	1	32.2	155	41.5	1446	9.2	11500
BZW50-22	BZW50-22B	5	22	24.4	27.1	29.8	1	39.4	127	51	1177	9.6	8500
BZW50-27	BZW50-27B	5	27	30	33.3	36.6	1	48.3	103	62	968	9.8	7000
BZW50-33	BZW50-33B	5	33	36.6	40.7	44.7	1	59	85	76	789	10	5750
BZW50-39	BZW50-39B	5	39	43.3	48.1	53	1	69.4	72	90	667	10.1	4800
BZW50-47	BZW50-47B	5	47	52	57.8	63.6	1	83.2	60.1	108	556	10.3	4100
BZW50-56	BZW50-56B	5	56	62.2	69.1	76	1	99.6	50	129	465	10.4	3400
BZW50-68	BZW50-68B	5	68	75.6	84	92.4	1	121	41	157	382	10.5	3000
BZW50-82	BZW50-82B	5	82	91	101.2	111	1	145	34	189	317	10.6	2600
BZW50-100	BZW50-100B	5	100	111	123.5	136	1	179	28	228	263	10.7	2300
BZW50-120	BZW50-120B	5	120	133	148.1	163	1	215	23	274	219	10.8	1900
BZW50-150	BZW50-150B	5	150	166	185.2	204	1	269	19	343	175	10.8	1700
BZW50-180	BZW50-180B	5	180	200	222	244	1	322	16	410	146	10.8	1500

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.

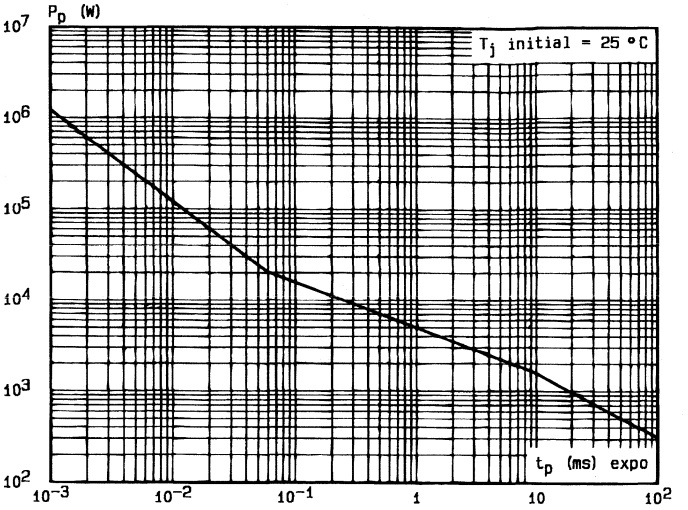


Fig.1 - Peak pulse power versus exponential pulse duration.

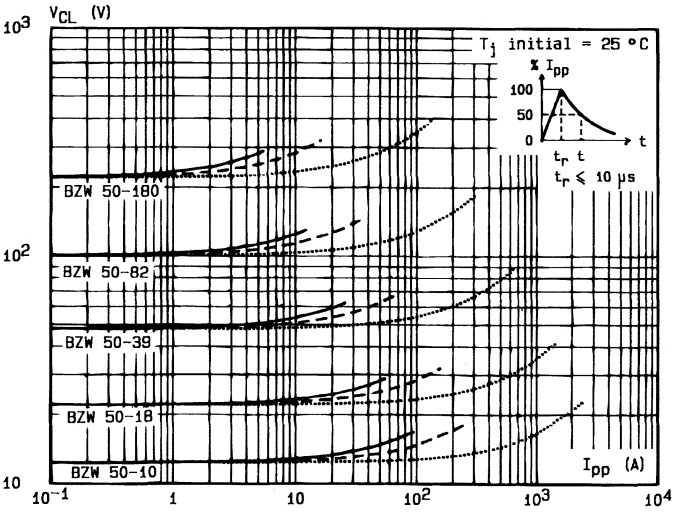


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·
t = 1 ms - - - -
t = 10 ms ———

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

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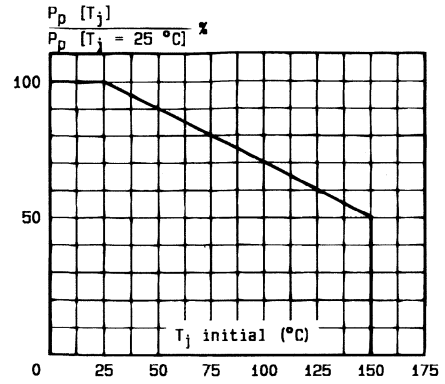


Fig.3 - Allowable power dissipation versus junction temperature.

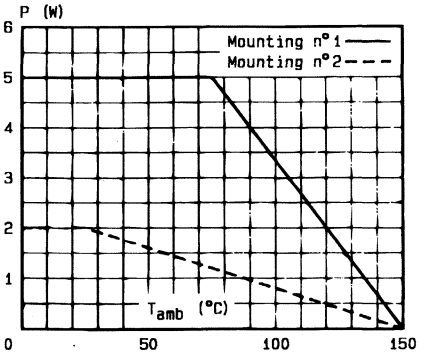


Fig.4 - Power dissipation versus ambient temperature.

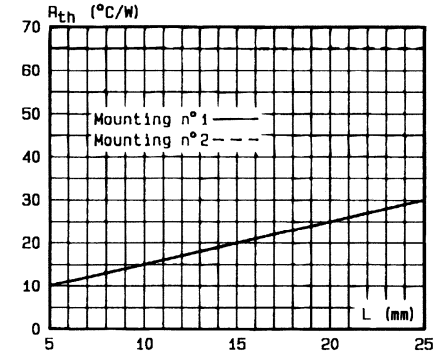
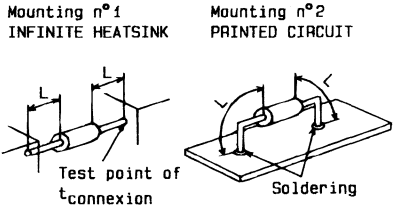


Fig.5 - Thermal resistance versus lead length.



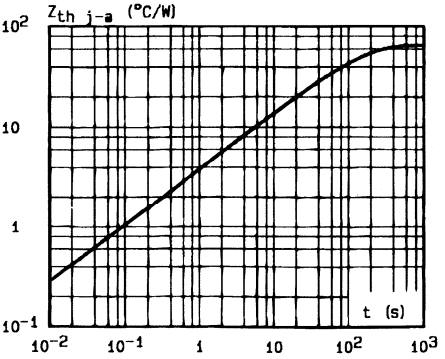


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

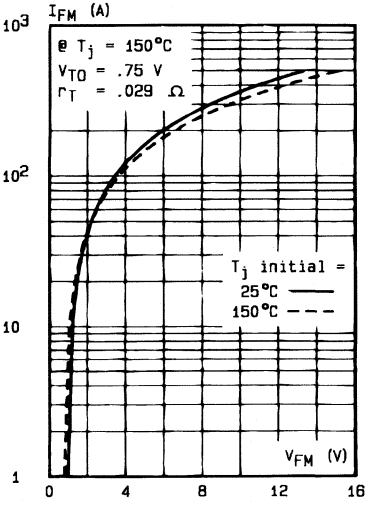


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88BZW50P4

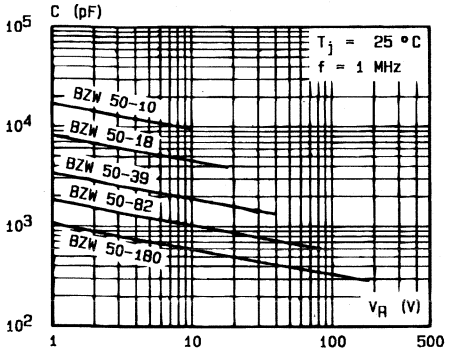


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

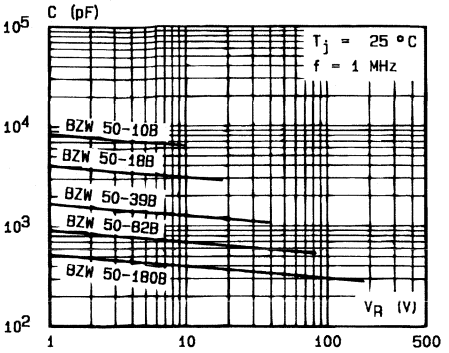
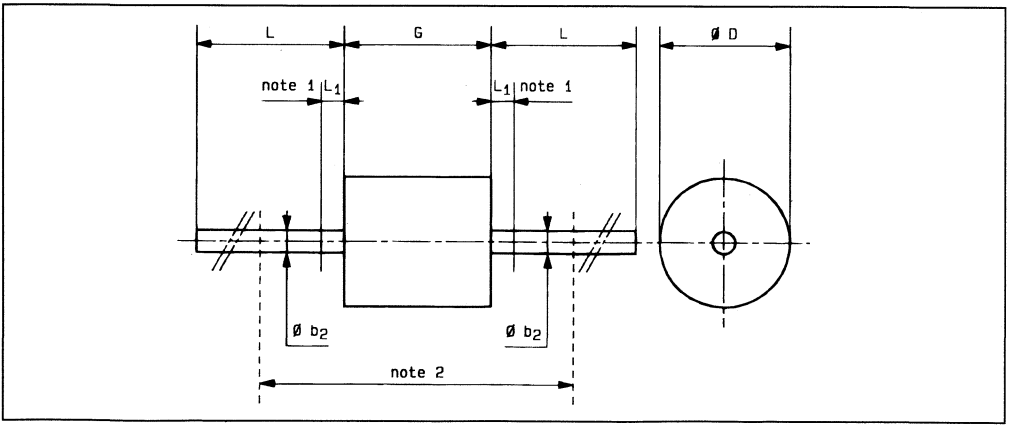


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88BZW50P5

PACKAGE MECHANICAL DATA

AG Plastic



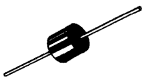
Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	1.35	1.45	0.053	0.057	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.79" (20 mm).
Ø D	–	8	–	0.315	
G	–	9	–	0.354	
L	20	–	0.787	–	
L_1	–	1.27	–	0.050	

Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 1 g.

BZW 100-20
BZW 100-24

UNIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY :
  1.8 kW / 15 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps



AG
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially designed for load dump effect protection.

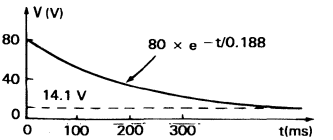
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 15 ms Exponential Pulse	T_j Initial = 25 °C See note 1	1800	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 75 °C	5	W
I_{FSM}	Non Repetitive Surge Peak Forward Current	T_j Initial = 25 °C t = 10 ms	200	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	15	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



LOAD DUMP TRANSIENT (standard SAE J1113A).

D88TRANSIL2

ELECTRICAL CHARACTERISTICS (T_j = 25°C)

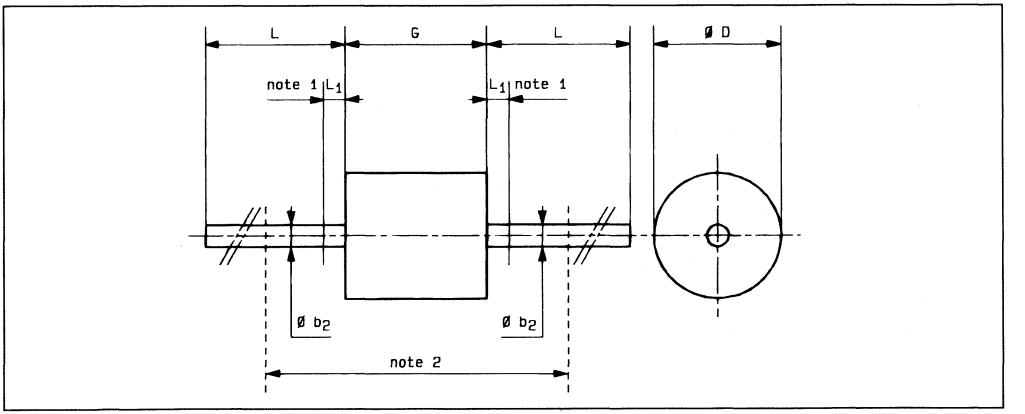
Symbol	Parameter	Value
V_{RM}	Stand-off Voltage	See table
$V_{(BR)}$	Breakdown Voltage	
$V_{(CL)}$	Clamping Voltage	
I_{pp}	Peak Pulse Current	
α_T	Temperature Coefficient of $V_{(BR)}$	
C	Capacitance	
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	1 ps max.
V_F	Peak Forward Voltage Drop (I_{FM} = 10 A)	1.9 V max.

Unidirectional Types	I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)		V_{CL} @ I_{pp} max. 15 ms expo.		α_T max.	C typ. V_R = 0 f = 1 MHz
	(μA)	(V)	min.	(mA)	(V)	(A)	(10^{-4}/°C)	(pF)
BZW100-20	50	20	24	1	36	50	9.6	4250
BZW100-24	50	24	29	1	40	45	9.8	3500

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.

PACKAGE MECHANICAL DATA

AG Plastic



Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	1.35	1.45	0.053	0.057	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.79" (20 mm).
Ø D	–	8	–	0.315	
G	–	9	–	0.354	
L	20	–	0.787	–	
L_1	–	1.27	–	0.050	

Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode.
Weight : 1 g.

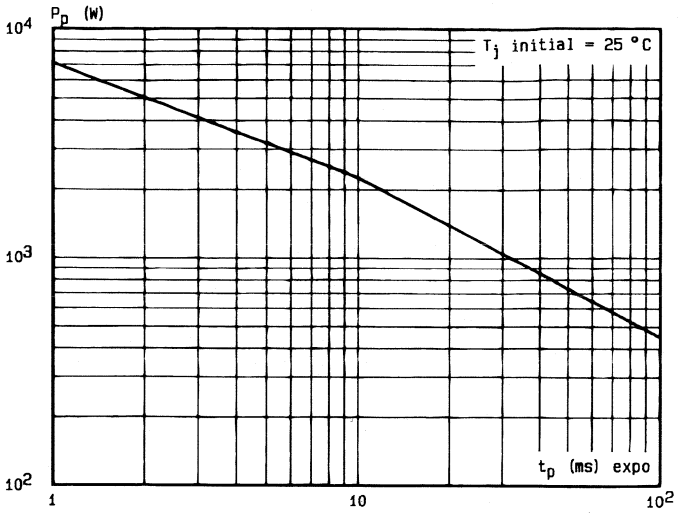


Fig.1 - Peak pulse power versus exponential pulse duration.

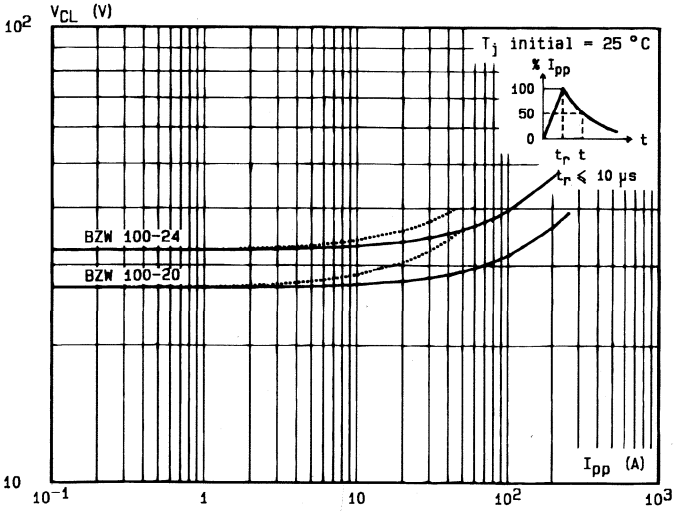


Fig.2 - Clamping voltage versus peak pulse current
exponential waveform t = 15 ms ·····
t = 1 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

DB8BZW100P3

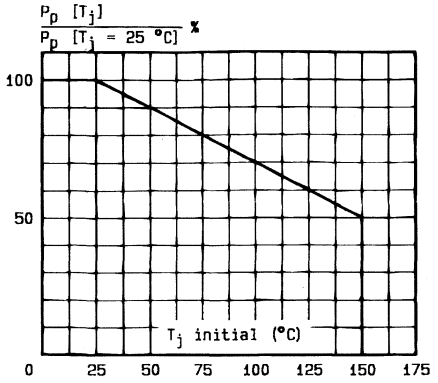


Fig.3 - Allowable power dissipation versus junction temperature.

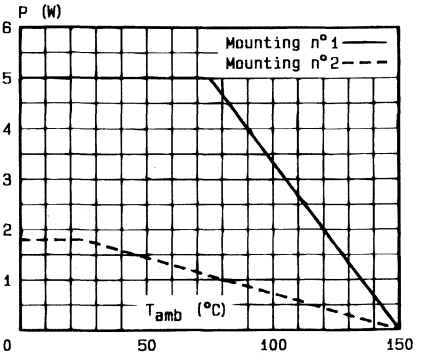


Fig.4 - Power dissipation versus ambient temperature.

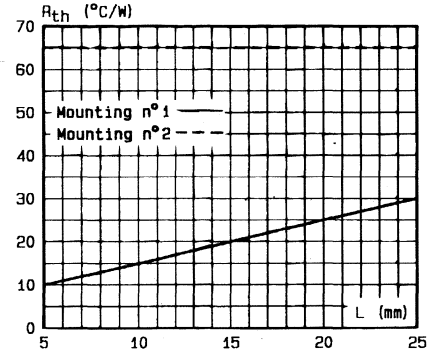
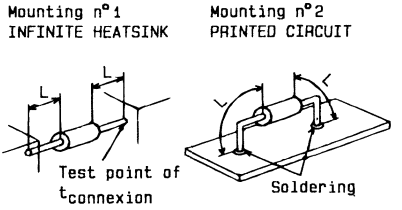


Fig.5 - Thermal resistance versus lead length.



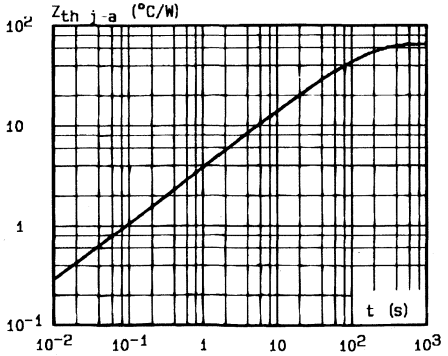


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

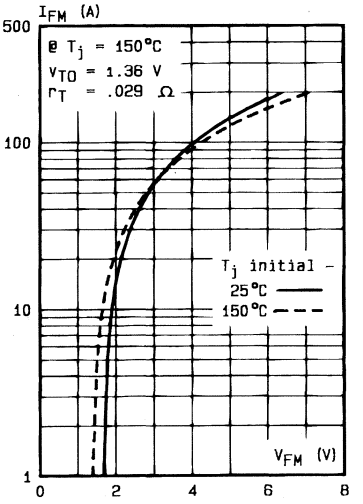


Fig.7 - Peak forward current versus peak forward voltage drop (maximum values).

DBBBZW100P4

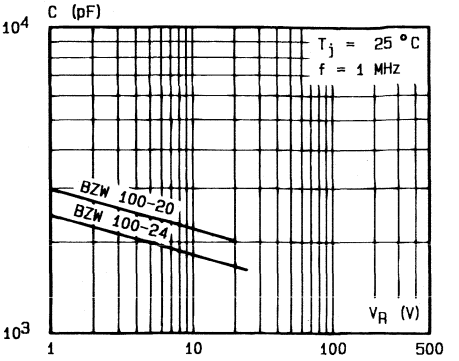


Fig.8 - Capacitance versus reverse aplied voltage (typical values).

D88BZW100P5

SGS-THOMSON MICROELECTRONICS

SM4T6V8, A → 220, A
SM4T6V8C, A → 200C, A

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 400 W / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 5.5 V → 188 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES

SOD 6
(Plastic)

SURFACE MOUNT TRANSIL FEATURES

- A PERFECT PICK AND PLACE BEHAVIOUR
- AN EXCELLENT ON BOARD STABILITY
- A FULL COMPATIBILITY WITH BOTH GLUING AND PASTE SOLDERING TECHNOLOGIES
- BODY MARKED WITH TYPE CODE AND LOGO
- STANDARD PACKAGING : 12 mm TAPE (EIA STD. RS481)
- TINNED COPPER LEADS
- HIGH TEMPERATURE RESISTANT RESIN

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

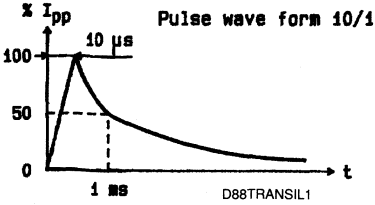
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	400	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 25 °C	1.2	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	50	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 175 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s		260	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



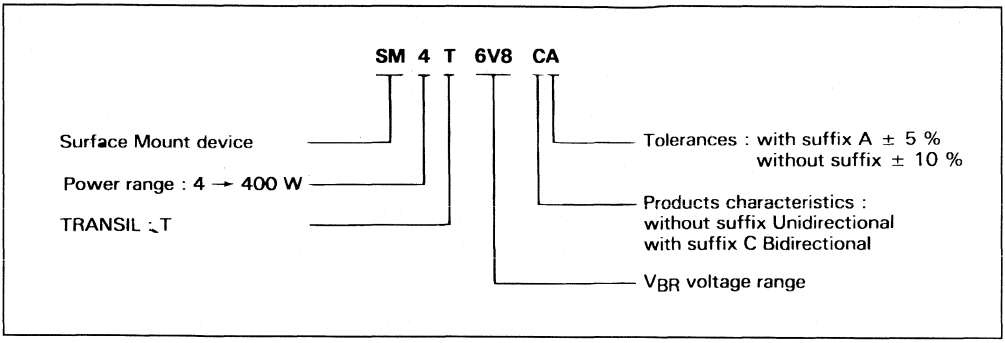
ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		Marking		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirectional	Bidirectional	Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
SM4T6V8	SM4T6V8C	QD	VD	1000	5.5	6.12	6.8	7.48	10	10.8	37	14	164	5.7	3500
SM4T6V8A	SM4T6V8CA	QE	VE	1000	5.8	6.45	6.8	7.14	10	10.5	38	13.4	174	5.7	3500
SM4T7V5	SM4T7V5C	QF	VF	500	6.05	6.75	7.5	8.25	10	11.7	34	15.2	151	6.1	3100
SM4T7V5A	SM4T7V5CA	QG	VG	500	6.4	7.13	7.5	7.88	10	11.3	35.4	14.5	160	6.1	3100
SM4T10	SM4T10C	QN	VN	10	8.1	9	10	11	1	15	27	19.5	246	7.3	2000
SM4T10A	SM4T10CA	QP	VP	10	8.55	9.5	10	10.5	1	14.5	27.6	18.6	258	7.3	2000
SM4T12	SM4T12C	QS	VS	5	9.72	10.8	12	13.2	1	17.3	23.1	22.7	211	7.8	1550
SM4T12A	SM4T12CA	QT	VT	5	10.2	11.4	12	12.6	1	16.7	24	21.7	221	7.8	1550
SM4T15	SM4T15C	QW	VW	5	12.1	13.5	15	16.5	1	22	18.2	28.4	169	8.4	1200
SM4T15A	SM4T15CA	QX	VX	5	12.8	14.3	15	15.8	1	21.2	19	27.2	176	8.4	1200
SM4T18	SM4T18C	RD	UD	5	14.5	16.2	18	19.8	1	26.5	15.1	34	141	8.8	975
SM4T18A	SM4T18CA	RE	UE	5	15.3	17.1	18	18.9	1	25.2	16	32.5	148	8.8	975
SM4T22	SM4T22C	RH	UH	5	17.8	19.8	22	24.2	1	31.9	12.5	41.2	116	9.2	800
SM4T22A	SM4T22CA	RK	UK	5	18.8	20.9	22	23.1	1	30.6	13	39.3	122	9.2	800
SM4T24	SM4T24C	RL	UL	5	19.4	21.6	24	26.4	1	34.7	11.5	44.9	107	9.4	725
SM4T24A	SM4T24CA	RM	UM	5	20.5	22.8	24	25.2	1	33.2	12	42.8	112	9.4	725
SM4T27	SM4T27C	RN	UN	5	21.8	24.3	27	29.7	1	39.1	10.2	50.5	95	9.6	625
SM4T27A	SM4T27CA	RP	UP	5	23.1	25.7	27	28.4	1	37.5	10.7	48.3	99	9.6	625
SM4T30	SM4T30C	RQ	UQ	5	24.3	27	30	33	1	43.5	9.2	56.1	86	9.7	575
SM4T30A	SM4T30CA	RR	UR	5	25.6	28.5	30	31.5	1	41.5	9.6	53.5	90	9.7	575
SM4T33	SM4T33C	RS	US	5	26.8	29.7	33	36.3	1	47.7	8.4	61.7	78	9.8	510
SM4T33A	SM4T33CA	RT	UT	5	28.2	31.4	33	34.7	1	45.7	8.8	59	81.5	9.8	510
SM4T36	SM4T36C	RU	UU	5	29.1	32.4	36	39.6	1	52	7.7	67.3	71	9.9	480
SM4T36A	SM4T36CA	RV	UV	5	30.8	34.2	36	37.8	1	49.9	8	64.3	74.5	9.9	480
SM4T39	SM4T39C	RW	UW	5	31.6	35.1	39	42.9	1	56.4	7.1	73	66	10.0	450
SM4T39A	SM4T39CA	RX	UX	5	33.3	37.1	39	41	1	53.9	7.4	69.7	69	10.0	450
SM4T68	SM4T68C	SN	WN	5	55.1	61.2	68	74.8	1	98	4.1	127	38	10.4	270
SM4T68A	SM4T68CA	SP	WP	5	58.1	64.6	68	71.4	1	92	4.3	121	39.5	10.4	270
SM4T100	SM4T100C	SW	WW	5	81	90	100	110	1	144	2.8	187	25.5	10.6	200
SM4T100A	SM4T100CA	SX	WX	5	85.5	95	100	105	1	137	2.9	178	27	10.6	200
SM4T150	SM4T150C	TH	XH	5	121	135	150	165	1	215	1.9	277	17.3	10.8	145
SM4T150A	SM4T150CA	TK	XK	5	128	143	150	158	1	207	2	265	18.1	10.8	145
SM4T200	SM4T200C	TS	XS	5	162	180	200	220	1	287	1.4	370	13	10.8	120
SM4T200A	SM4T200CA	TT	XT	5	171	190	200	210	1	274	1.5	353	13.6	10.8	120
SM4T220		TU		5	178	198	220	242	1	315	1.3	406	11.8	10.8	110
SM4T220A		TV		5	188	209	220	231	1	301	1.4	388	12.4	10.8	110

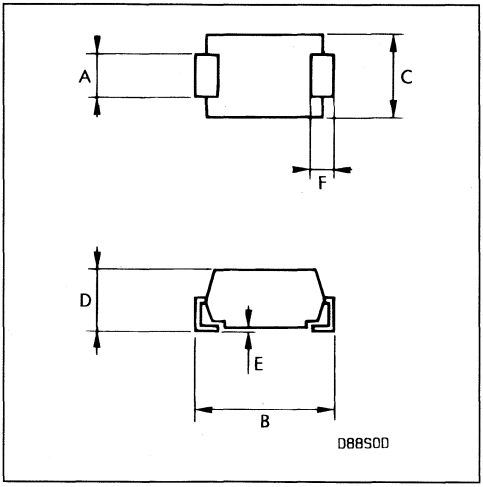
* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.

ORDER CODE



PACKAGE MECHANICAL DATA

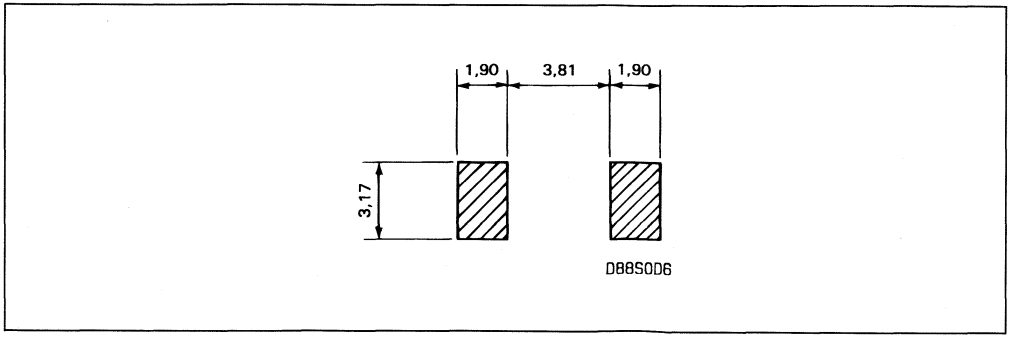
SOD 6 Plastic



Ref.	Millimetres		Inches	
	Min.	Max.	Min.	Max.
A	2.8	3.2	0.110	0.126
B	6.0	6.4	0.236	0.252
C	3.8	4.2	0.150	0.165
D	2.5	3.1	0.098	0.122
E	–	0.1	–	0.004
F	0.9	1.3	0.035	0.051

Laser marking.
The logo indicates cathode for unidirectional types.

FOOT PRINT DIMENSIONS (Millimeters)



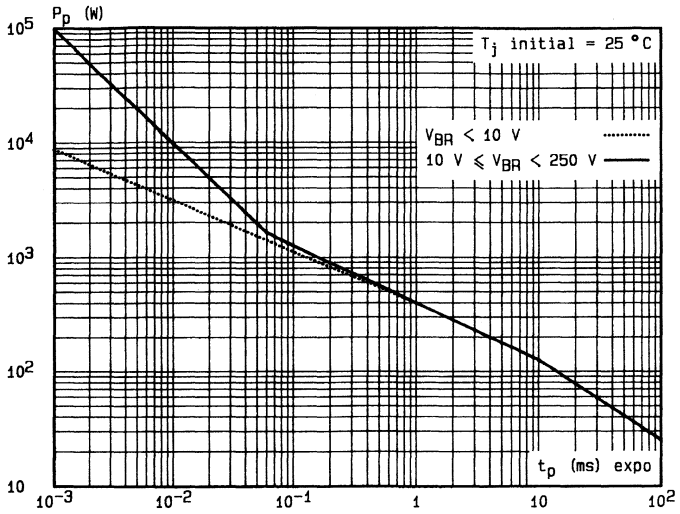


Fig.1 - Peak pulse power versus exponential pulse duration.

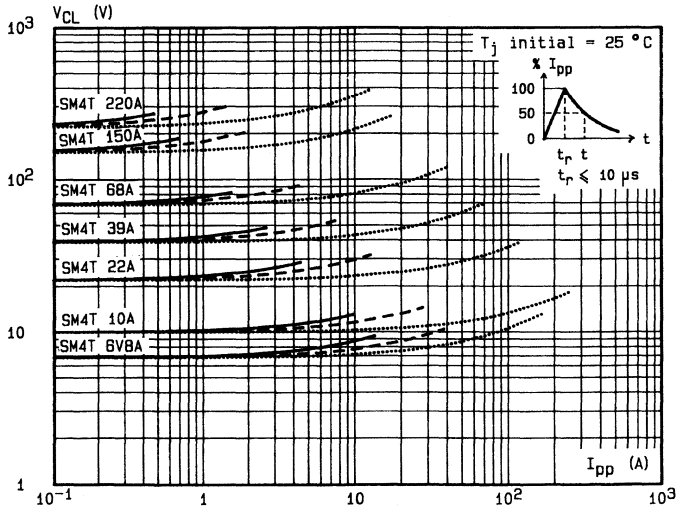


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ———

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

DB8SM4TP4

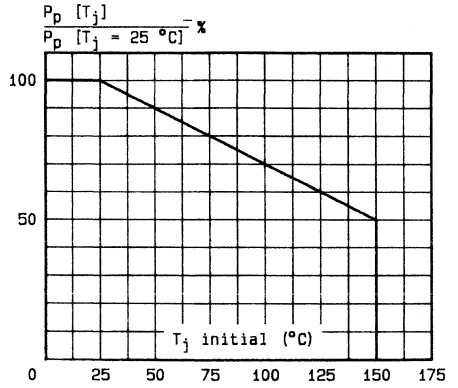


Fig.3 - Allowable power dissipation versus junction temperature.

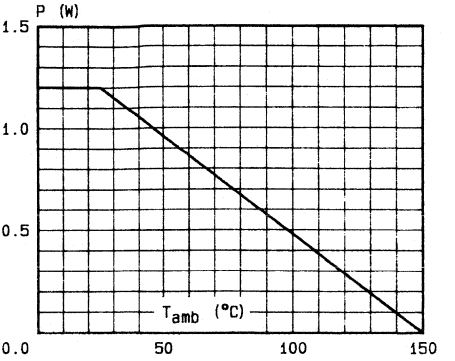


Fig.4 - Power dissipation versus ambient temperature.

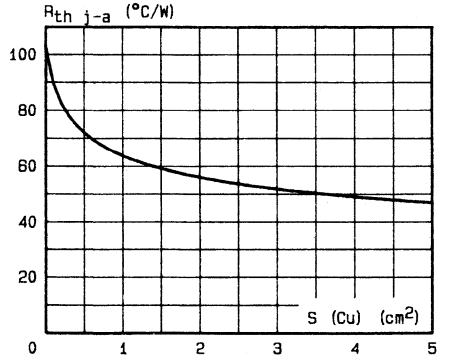


Fig.5 - Thermal resistance junction-ambient versus Cu surface (printed circuit).

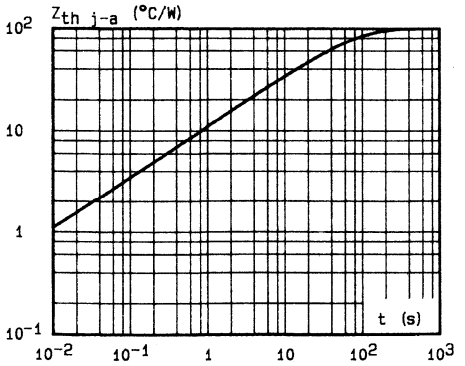


Fig.6 - Transient thermal impedance junction-ambient versus pulse duration.

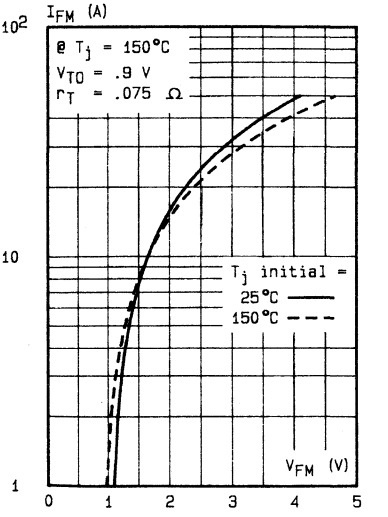


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88SM4TP5

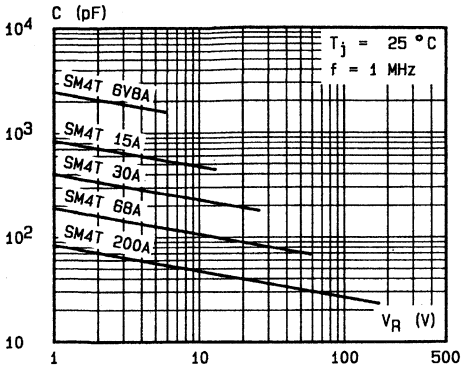


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

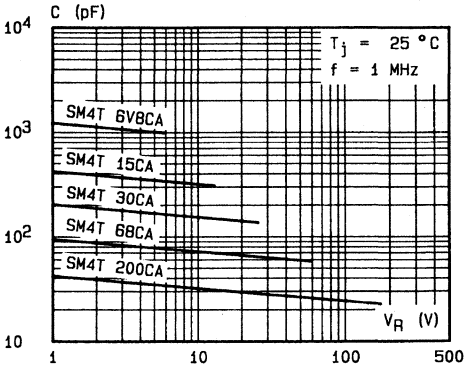


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88SM4TP6

SGS-THOMSON MICROELECTRONICS

SM6T6V8, A → 220, A
SM6T6V8C, A → 200C, A

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 600 W / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 5.5 V → 188 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES

SOD 6
(Plastic)

SURFACE MOUNT TRANSIL FEATURES

- A PERFECT PICK AND PLACE BEHAVIOUR
- AN EXCELLENT ON BOARD STABILITY
- A FULL COMPATIBILITY WITH BOTH GLUING AND PASTE SOLDERING TECHNOLOGIES
- BODY MARKED WITH TYPE CODE AND LOGO
- STANDARD PACKAGING : 12 mm TAPE (EIA STD. RS481)
- TINNED COPPER LEADS
- HIGH TEMPERATURE RESISTANT RESIN

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

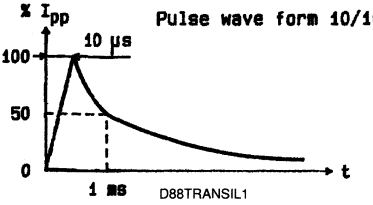
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	600	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 25 °C	1.2	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	50	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 175 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s		260	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



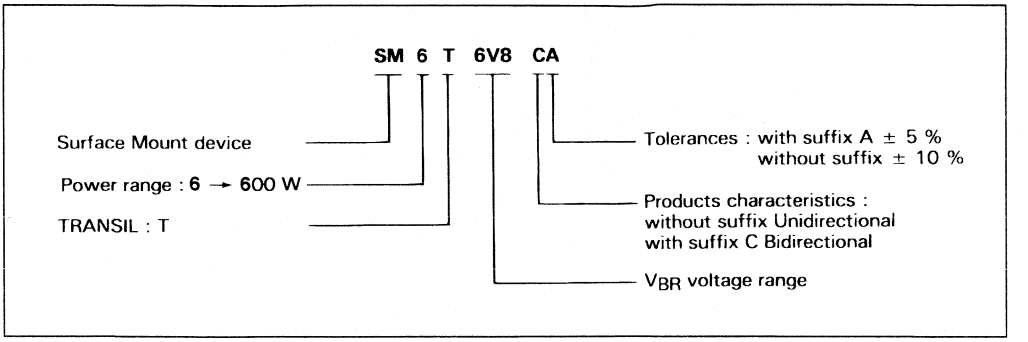
ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		Marking		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirec-tional	Bidirec-tional	Unidirec-tional	Bidirec-tional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
SM6T6V8	SM6T6V8C	DD	LD	1000	5.5	6.12	6.8	7.48	10	10.8	55	14	250	5.7	4000
SM6T6V8A	SM6T6V8CA	DE	LE	1000	5.8	6.45	6.8	7.14	10	10.5	57	13.4	261	5.7	4000
SM6T7V5	SM6T7V5C	DF	LF	500	6.05	6.75	7.5	8.25	10	11.7	51	15.2	230	6.1	3700
SM6T7V5A	SM6T7V5CA	DG	LG	500	6.4	7.13	7.5	7.88	10	11.3	53	14.5	241	6.1	3700
SM6T10	SM6T10C	DN	LN	10	8.1	9.0	10	11	1	15	40	19.5	369	7.3	2800
SM6T10A	SM6T10CA	DP	LP	10	8.55	9.5	10	10.5	1	14.5	41	18.6	387	7.3	2800
SM6T12	SM6T12C	DS	LS	5	9.72	10.8	12	13.2	1	17.3	35	22.7	317	7.8	2300
SM6T12A	SM6T12CA	DT	LT	5	10.2	11.4	12	12.6	1	16.7	36	21.7	332	7.8	2300
SM6T15	SM6T15C	DW	LW	5	12.1	13.5	15	16.5	1	22	27.5	28.4	254	8.4	1900
SM6T15A	SM6T15CA	DX	LX	5	12.8	14.3	15	15.8	1	21.2	28	27.2	265	8.4	1900
SM6T18	SM6T18C	ED	MD	5	14.5	16.2	18	19.8	1	26.5	22.5	34	212	8.8	1600
SM6T18A	SM6T18CA	EE	ME	5	15.3	17.1	18	18.9	1	25.2	24	32.5	222	8.8	1600
SM6T22	SM6T22C	EH	MH	5	17.8	19.8	22	24.2	1	31.9	18.5	41.2	175	9.2	1350
SM6T22A	SM6T22CA	EK	MK	5	18.8	20.9	22	23.1	1	30.6	20	39.3	183	9.2	1350
SM6T24	SM6T24C	EL	ML	5	19.4	21.6	24	26.4	1	34.7	17.5	44.9	160	9.4	1250
SM6T24A	SM6T24CA	EM	MM	5	20.5	22.8	24	25.2	1	33.2	18	42.8	168	9.4	1250
SM6T27	SM6T27C	EN	MN	5	21.8	24.3	27	29.7	1	39.1	15.5	50.5	143	9.6	1150
SM6T27A	SM6T27CA	EP	MP	5	23.1	25.7	27	28.4	1	37.5	16	48.3	149	9.6	1150
SM6T30	SM6T30C	EQ	MQ	5	24.3	27	30	33	1	43.5	13.5	56.1	128	9.7	1075
SM6T30A	SM6T30CA	ER	MR	5	25.6	28.5	30	31.5	1	41.4	14.5	53.5	134	9.7	1075
SM6T33	SM6T33C	ES	MS	5	26.8	29.7	33	36.3	1	47.7	12.5	61.7	117	9.8	1000
SM6T33A	SM6T33CA	ET	MT	5	28.2	31.4	33	34.7	1	45.7	13.1	59	122	9.8	1000
SM6T36	SM6T36C	EU	MU	5	29.1	32.4	36	39.6	1	52	11.5	67.3	107	9.9	950
SM6T36A	SM6T36CA	EV	MV	5	30.8	34.2	36	37.8	1	49.9	12	64.3	112	9.9	950
SM6T39	SM6T39C	EW	MW	5	31.6	35.1	39	42.9	1	56.4	10.6	73	99	10.0	900
SM6T39A	SM6T39CA	EX	MX	5	33.3	37.1	39	41	1	53.9	11.1	69.7	103	10.0	900
SM6T68	SM6T68C	FP	NP	5	55.1	61.2	68	74.8	1	98	6.1	127	57	10.4	625
SM6T68A	SM6T68CA	FQ	NQ	5	58.1	64.6	68	71.4	1	92	6.5	121	59.5	10.4	625
SM6T100	SM6T100C	FX	NX	5	81	90	100	110	1	144	4.2	187	38.5	10.6	500
SM6T100A	SM6T100CA	FY	NY	5	85.5	95	100	105	1	137	4.4	178	40.5	10.6	500
SM6T150	SM6T150C	GK	OK	5	121	135	150	165	1	215	2.8	277	26	10.8	400
SM6T150A	SM6T150CA	GL	OL	5	128	143	150	158	1	207	2.9	265	27.2	10.8	400
SM6T200	SM6T200C	GT	OT	5	162	180	200	220	1	287	2.1	370	19.4	10.8	350
SM6T200A	SM6T200CA	GU	OU	5	171	190	200	210	1	274	2.2	353	20.4	10.8	350
SM6T220		GV		5	178	198	220	242	1	316	1.9	406	17.7	10.8	330
SM6T220A		GW		5	188	209	220	231	1	301	2	388	18.6	10.8	330

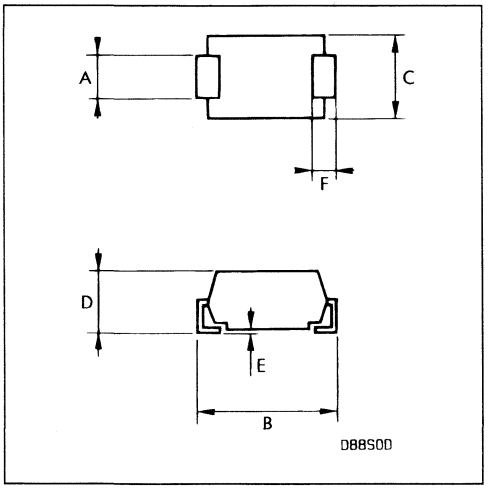
* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.

ORDER CODE



PACKAGE MECHANICAL DATA

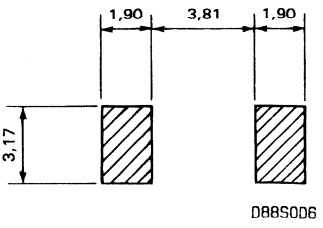
SOD 6 Plastic



Ref.	Millimetres		Inches	
	Min.	Max.	Min.	Max.
A	2.8	3.2	0.110	0.126
B	6.0	6.4	0.236	0.252
C	3.8	4.2	0.150	0.165
D	2.5	3.1	0.098	0.122
E	–	0.1	–	0.004
F	0.9	1.3	0.035	0.051

Laser marking.
The logo indicates cathode for unidirectional types.

FOOT PRINT DIMENSIONS (Millimeters)



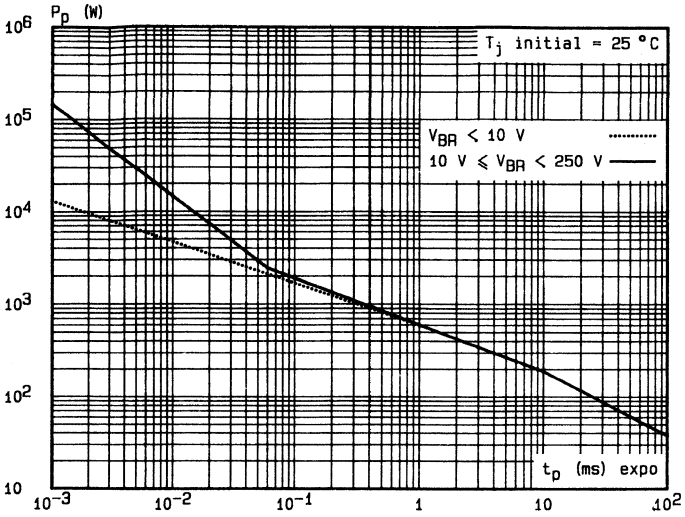


Fig.1 - Peak pulse power versus exponential pulse duration.

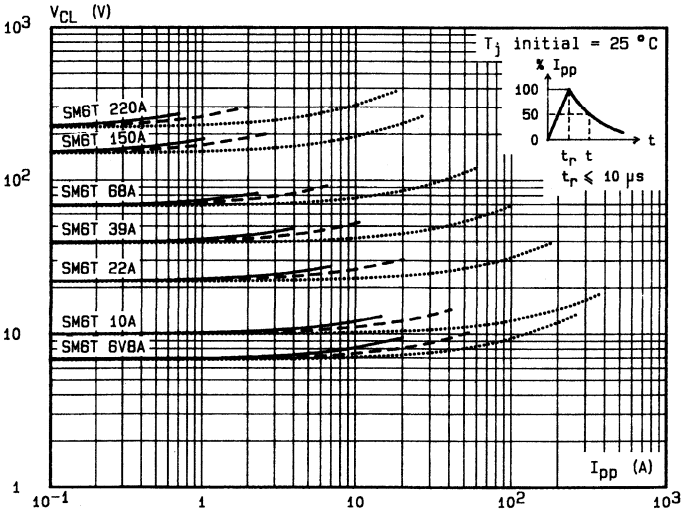


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

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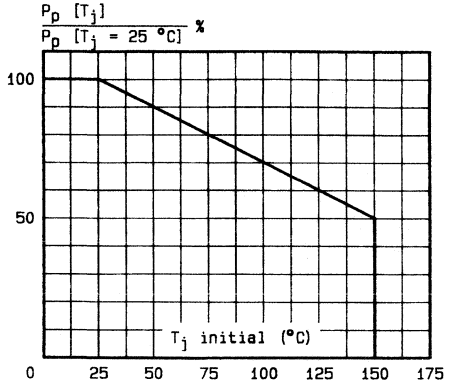


Fig.3 - Allowable power dissipation versus junction temperature.

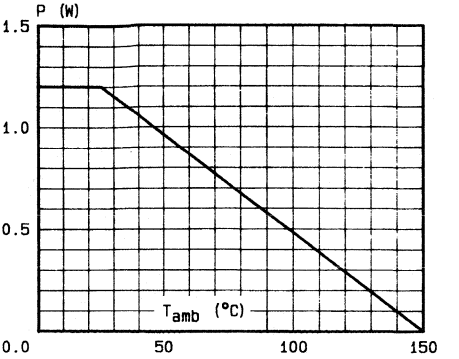


Fig.4 - Power dissipation versus ambient temperature.

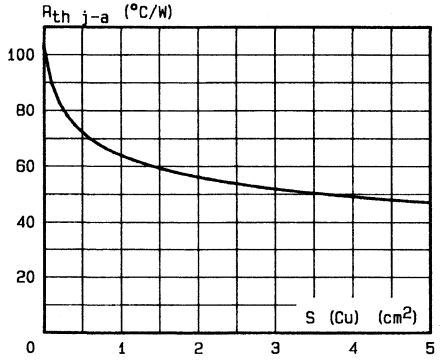


Fig.5 - Thermal resistance junction-ambient versus Cu surface (printed circuit).

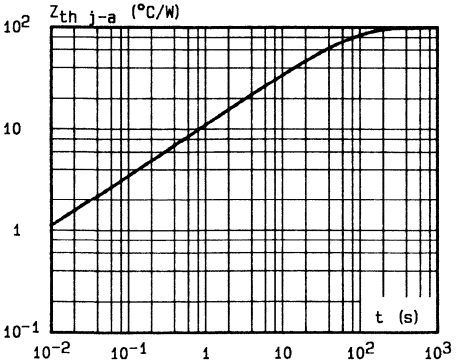


Fig.6 - Transient thermal impedance junction-ambient versus pulse duration.

D88SM6TP5

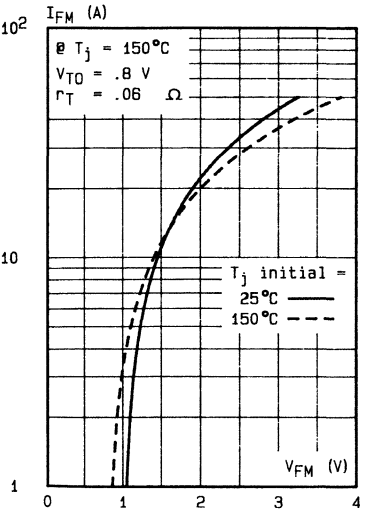


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

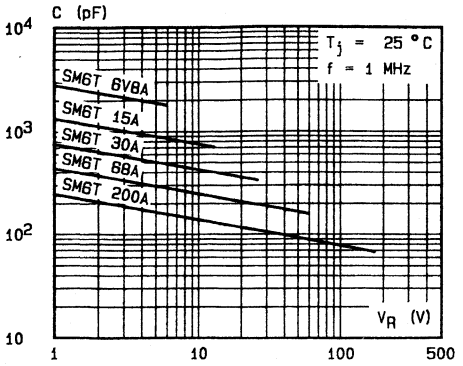


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

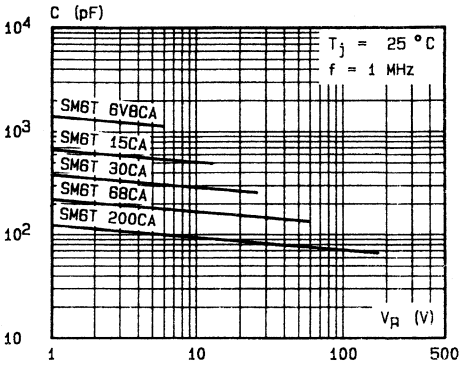


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

DB8SM6TP6

SM15T6V8, A → 220, A
SM15T6V8C, A → 200C, A

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY :
  1.5 kW / 1 ms EXPO
- VERY FAST CLAMPING TIME :
  1 ps FOR UNIDIRECTIONAL TYPES
  5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE :
  5.5 V → 188 V
- ORDER CODE :
  TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES

SOD 15
(Plastic)

SURFACE MOUNT TRANSIL FEATURES

- A PERFECT PICK AND PLACE BEHAVIOUR
- AN EXCELLENT ON BOARD STABILITY
- A FULL COMPATIBILITY WITH BOTH GLUING AND PASTE SOLDERING TECHNOLOGIES
- BODY MARKED WITH TYPE CODE AND LOGO
- STANDARD PACKAGING : 12 mm TAPE (EIA STD. RS481)
- TINNED COPPER LEADS
- HIGH TEMPERATURE RESISTANT RESIN

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

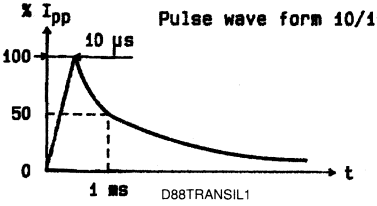
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	1500	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 25 °C	1.7	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	150	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 175 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s		260	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads	10	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



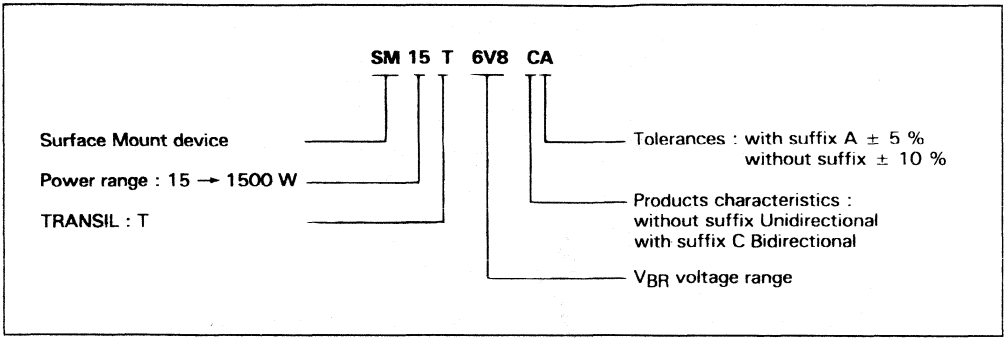
ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		Marking		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirec-tional	Bidirec-tional	Unidirec-tional	Bidirec-tional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
SM15T6V8	SM15T6V8C	MDD	BDD	1000	5.5	6.12	6.8	7.48	10	10.8	139	14	714	5.7	9500
SM15T6V8A	SM15T6V8CA	MDE	BDE	1000	5.8	6.45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
SM15T7V5	SM15T7V5C	MDF	BDF	1000	6.05	6.75	7.5	8.25	10	11.7	128	15.2	660	6.1	8500
SM15T7V5A	SM15T7V5CA	MDG	BDG	1000	6.4	7.13	7.5	7.88	10	11.3	132	14.5	690	6.1	8500
SM15T10	SM15T10C	MDN	BDN	10	8.1	9.0	10	11	1	15	100	19.5	928	7.3	7000
SM15T10A	SM15T10CA	MDP	BDP	10	8.55	9.5	10	10.5	1	14.5	103	18.6	968	7.3	7000
SM15T12	SM15T12C	MDS	BDS	5	9.72	10.8	12	13.2	1	17.3	87	22.7	793	7.8	6000
SM15T12A	SM15T12CA	MDT	BDT	5	10.2	11.4	12	12.6	1	16.7	90	21.7	829	7.8	6000
SM15T15	SM15T15C	MDW	BDW	5	12.1	13.5	15	16.5	1	22	68	28.4	634	8.4	5000
SM15T15A	SM15T15CA	MDX	BDX	5	12.8	14.3	15	15.8	1	21.2	71	27.2	662	8.4	5000
SM15T18	SM15T18C	MED	BED	5	14.5	16.2	18	19.8	1	26.5	56.5	34	529	8.8	4300
SM15T18A	SM15T18CA	MEE	BEE	5	15.3	17.1	18	18.9	1	25.2	59.5	32.5	554	8.8	4300
SM15T22	SM15T22C	MEH	BEH	5	17.8	19.8	22	24.2	1	31.9	47	41.2	437	9.2	3700
SM15T22A	SM15T22CA	MEK	BEK	5	18.8	20.9	22	23.1	1	30.6	49	39.3	458	9.2	3700
SM15T24	SM15T24C	MEL	BEL	5	19.4	21.6	24	26.4	1	34.7	43	44.9	401	9.4	3500
SM15T24A	SM15T24CA	MEM	BEM	5	20.5	22.8	24	25.2	1	33.2	45	42.8	421	9.4	3500
SM15T27	SM15T27C	MEN	BEN	5	21.8	24.3	27	29.7	1	39.1	38.5	50.5	356	9.6	3200
SM15T27A	SM15T27CA	MEP	BEP	5	23.1	25.7	27	28.4	1	37.5	40	48.3	373	9.6	3200
SM15T30	SM15T30C	MEQ	BEQ	5	24.3	27	30	33	1	43.5	34.5	56.1	321	9.7	2900
SM15T30A	SM15T30CA	MER	BER	5	25.6	28.5	30	31.5	1	41.4	36	53.5	336	9.7	2900
SM15T33	SM15T33C	MES	BES	5	26.8	29.7	33	36.3	1	47.7	31.5	61.5	292	9.8	2700
SM15T33A	SM15T33CA	MET	BET	5	28.2	31.4	33	34.7	1	45.7	33	59	305	9.8	2700
SM15T36	SM15T36C	MEU	BEU	5	29.1	32.4	36	39.6	1	52	29	67.3	267	9.9	2500
SM15T36A	SM15T36CA	MEV	BEV	5	30.8	34.2	36	37.8	1	49.9	30	64.3	280	9.9	2500
SM15T39	SM15T39C	MEW	BEW	5	31.6	35.1	39	42.9	1	56.4	26.5	73	246	10.0	2400
SM15T39A	SM15T39CA	MEX	BEX	5	33.3	37.1	39	41	1	53.9	28	69.7	258	10.0	2400
SM15T68	SM15T68C	MFN	BFN	5	55.1	61.2	68	74.8	1	98	15.3	127	142	10.4	1550
SM15T68A	SM15T68CA	MFP	BFP	5	58.1	64.6	68	71.4	1	92	16.3	121	148	10.4	1550
SM15T100	SM15T100C	MFW	BFW	5	81	90	100	110	1	144	10.4	187	96	10.6	1150
SM15T100A	SM15T100CA	MFX	BFX	5	85.5	95	100	105	1	137	11	178	101	10.6	1150
SM15T150	SM15T150C	MGH	BGH	5	121	135	150	165	1	215	7	277	65	10.8	850
SM15T150A	SM15T150CA	MGK	BGK	5	128	143	150	158	1	207	7.2	265	68	10.8	850
SM15T200	SM15T200C	MGU	BGU	5	162	180	200	220	1	287	5.2	370	48.5	10.8	675
SM15T200A	SM15T200CA	MGV	BGV	5	171	190	200	210	1	274	5.5	353	51	10.8	675
SM15T220		MGW		5	175	198	220	242	1	344	4.3	406	44.5	10.8	625
SM15T220A		MGX		5	185	209	220	231	1	328	4.6	388	46.5	10.8	625

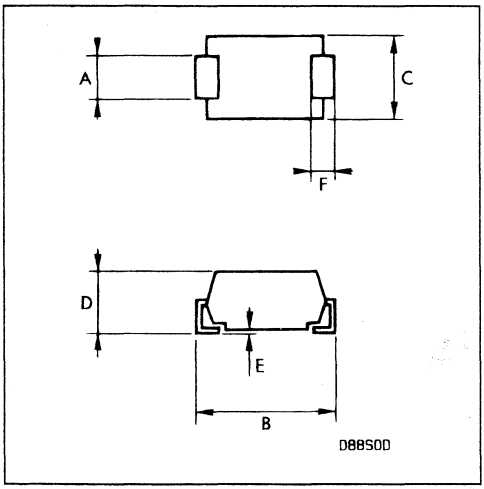
* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.

ORDER CODE



PACKAGE MECHANICAL DATA

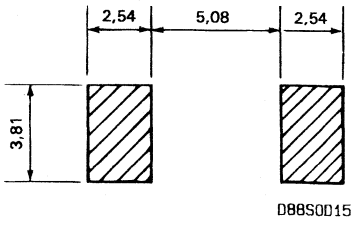
SOD 15 Plastic



Ref.	Millimetres		Inches	
	Min.	Max.	Min.	Max.
A	2.8	3.2	0.110	0.126
B	7.6	8.0	0.300	0.315
C	4.8	5.2	0.190	0.200
D	2.5	3.1	0.098	0.122
E	–	0.1	–	0.004
F	1.3	1.7	0.051	0.067

Laser marking.
The logo indicates cathode for unidirectional types.

FOOT PRINT DIMENSIONS (Millimeters)



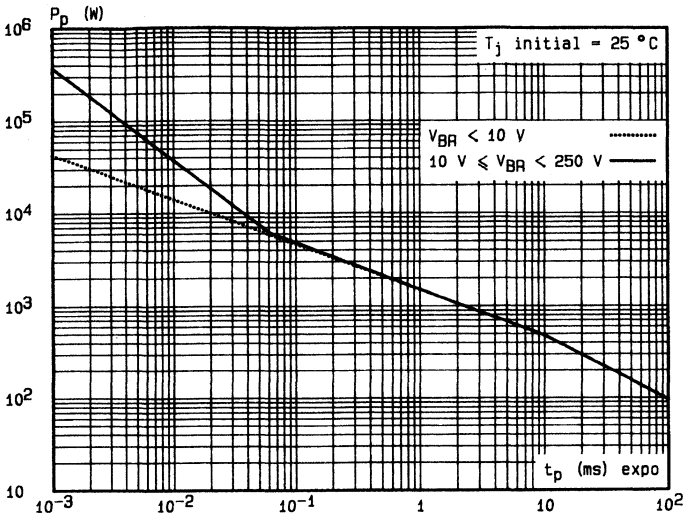


Fig.1 - Peak pulse power versus exponential pulse duration.

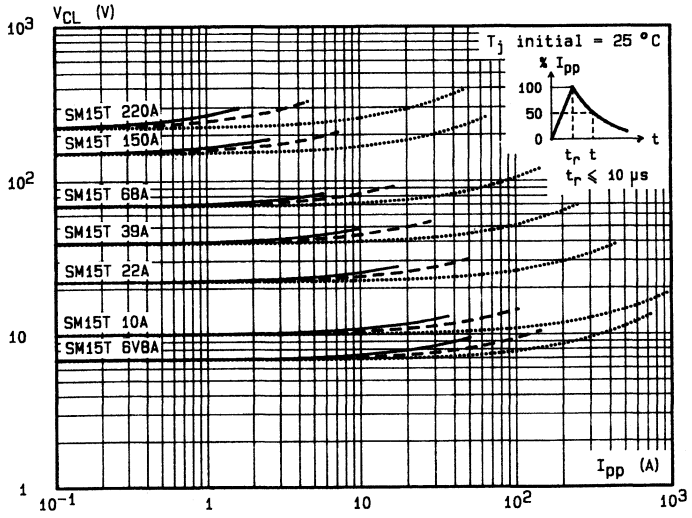


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ———

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

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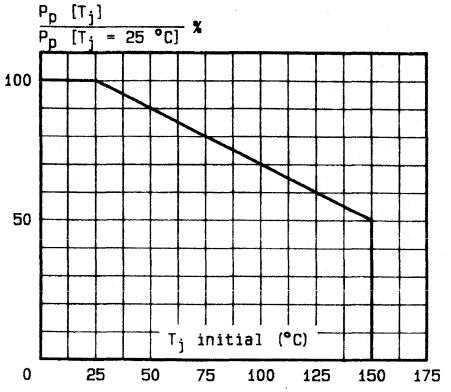


Fig.3 - Allowable power dissipation versus junction temperature.

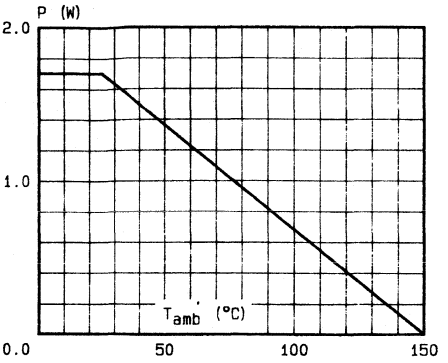


Fig.4 - Power dissipation versus ambient temperature.

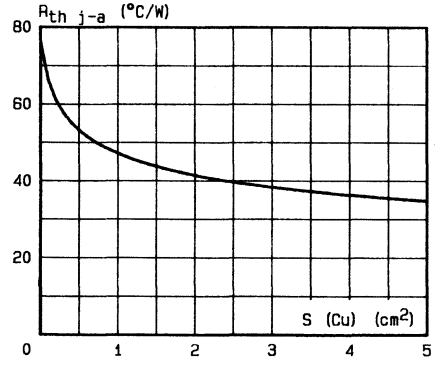


Fig.5 - Thermal resistance junction-ambient versus Cu surface (printed circuit).

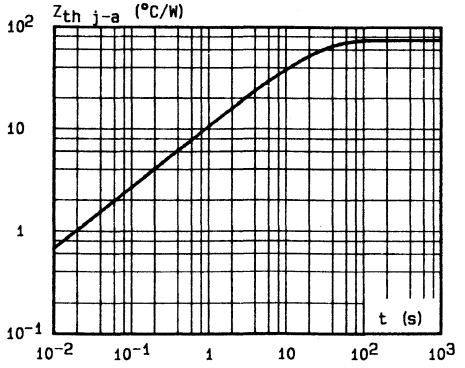


Fig.6 - Transient thermal impedance junction-ambient versus pulse duration.

D88SM15TP5

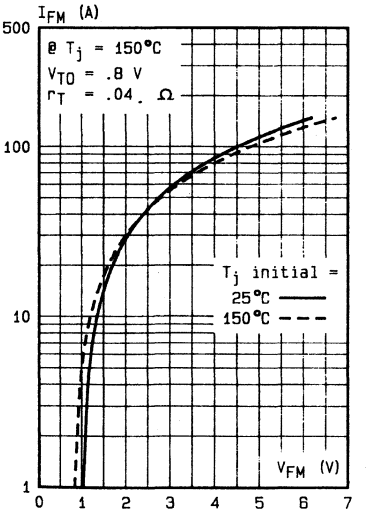


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

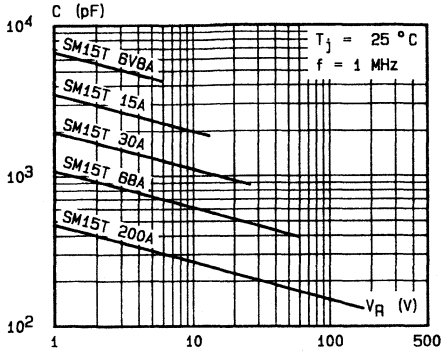


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

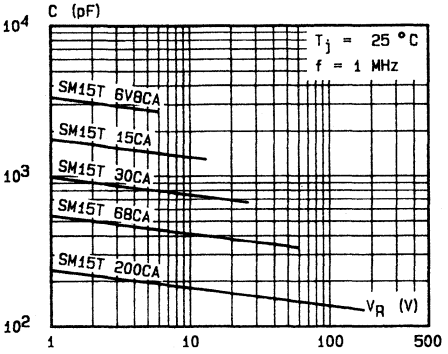
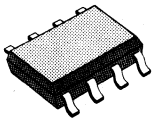


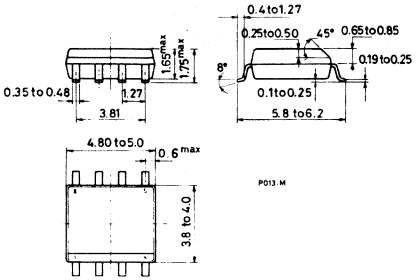
Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88SM15TP6

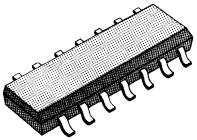
PACKAGES

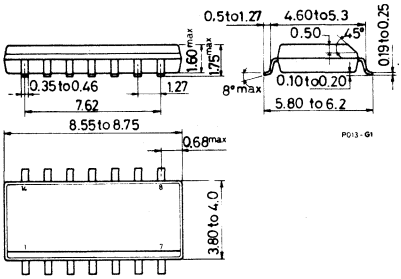
SO-8J





SO-14J





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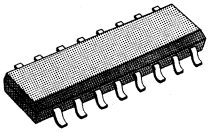
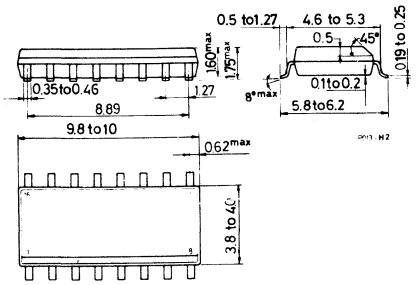
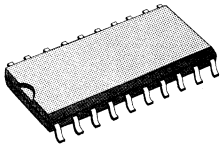
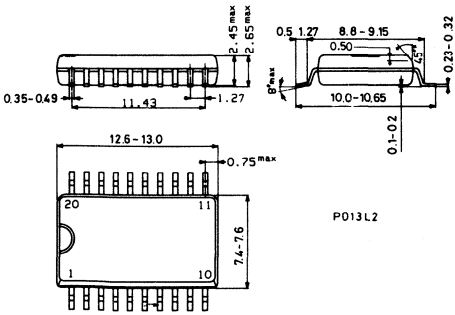




SO-20L
SO-20 (12+4+4)





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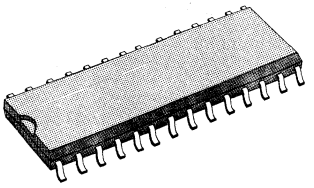
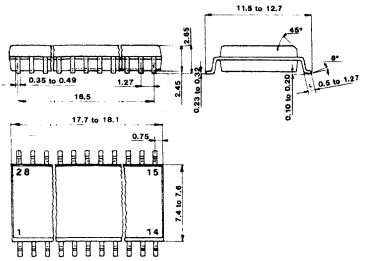
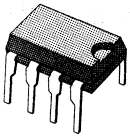
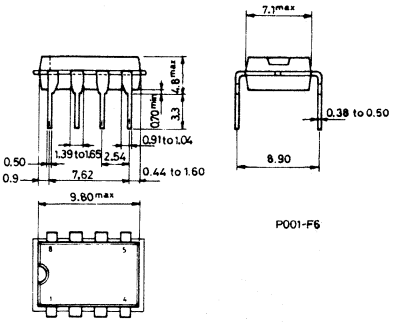


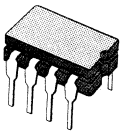


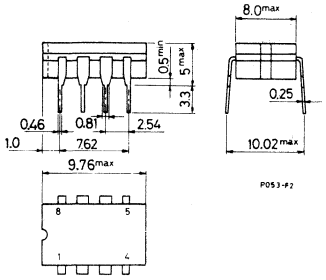
8 lead Plastic Minidip
4 + 4 lead Powerdip



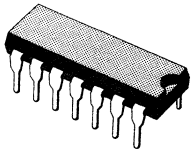


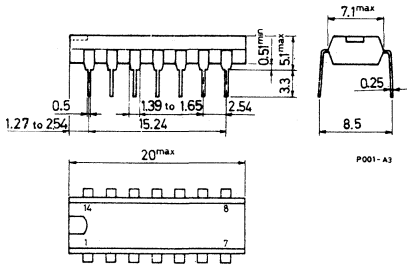
8 lead Ceramic Minidip



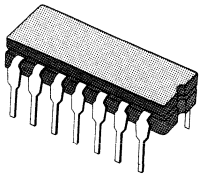


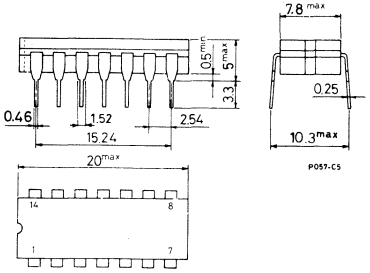
14 lead Plastic Dip



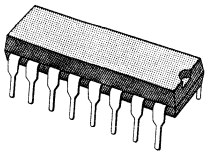


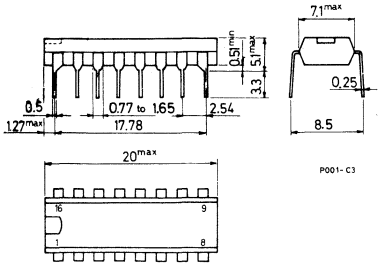
14 lead Ceramic Dip



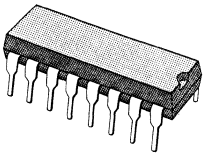


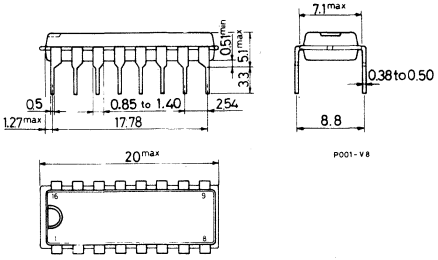
16 lead Plastic Dip (0.25)



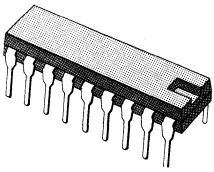


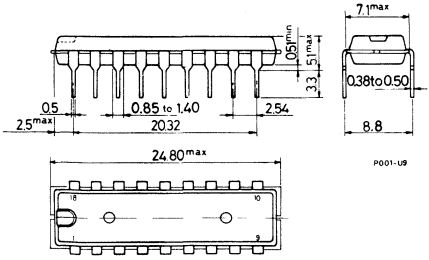
16 lead Plastic Dip (0.4)
8 + 8 lead Powerdip
12 + 2 + 2 lead Powerdip



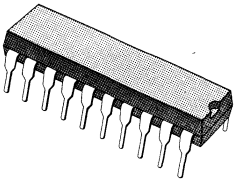


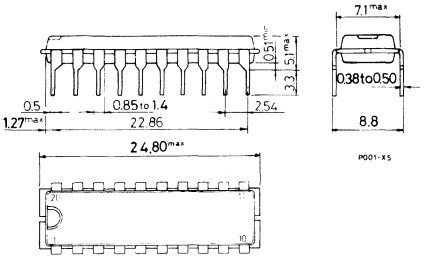
18 lead Plastic Dip



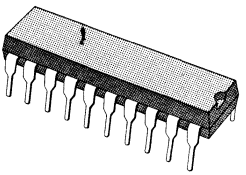


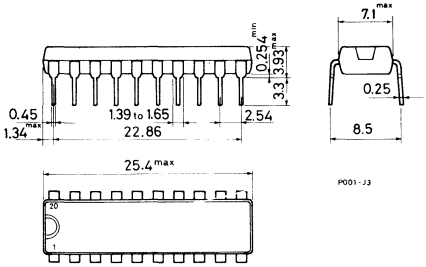
20 lead Plastic Dip (0.4)
16 + 2 + 2 Powerdip



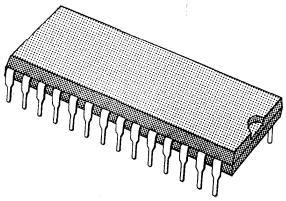


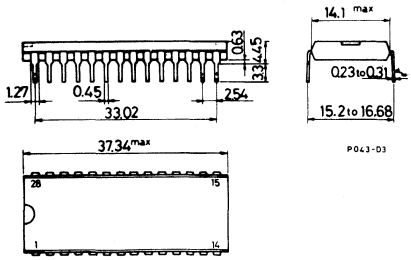
20 lead Plastic Dip (0.25)



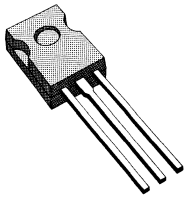


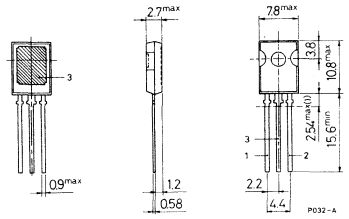
28 lead Plastic Dip





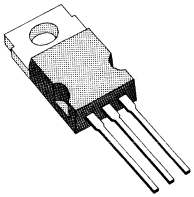
SOT-82

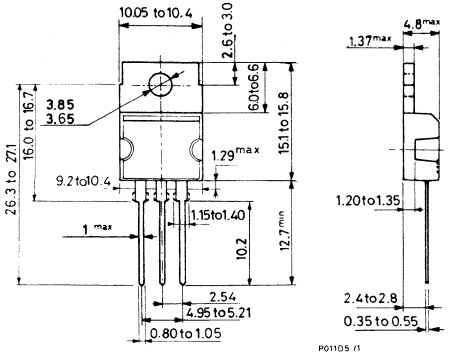




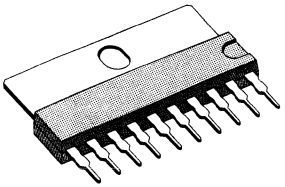
(1) Within this region the cross-section of the leads is uncontrolled

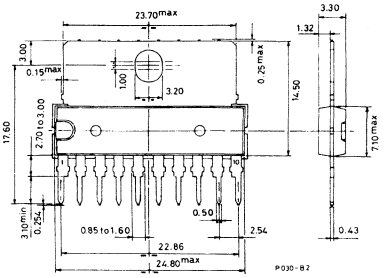
TO-220



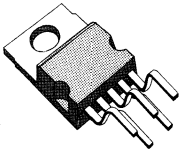


SIP-10

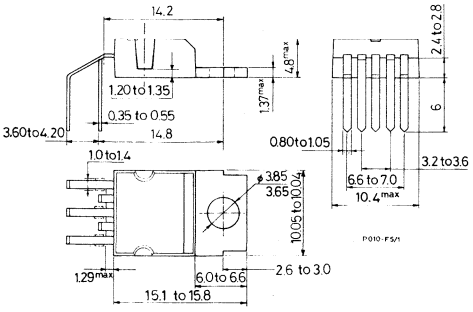




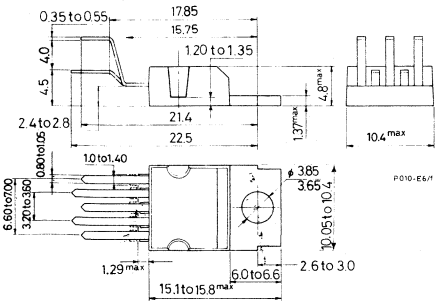
PENTAWATT



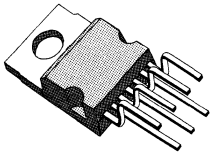
Horizontal Version



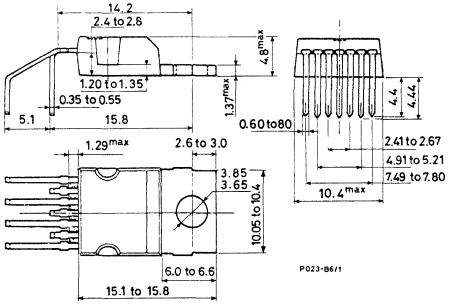
Vertical Version



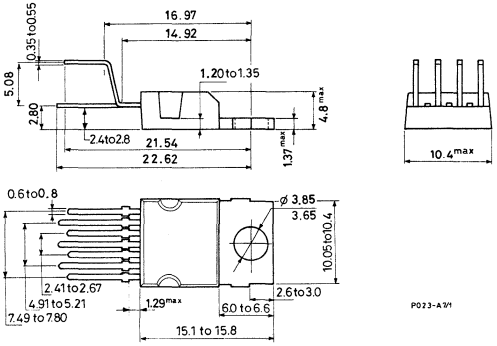
HEPTAWATT



Horizontal Version



Vertical Version



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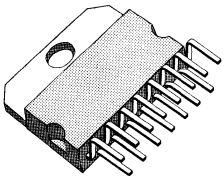
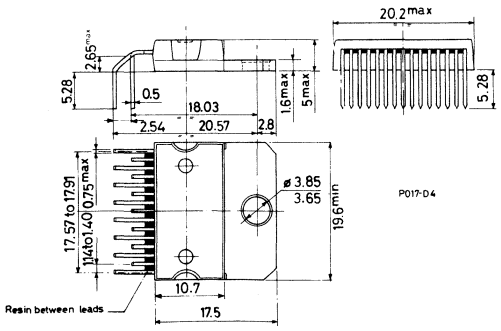
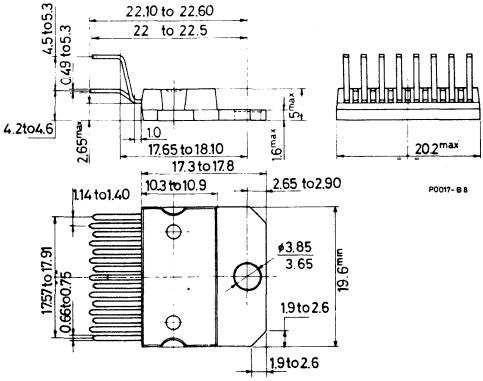


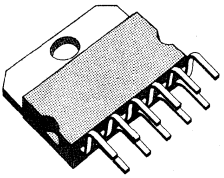
Horizontal Version

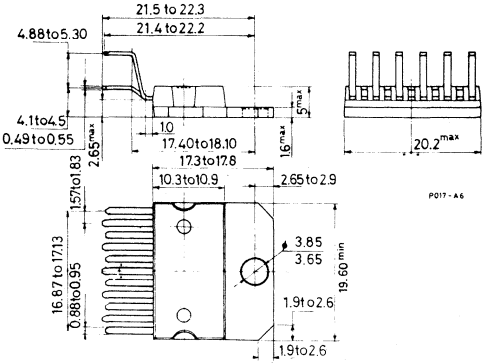


Vertical Version

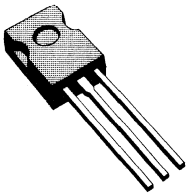


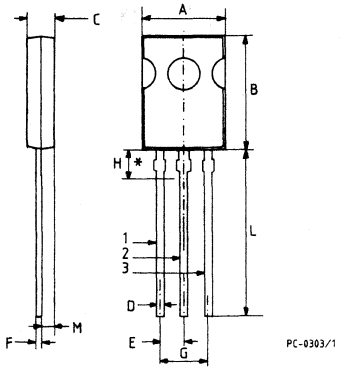
MULTIWATT-11





SOT-82 (Discrete)



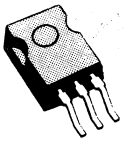


	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	7.4	7.8	0.295	0.307
B	10.5	10.8	0.413	0.425
C	2.4	2.7	0.094	0.106
D	0.7	0.9	0.027	0.035
E	2.2 typ.		0.087 typ.	
F	0.49	0.75	0.019	0.029
G	4.4 typ.		0.173 typ.	
H	2.54 typ.		0.100 typ.	
L	15.7 typ.		0.618 typ.	
M	1.2 typ.		0.047 typ.	

pin 1: Base - pin 2: Collector - pin 3: Emitter

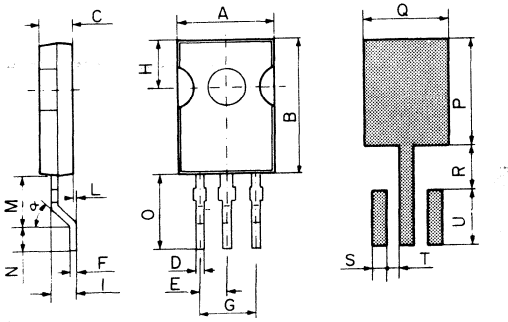
*: WITHIN THIS REGION THE CROSS-SECTION OF THE LEADS IS UNCONTROLLED

SOT-194



LEAD FORMED SOT-82 FOR SURFACE MOUNTING ASSEMBLY

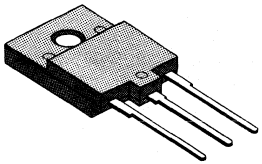
MECHANICAL DATA



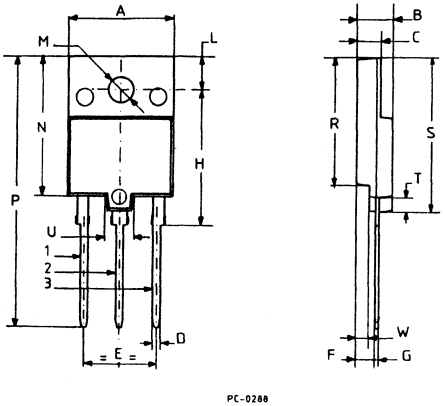
PC-0276

	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	7.4	7.8	0.295	0.307
B	10.5	10.8	0.413	0.425
C	2.4	2.7	0.094	0.106
D	0.7	0.9	0.027	0.035
E	2.2 typ.		0.087 typ.	
F	0.45	0.65	0.017	0.026
G	4.4 typ.		0.173 typ.	
H	3.8 typ.		0.149 typ.	
I	1.8 typ.		0.070 typ.	
L	0.1 typ.		0.004 typ.	
M	3.8	4.2	0.149	0.165
N	2 typ.		0.078 typ.	
O	6 typ.		0.236 typ.	
α	45°		45°	
P	8.5 typ.		0.334 typ.	
Q	6.7 typ.		0.263 typ.	
R	3.5 typ.		0.137 typ.	
S	1.2 typ.		0.047 typ.	
T	1 typ.		0.039 typ.	
U	4.5 typ.		0.177 typ.	

ISOWATT-218



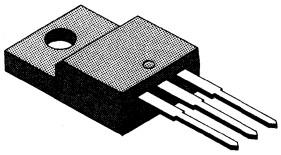
MECHANICAL DATA



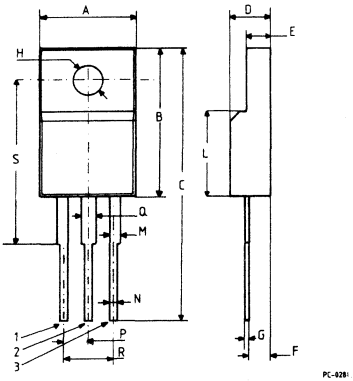
	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	15.8	16.2	0.622	0.637
B	5.35	5.65	0.210	0.222
C	3.3	3.8	0.130	0.149
D	1.05	1.25	0.041	0.049
E	10.8	11.2	0.425	0.441
F	2.9	3.1	0.114	0.122
G	0.45	1	0.017	0.039
H	20.25	20.75	0.797	0.817
L	4.85	5.25	0.190	0.206
M	3.5	3.7	0.137	0.145
N	20.8	21.2	0.818	0.834
P	40.5	42.5	1.594	1.673
R	19.1	19.9	0.752	0.783
S	22.8	23.6	0.897	0.929
T	2.1	2.3	0.082	0.090
U	4.6 typ.		0.181 typ.	
W	1.88	2.08	0.074	0.081

pin 1: Base - pin 2: Collector - pin 3: Emitter

ISOWATT-220



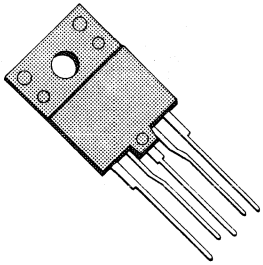
MECHANICAL DATA



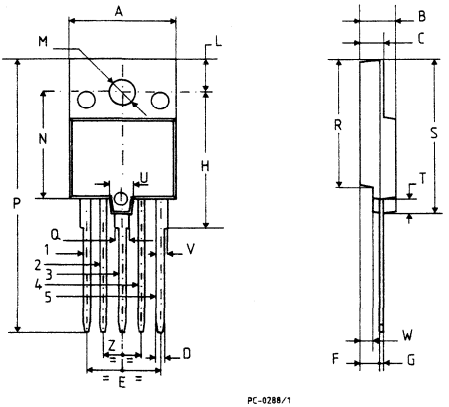
	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	10	10.4	0.393	0.409
B	15.9	16.4	0.626	0.645
C	28.6	30.6	1.126	1.204
D	4.4	4.6	0.173	0.181
E	2.5	2.7	0.098	0.106
F	2.4	2.75	0.094	0.108
G	0.4	0.7	0.015	0.027
H	3	3.2	0.118	0.126
L	9	9.3	0.354	0.366
M	1.15	1.7	0.045	0.067
N	0.75	1	0.030	0.039
P	2.4	2.7	0.094	0.106
Q	1.15	1.7	0.045	0.067
R	4.95	5.2	0.195	0.204
S	16 typ		0.630 typ	

pin 1: Base - pin 2: Collector - pin 3: Emitter

ISOWATT-5

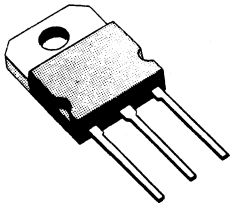


MECHANICAL DATA

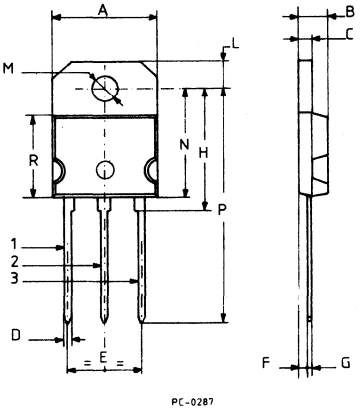


	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	15.8	16.2	0.622	0.637
B	5.35	5.65	0.210	0.222
C	3.3	3.8	0.130	0.149
D	0.75	1	0.029	0.039
E	10.16 typ.		0.400 typ.	
F	2.9	3.1	0.114	0.122
G	0.45	1	0.017	0.039
H	20.25	20.75	0.797	0.817
L	4.85	5.25	0.190	0.206
M	3.5	3.7	0.137	0.145
N	16 typ.		0.630 typ.	
P	40.5	42.5	1.594	1.673
Q	1.3 typ.		0.051 typ.	
R	19.1	19.9	0.752	0.783
S	22.8	23.6	0.897	0.929
T	2.1	2.3	0.082	0.090
U	3.1 typ.		0.122 typ.	
V	1.5 typ.		0.063 typ.	
W	1.88	2.08	0.074	0.081
Z	5.08 typ.		0.200 typ.	

TO-218 (SOT 93)



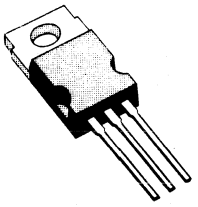
MECHANICAL DATA



	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	14.7	15.2	0.578	0.598
B	4.7	4.9	0.185	0.193
C	1.9	2.1	0.075	0.082
D	1.1	1.3	0.043	0.051
E	10.8	11.1	0.425	0.437
F	2.5 typ		0.098 typ	
G	0.5	0.78	0.019	0.030
H	18 typ		0.708 typ	
L	3.95	4.15	0.155	0.163
M	4	4.1	0.157	0.161
N	—	16.2	—	0.637
P	31 typ		1.220 typ	
R	—	12.2	—	0.480

pin 1: GATE - pin 2: DRAIN - pin 3: SOURCE

TO-220 (Discrete)



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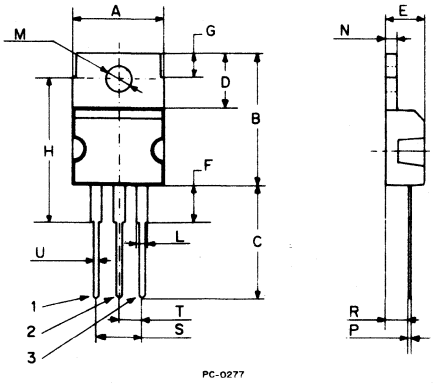
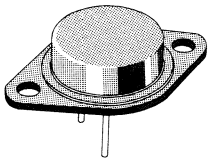


	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	10	10.4	0.393	0.409
B	15.2	15.9	0.598	0.626
C	12.7	13.7	0.500	0.539
D	6.2	6.6	0.244	0.260
E	4.4	4.6	0.173	0.181
F	3.5	5.5	0.137	0.216
G	2.65	2.95	0.104	0.116
H	17.6 typ.		0.692 typ.	
L	1.14	1.7	0.044	0.067
M	3.75	3.85	0.147	0.151
N	1.23	1.32	0.048	0.051
P	0.41	0.64	0.016	0.025
R	2.4	2.72	0.094	0.107
S	4.95	5.15	0.194	0.203
T	2.4	2.7	0.094	0.106
U	0.61	0.94	0.024	0.037

pin 1: GATE - pin 2: DRAIN - pin 3: SOURCE



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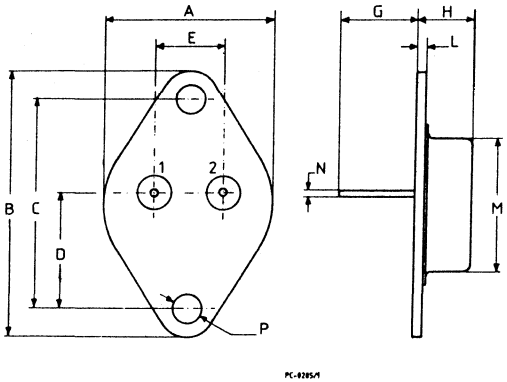

	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	25	26	0.984	1.023
B	38.5	39.3	1.515	1.547
C	30	30.3	1.181	1.193
D	16.5	17.2	0.649	0.677
E	10.7	11.1	0.421	0.437
G	11	13.1	0.433	0.515
H	8.32	8.92	0.327	0.351
L	1.5	1.65	0.059	0.065
M	19	20	0.748	0.787
N	0.97	1.15	0.038	0.045
P	4	4.09	0.157	0.161

pin 1: Base - pin 2: Emitter - pin 3: Collector

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